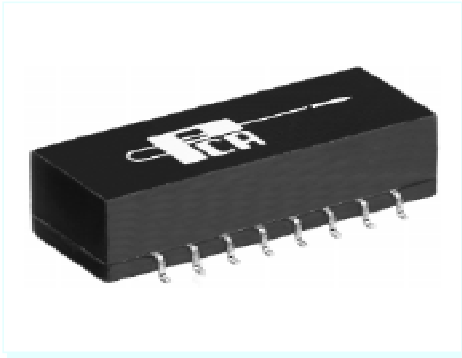


## EPF8048G



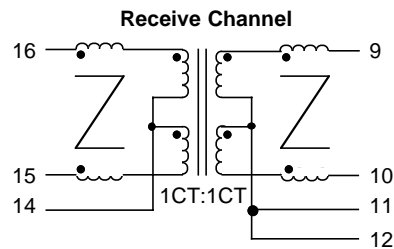
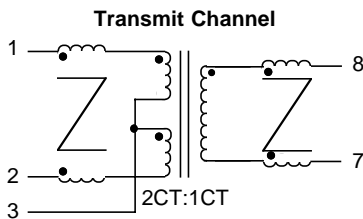
- Optimized to work with ML6692/94 PHY chip •
- Guaranteed to operate with 8 mA DC bias at 70°C on cable side •
- Complies with or exceeds IEEE 802.3, 100 BX Standards •
- Robust construction allows for most severe soldering processes •

### Electrical Parameters @ 25° C

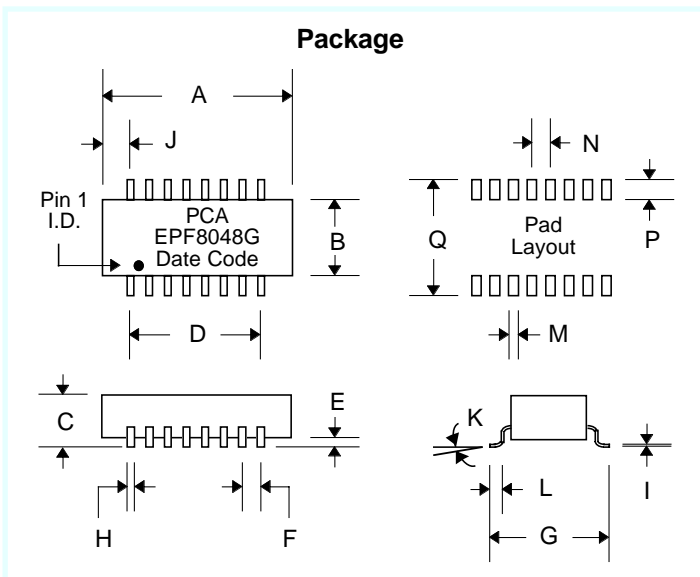
OCL @ 70°C 100 KHz, 0.1 Vrms 8 mA DC Bias	Insertion Loss (dB Max.)		Return Loss (dB Min.)						Common Mode Rejection (dB Min.)						Crosstalk (dB Min.) [Between Channels]
	1-100 MHz		1-60 MHz	60-80 MHz	80-100 MHz	30-100 MHz	100-200 MHz	200-500 MHz	10-100 MHz						
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	
350µH	-1	-1	-18	-18	-12	-12	-10	-10	-40	-40	-30	-30	-25	-25	-40

• Isolation : 1500 Vrms • Cable Impedance : 100 Ω • Rise Time : 3.0 nS Max. • \*Optional •

### Schematic



### Package



### Dimensions

Dim.	(Inches)			(Millimeters)		
	Min.	Max.	Nom.	Min.	Max.	Nom.
A	.970	.990		24.64	25.15	
B	.380	.400		9.65	10.16	
C	.223	.243		5.66	6.17	
D	.700	Typ.		17.78	Typ.	
E	.003	.020		0.076	.508	
F	.100	Typ.		2.54	Typ.	
G	.500	.520		12.7	13.20	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.090	Typ.		2.28	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.100			2.54
P			.092			2.34
Q			.560			14.22

## EPF8048G

The circuit below is a guideline for interconnecting PCA's EPF8048G with ML6692 or ML6694 chip applications. Further details can be obtained from the chip manufacturer application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 100 BX protocol. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chips supporting resistor to get at least 2.12V pk-pk across the transmit pins.

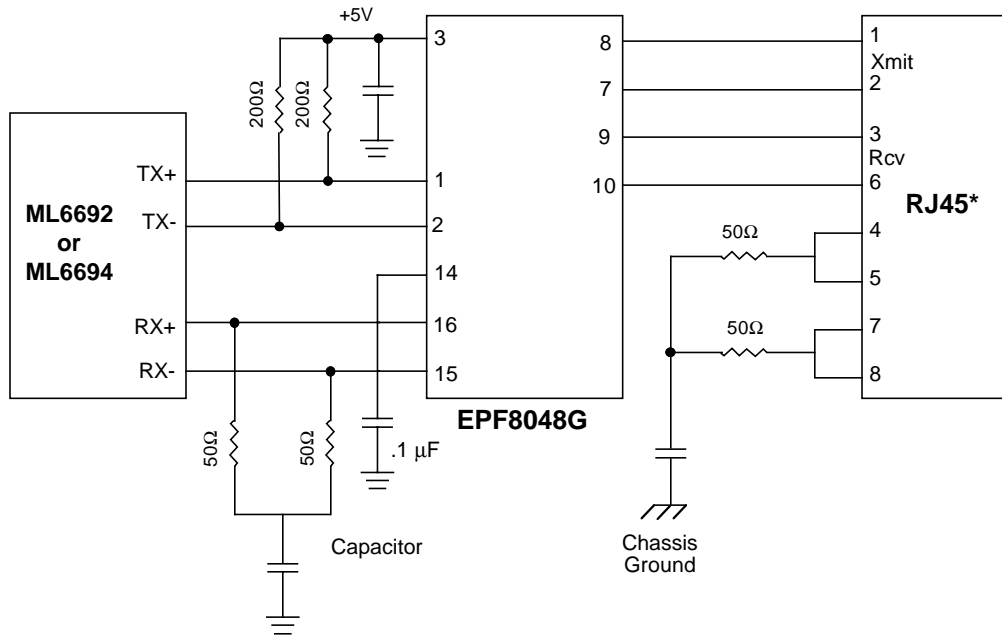
Note that in the 100 BX application, you do not need a split primary. The reason is that there is no 10 Base T to negotiate. The receiver side can be terminated as shown or by a single 100 ohms with primary center tap taken to ground via a suitable cap. Note that in the 100 BX application, you do not need a split primary. The reason is that there is no 10 Base-T to negotiate. The receiver side can be terminated as shown or by a single 100 ohms with primary center tap taken to ground via a suitable cap. **NOTE THAT THIS PART DOES NOT HAVE A TRANSMIT CHANNEL CENTER TAP ON THE CABLE SIDE.** Sufficient common mode attenuation is provided by the high performance common mode chokes on chip side as well as the cable side thus making this part easy to manufacture at reduced costs. A proper system board design may allow some users to benefit from this simplified structure of the transmit channel.

The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8048G. There need not be any ground plane beyond this plane.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

### Typical Application Circuit for UTP



Notes : \* NIC Side is shown. Hub side connection will swap pins 3-6 with 1-2.