TVS Diodes

Transient Voltage Suppressor Diodes

ESD3V3U4ULC

Ultra Low Capacitance ESD Array

ESD3V3U4ULC

Data Sheet

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Preliminary

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 0.9, 2010-10-14	

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Last Trademarks Update 2010-06-09

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1 Ultra Low Capacitance ESD Array

1.1 Features

- ESD / Transient protection of high speed data lines exceeding :
  - IEC61000-4-2 (ESD) : ±20 kV (air/contact)
  - IEC61000-4-4 (EFT) : 2.5 kV (5/50ns)
  - IEC61000-4-5 (Surge) : 3 A (8/20ns)
- Maximum working voltage: V_{RWM} = 3.3 V
- Very low reverse current: I_R = 1 nA (typical)
- Extremely low capacitance C_L = 0.4 pF I/O to GND (typical)
- Very low reverse clamping voltage: V_{CL}= 9 V at I_{PP} = 16 A (typical)
- Very low forward clamping voltage: V_{FC}= 6 V at I_{PP} = 16 A (typical)
- Very low reverse dynamic resistance: $R_{dyn,rev}$ = 0.2 Ω (typical)
- TSLP-9-1 package with pad pitch 0.5 mm
- Optimized pad design to simplify PCB layout
- Pb-free and Halogen-Free package (RoHS compliant)

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort, Mobile communication, LCD displays, Camera
- Consumer products (STB, MP3, DVD, DSC, ...) Notebooks and desktop computers, peripherals

2 Product Description

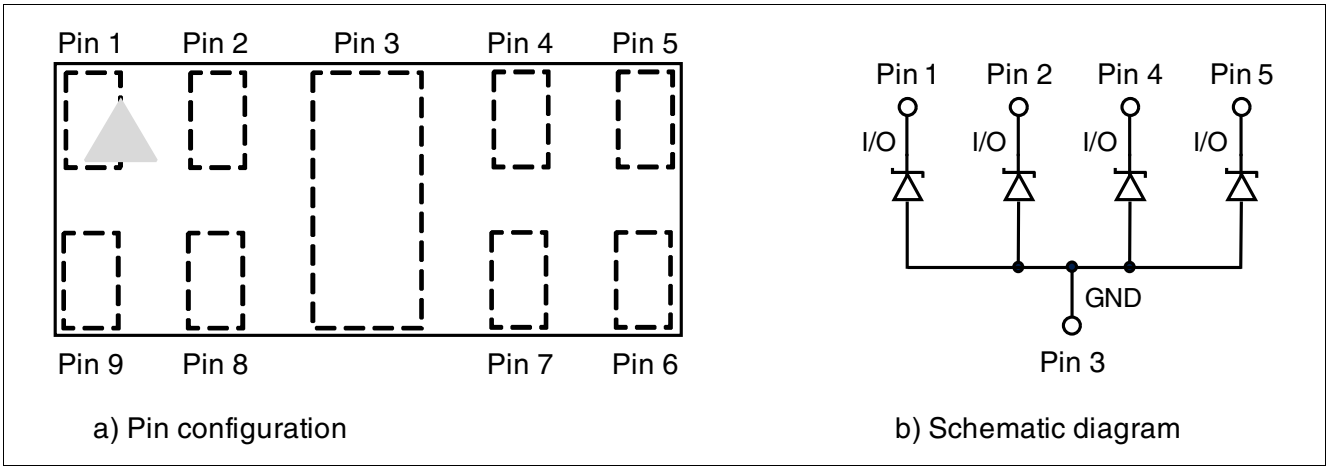

Figure 1 a) Pin Configuration and b) Schematic Diagram

Table 1 Ordering information

Type	Package	Configuration	Marking code
ESD3V3U4ULC	PG-TSLP-9-1	4 lines, uni-directional	Z2

3 Characteristics

Table 2 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1)]	V_{ESD}	-20	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	–	3	A
Operating temperature	T_{OP}	-40	–	125	°C
Storage temperage	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2
2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

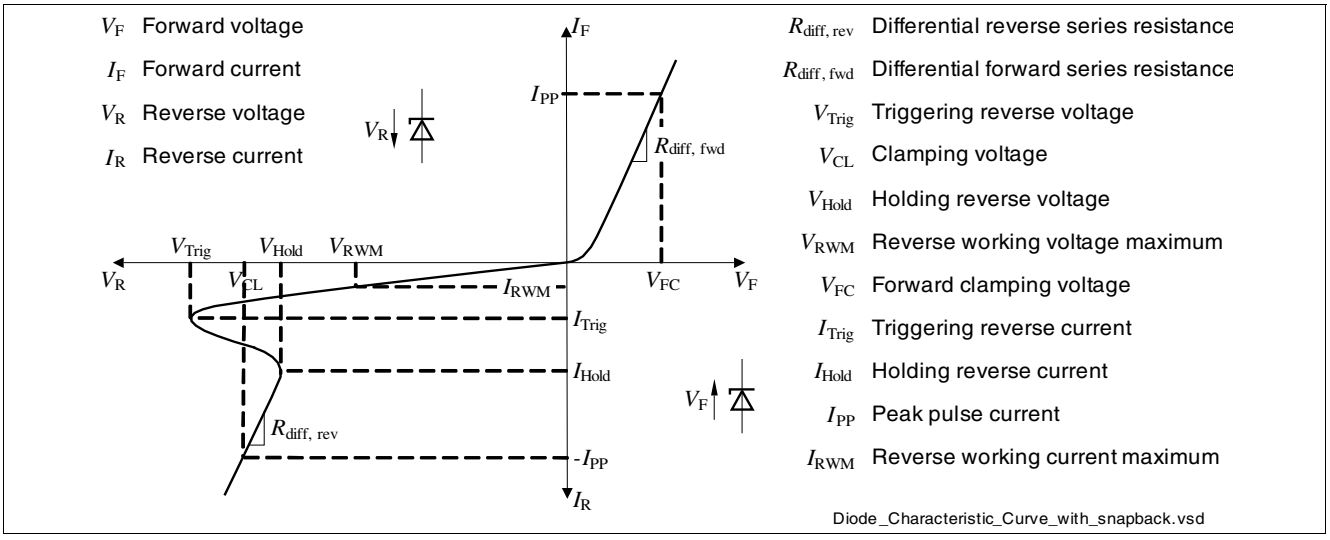

Figure 2 Definitions of electrical characteristics[1]

Table 3 DC characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	I/O to *GND*
Reverse current	I_R	–	1	50	nA	V_R = 3.3 V, I/O to *GND*

Table 4 RF characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.4	0.65	pF	V_R = 0 V, f = 1 MHz, I/O to GND
		–	0.2	0.35	pF	V_R = 0V, f = 1 MHz, I/O to I/O

Table 5 ESD characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse clamping voltage[1)] [2]	V_{CL}	–	9	–	V	I_{PP} = 16 A
		–	12	–	V	I_{PP} = 30 A
Forward clamping voltage[1)] [2]	V_{FC}	–	6	–	V	I_{PP} = 16 A
		–	10	–	V	I_{PP} = 30 A
Reverse dynamic resistance[1)] [2]	$R_{dyn, rev}$	–	0.2	–	Ω	
Forward dynamic resistance [1)][2]	$R_{dyn, fwd}$	–	0.25	–	Ω	

1) Please refer to Application Note AN210. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between I_{PP1} = 10 A and I_{PP2} = 40 A.

3.2 Typical Performance characteristics at T_A = 25 °C, unless otherwise specified

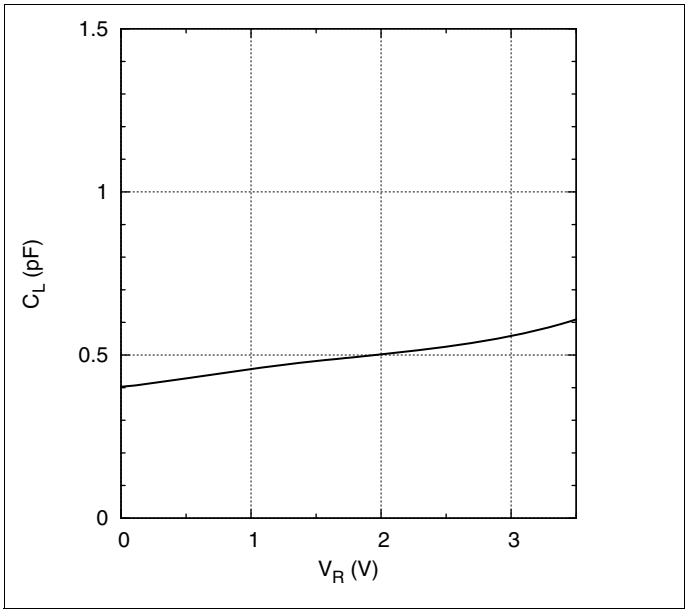

Figure 3 Line capacitance $C_L = f(V_R)$

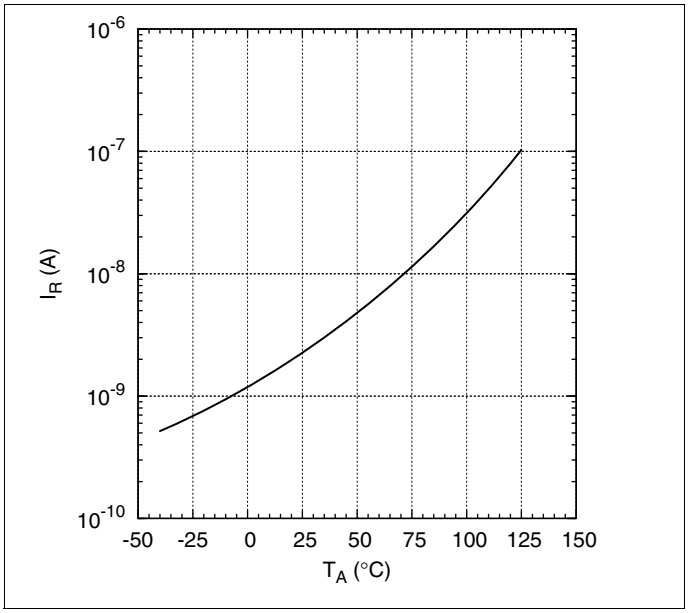

Figure 4 Reverse current $I_R = f(T_A)$, V_R = 3.3 V

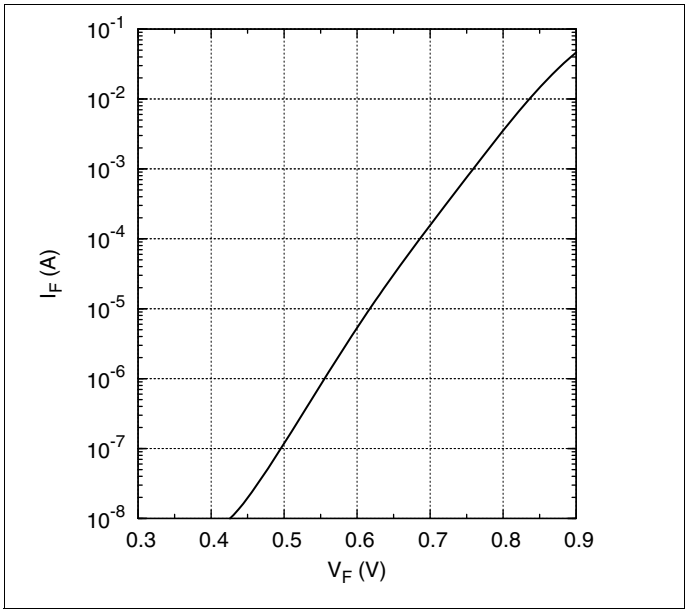

Figure 5 Forward characteristic, $I_F = f(V_F)$, current forced

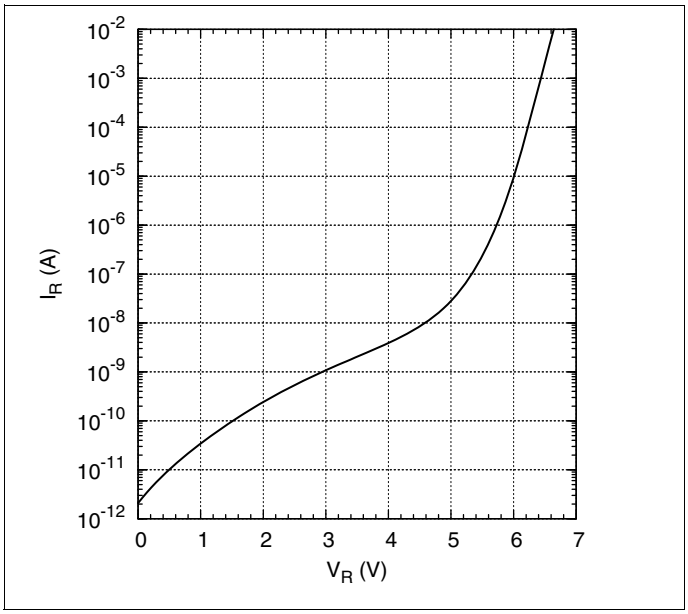

Figure 6 Reverse characteristic, $I_R = (V_R)$, voltage forced

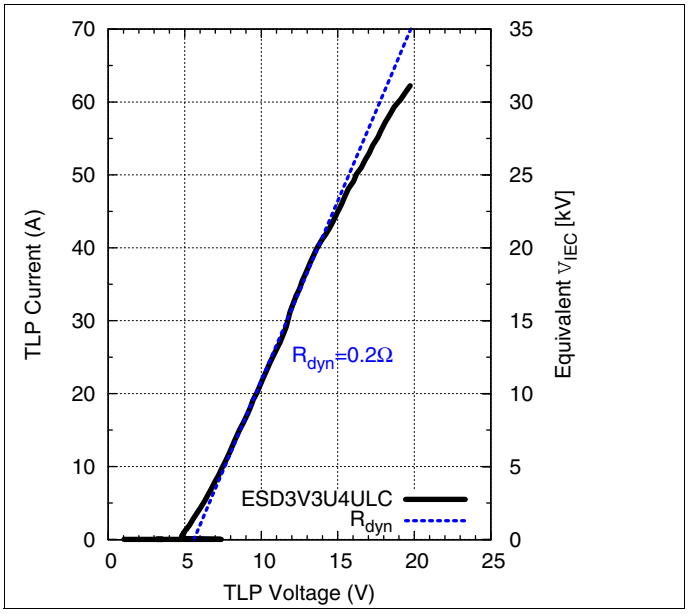

Figure 7 Reverse TLP characteristic[Note:] [2]

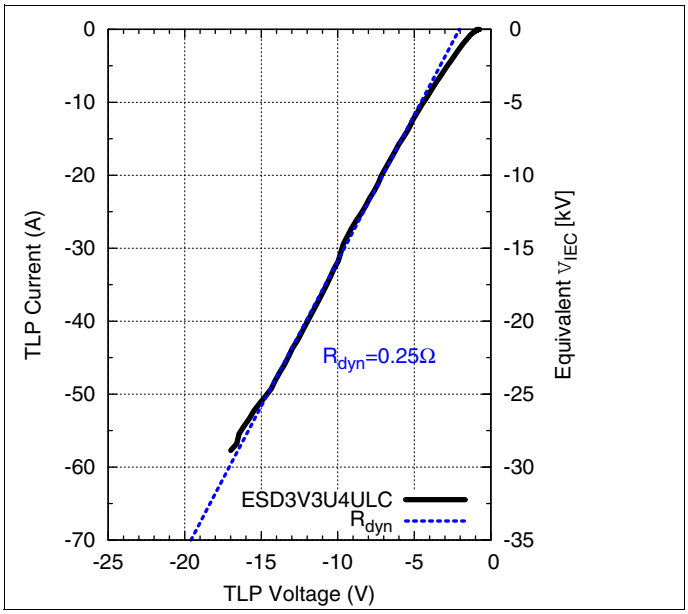

Figure 8 Forward TLP characteristic[Note:] [2]

Note: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between I_{PP1} = 10 A and I_{PP2} = 40 A. The equivalent stress level V_{IEC} according IEC 61000-4-2 (R = 330 Ω , C = 150 pF) is calculated at the broad peak of the IEC waveform at t = 30 ns with 2 A / kV

4 Application Information

To design USB3.0 link for best system level ESD performance and error free Signal Integrity is mandatory.

To bring both requirements together, the ESD protection devices has to provide excellent ESD and a very low device capacitance. The Infineon ESD3V3U4ULC in “array” configuration, combined with a clear and straight forward “full through” layout fulfills these requirements in the best way.

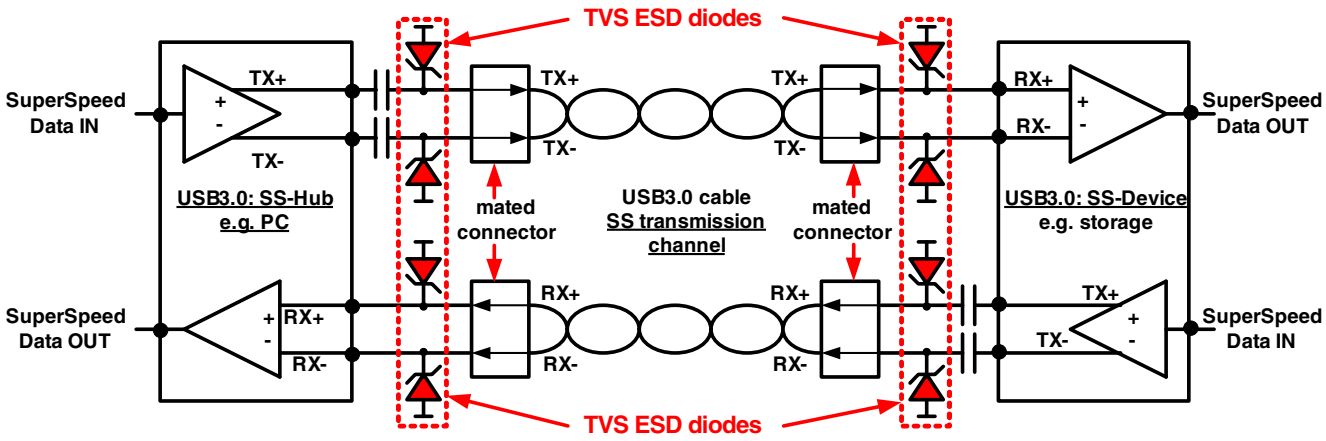

Figure 9 USB3.0 structure with ESD protection devices [3]

5 Ordering information scheme

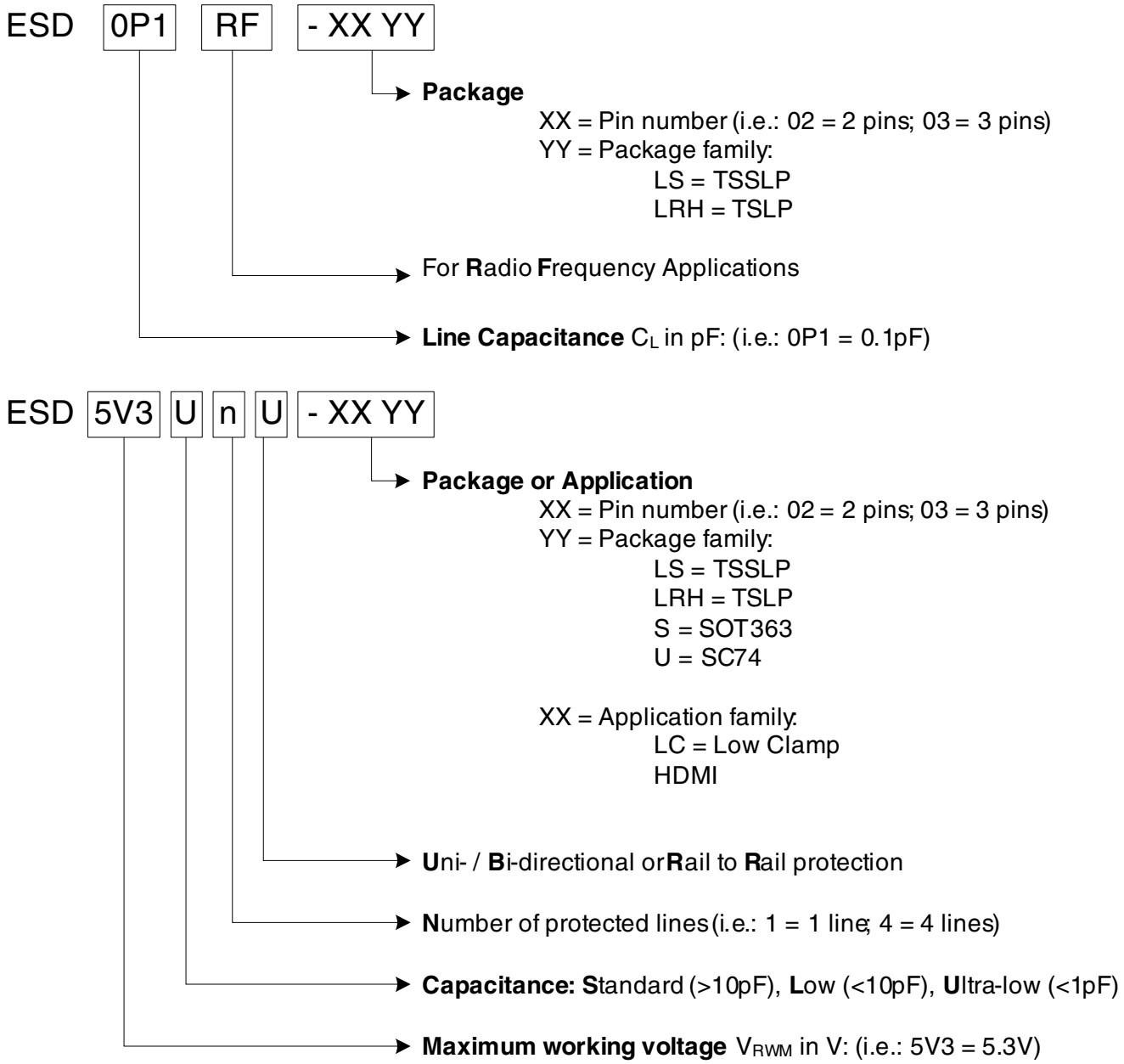

Figure 10 Ordering Information Scheme

6 Package Information

6.1 PG-TSLP-9-1

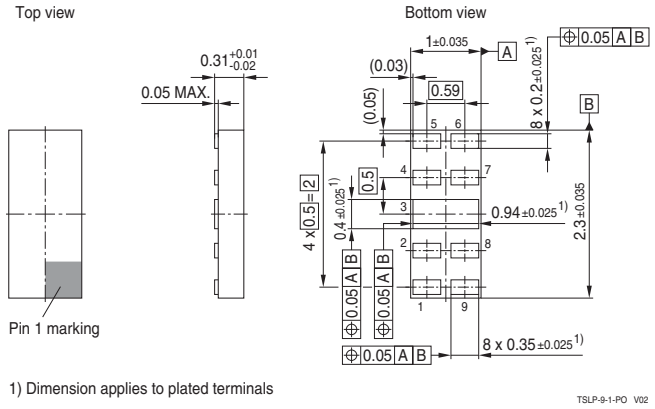

Figure 11 PG-TSLP-9-1: Package Overview

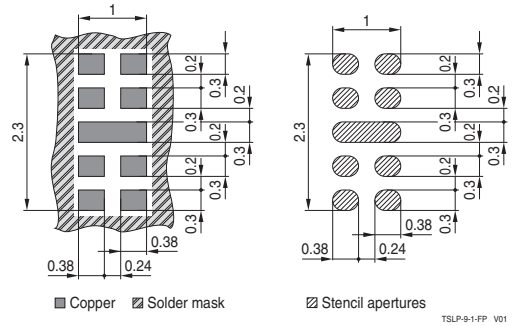

Figure 12 PG-TSLP-9-1: Footprint

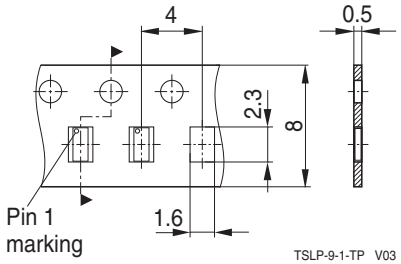

Figure 13 PG-TSLP-9-1: Packing

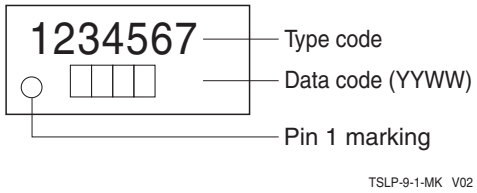

Figure 14 PG-TSLP-9-1: Marking

References

[1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Intergrity.

Terminology

C_L	Line capacitance
DSC	Digital Still Camera
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
HDMI	High Definition Multimedia Interface
IEC	International Electrotechnical Commission
I_{PP}	Peak pulse current
I_R	Reverse current
I_{RWM}	Reverse working current maximum
LCD	Liquid Crystal Display
MP3	Moving Picture Experts Group III
PCB	Printed Circuit Board
$R_{dyn, fwd}$	Forward dynamic resistance
$R_{dyn, rev}$	Reverse dynamic resistance
RoHS	Restriction of Hazardous Substances Directive
S-ATA	Serial Advanced Technology Attachment
STB	Set-Top-Box
T_A	Ambient temperature
TLP	Transmission Line Pulse
T_{OP}	Operation temperature
t_p	Pulse duration
t_r	Pulse rise time
T_{stg}	Storage temperature
USB	Universal Serial Bus
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_{FC}	Forward Clamping Voltage
V_{Hold}	Holding Voltage
V_{IEC}	Equivalent stress level according IEC61000-4-2 (R = 330 Ω , C = 150 pF)
V_R	Reverse voltage
V_{RWM}	Reverse working voltage maximum
V_{Trig}	Triggering Voltage
Z_0	Impedance

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