ESDA14V2-4BF2

ASD
(Application Specific Devices)

QUAD BIDIRECTIONAL TRANSIL™ ARRAY FOR ESD PROTECTION

APPLICATION

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.

DESCRIPTION

The ESDA14V2-4BF2 is a monolithic array designed to protect up to 4 lines in a bidirectional way against ESD transients.

The device is ideal for situations where board space saving is requested.

FEATURES

- 4 Bidirectional Transil functions
- ESD Protection: IEC61000-4-2 level 4
- Stand off voltage: 12 V Min.
- Low leakage current < 1 µA
- 50 W Peak pulse power (8/20 µs)

BENEFITS

- High ESD protection level
- High integration
- Suitable for high density boards

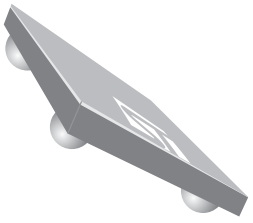
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

15 kV	(air discharge)
8 kV	(contact discharge)

MIL STD 883F- Method 3015-7: class3

25 kV	(human body model)



Flip-Chip
(5 Bumps)

Table 1: Order Code

Part Number	Marking
ESDA14V2-4BF2	EA

Figure 1: Pin Configuration (Bump side)

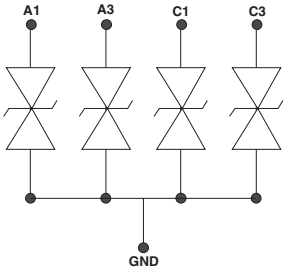
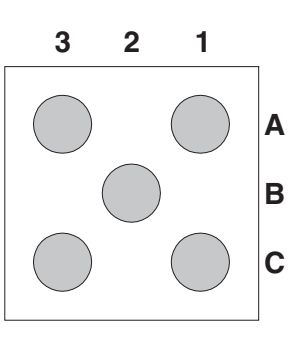


Figure 2: Pin Configuration (Bump Side)



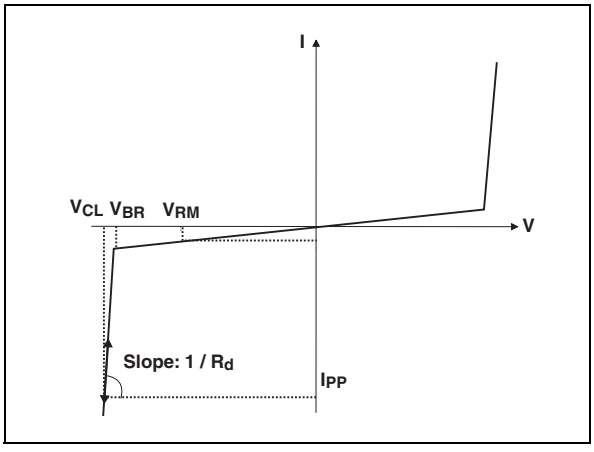
TM: TRANSIL is a trademark of STMicroelectronics.

Table 2: Absolute Ratings (limiting values)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge	MIL STD 883E - Method 3015-7 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	± 25 ± 15 ± 8	kV
P_{PP}	Peak pulse power (8/20 µs)		50	W
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C
T_{op}	Operating temperature range		-40 to +125	°C

Table 3: Electrical Characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
C	Capacitance



Part Number	V_{BR} min.	V_{BR} max.	@ I_R	I_{RM} max.	@ V_{RM}	R_d typ. note 1	αT max. note 2	C max. 0V bias
	V	V	mA	µA	V	Ω	10^{-4}/°C	pF
ESDA14V2-4BF2	14.2	18	1	1	12	3.2	10	15
				0.1	3			

Note 1: Square pulse, I_{PP} = 3A, tp = 2.5 µs.

Note 2: $\Delta V_{BR} = \alpha T$ (Tamb -25 °C) x V_{BR} (25 °C)

Figure 3: Clamping voltage versus peak pulse current (Tj initial = 25 °C) (Rectangular waveform, t_p = 2.5 µs)

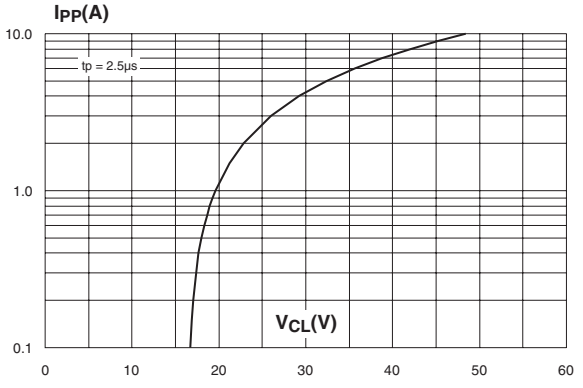


Figure 4: Capacitance versus reverse applied voltage (typical values)

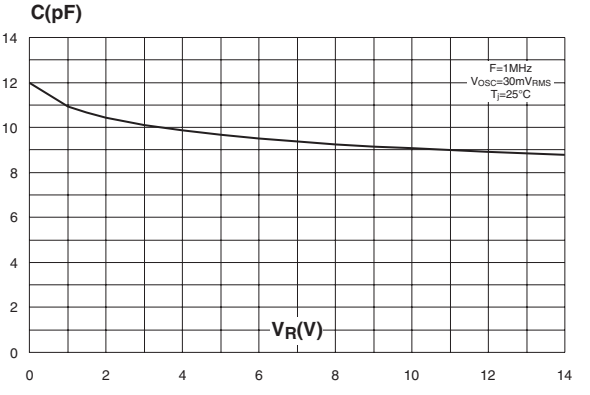


Figure 5: Relative variation of leakage current versus junction temperature (typical values)

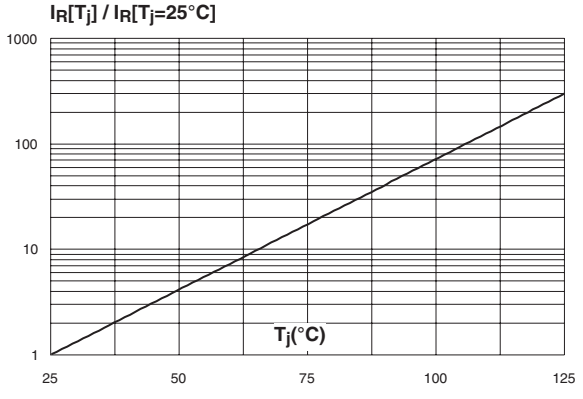


Figure 6: ESD response to IEC61000-4-2 (+15 kV air discharge)

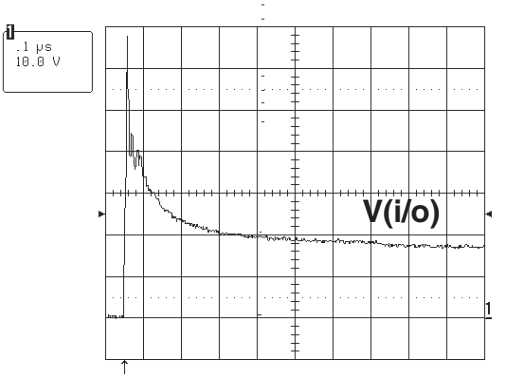


Figure 7: ESD response to IEC61000-4-2 (-15 kV air discharge)

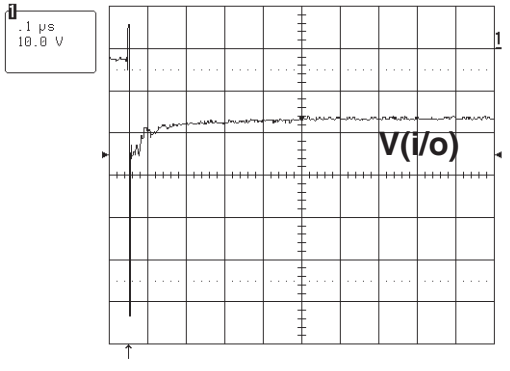


Figure 8: Analog crosstalk

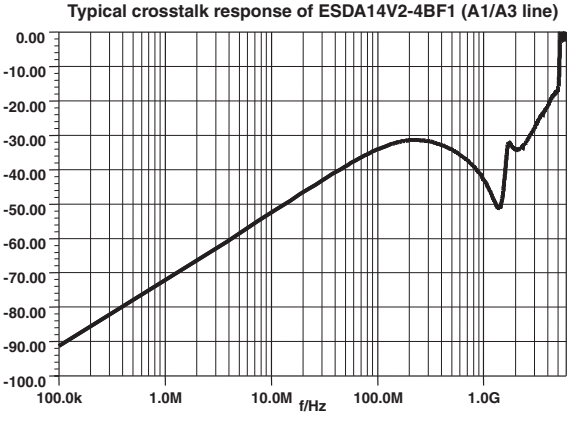


Figure 9: Digital crosstalk

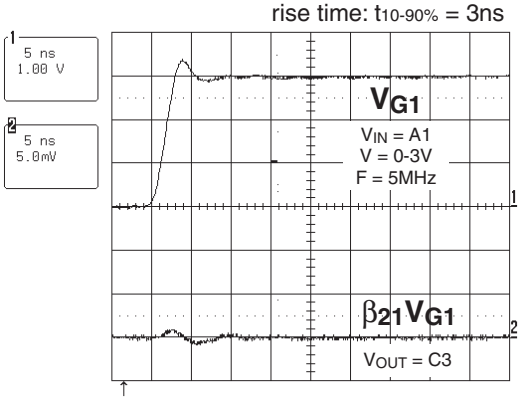


Figure 10: Application example

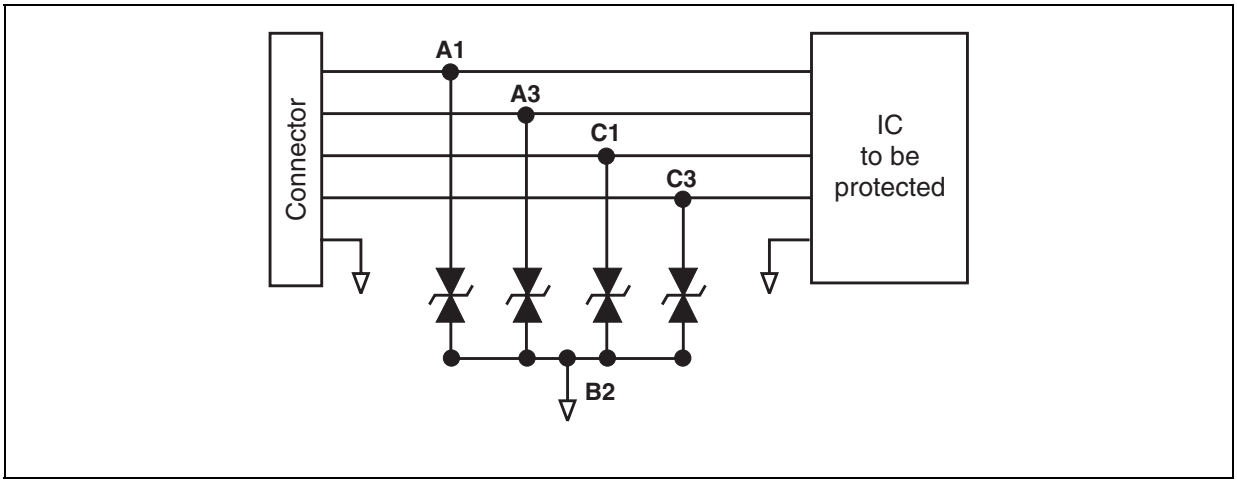


Figure 11: Aplac model

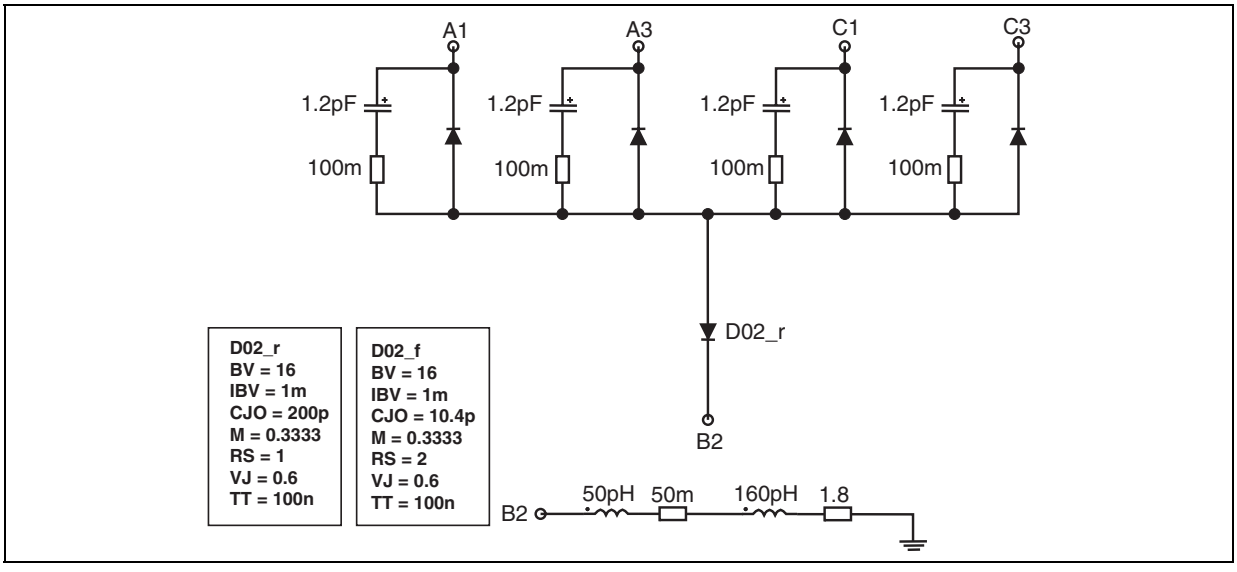


Figure 12: Ordering Information Scheme

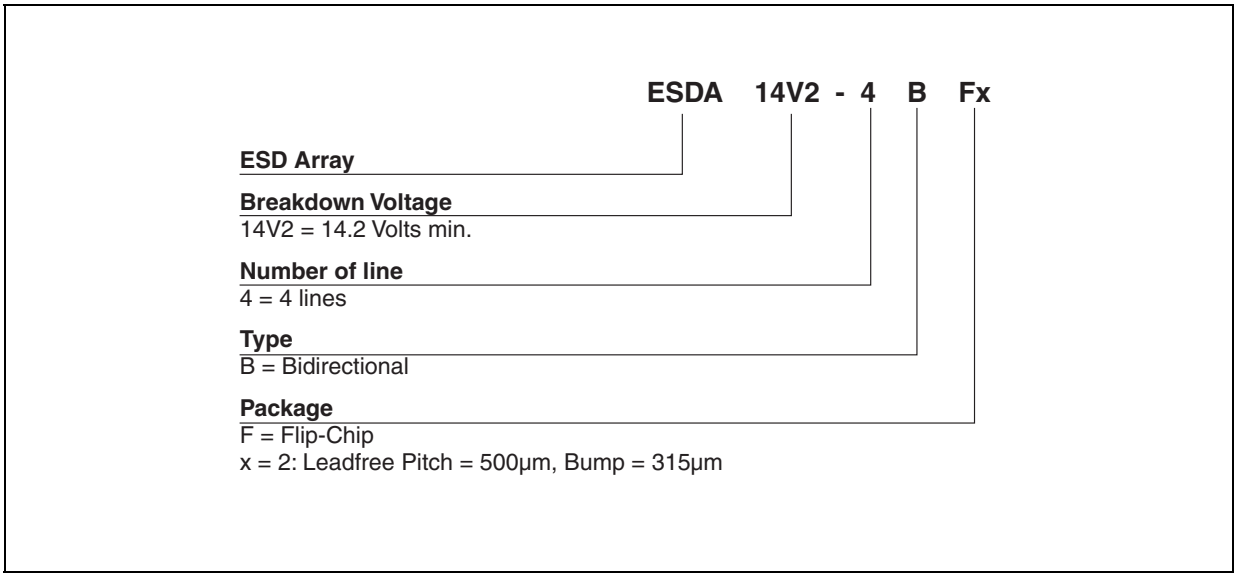


Figure 13: FLIP-CHIP Package Mechanical Data

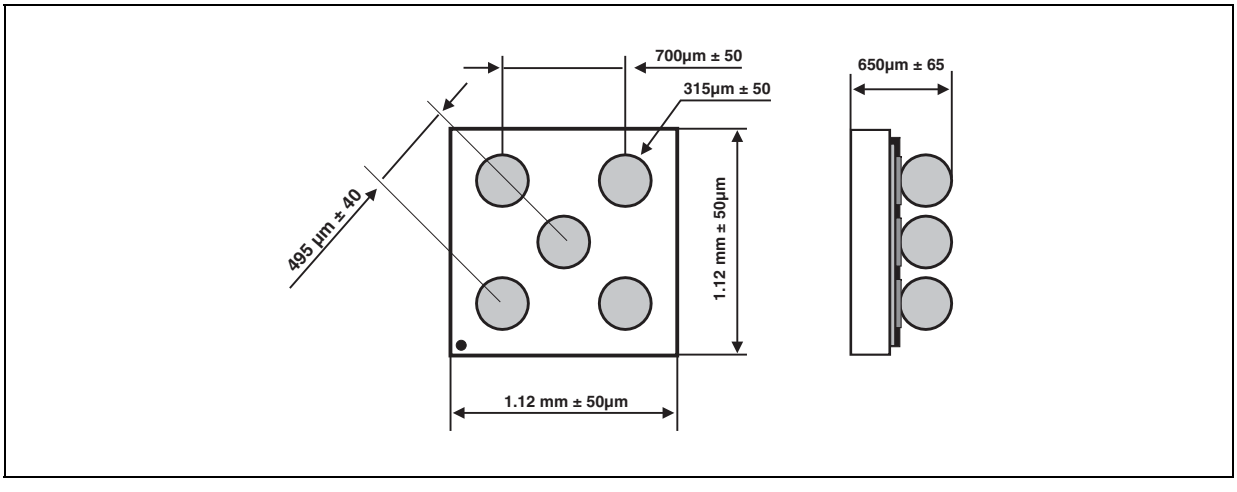


Figure 14: Foot print recommendations

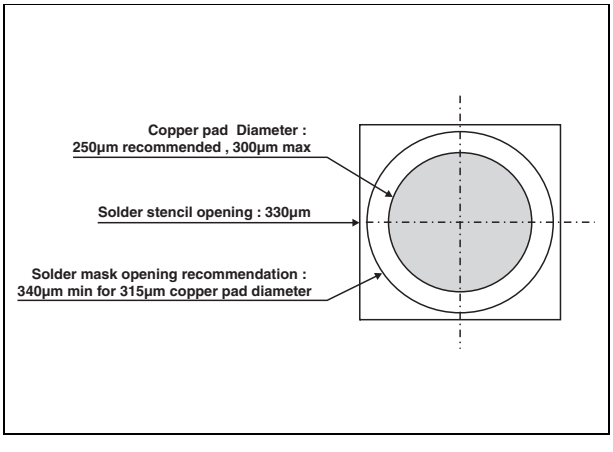


Figure 15: Marking

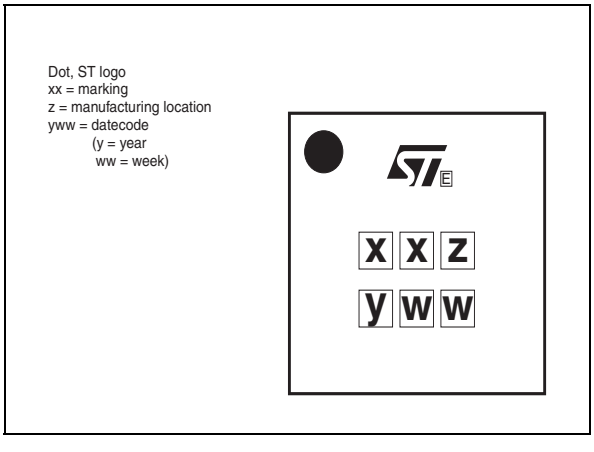
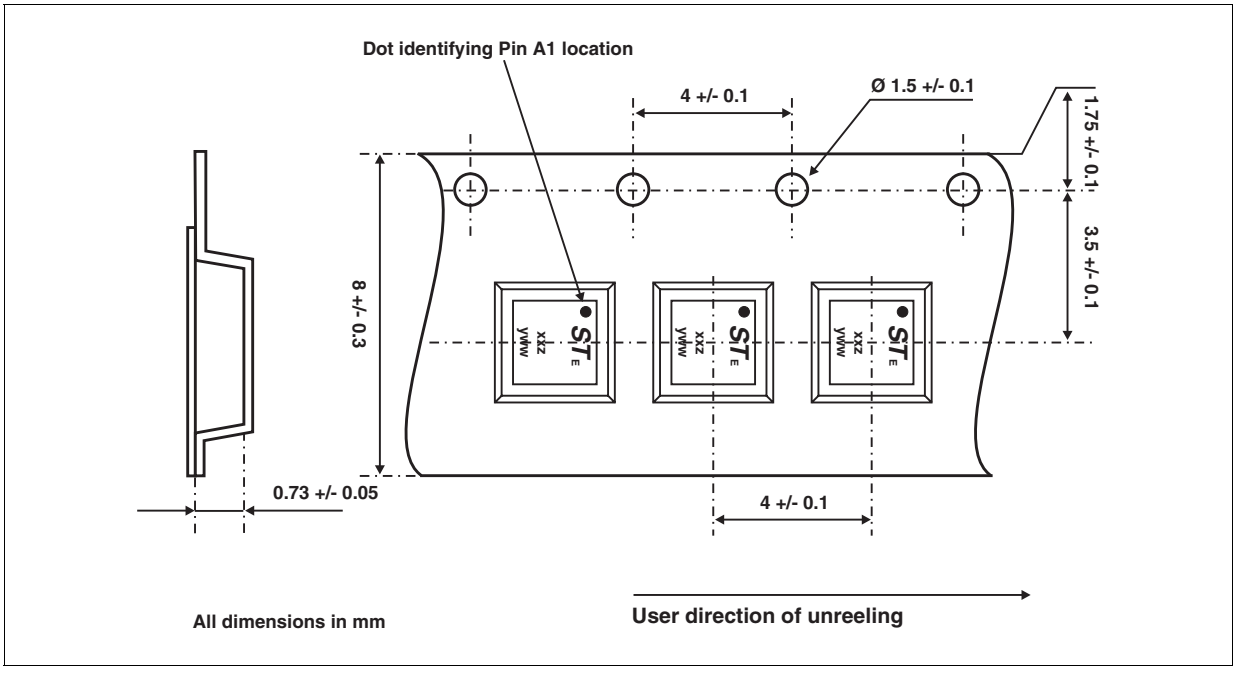


Figure 16: FLIP-CHIP Tape and Reel Specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-4BF2	EA	Flip-Chip	2.1 mg	5000	Tape & reel 7”

Note: More informations are available in the application notes:
AN1235: “Flip-Chip: Package description and recommendations for use”

Table 5: Revision History

Date	Revision	Description of Changes
14-Mar-2005	1	First issue.
18-Oct-2005	2	Dimension from center bump to corner bump changed in Figure 13 to indicate diagonal instead of perpendicular measurement. No values changed. ECOPACK statement added.
17-Jan-2006	3	Die dimensions changed in Figure 13. Cavity depth changed in Figure 16

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