ESDALY

Automotive dual Transil™ array for ESD protection

Features

- Dual unidirectional Transil functions
- Low leakage current: I_R max. < 20 µA at V_{BR}
- 300 W peak pulse power (8/20 µs)

Benefits

- High ESD protection level: up to 25 kV
- High integration
- Suitable for high density boards
- AEC-Q101 qualified

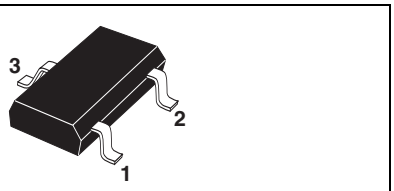
Complies with the following standards

- ISO 10605: C = 150 pF, R = 330 Ω
  - 30 kV (air discharge)
  - 30 kV (contact discharge)
- ISO 10605: C = 330 pF, R = 330 Ω
  - 30 kV (air discharge)
  - 30 kV (contact discharge)
- ISO 7637-2[(a)]
  - Pulse 1: V_S = -100 V
  - Pulse 2a: V_S = +50 V
  - Pulse 3a: V_S = -150 V
  - Pulse 3b: V_S = +100 V

Applications

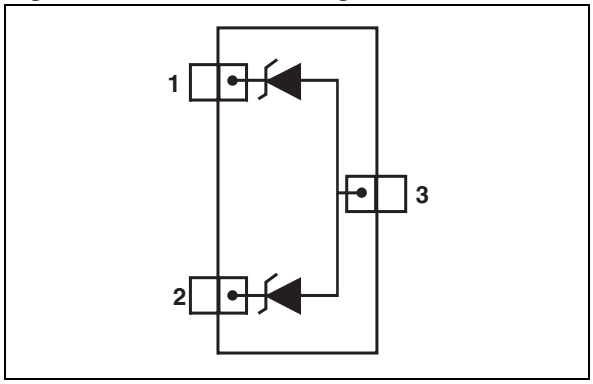
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Entertainment
- Signal communications
- Connectivity
- Comfort and convenience



SOT23-3L

Figure 1. Functional diagram



Description

The ESDALY is a monolithic array designed to protect 1 line or 2 lines against ESD transients. The device is ideal for applications where both reduced line capacitance and board space saving are required. It can also be used as bidirectional suppressor by connecting only pin 1 and 2.

a. Not applicable to parts with stand-off voltage lower than the average battery voltage (13.5 V)

TM: Transil is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage(1)	ISO 10605 (C = 330 pF, R = 330 Ω): contact discharge air discharge ISO 10605: C = 150 pF, R = 330 Ω contact discharge air discharge	 30 30 30 30	kV
P_{PP}	Peak pulse power (8/20µs)		300	W
I_{PP}	Peak pulse current (8/20µs)	ESDA5V3LY ESDA6V1LY ESDA14V2LY ESDA25LY	25 18 14 7	A
T_j	Operating junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm from case		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
I_{PP}	=	Forward current
R_d	=	Dynamic resistance
αT	=	Voltage temperature coefficient
C_{line}	=	Line capacitance

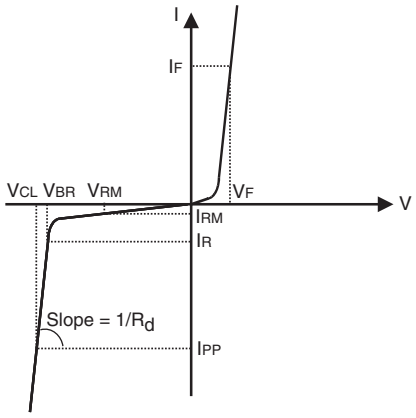


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Order code	V_{BR} @ I_R			I_{RM} @ V_{RM}		V_{CL}@I_{PP}(1)		V_F@ I_F		R_d(2)	αT(3)	C_{line}
	Min.	Max.		Max.		Max.		Max.		Typ.	Max.	Typ.
	V	V	mA	µA	V	V	A	V	mA	mΩ	10^{-4}/°C	pF
ESDA5V3LY	5.3	5.9	1	2	3	19	25	1.25	200	280	5	220
ESDA6V1LY	6.1	7.2	1	20	5.2	16	18	1.25	200	350	6	140
ESDA14V2LY	14.2	15.8	1	5	12	21	14	1.25	200	650	10	90
ESDA25LY	25	30	1	1	24	43	7	1.2	10	1000	10	50

1. 8/20 µs waveform
2. Square pulse, I_{pp} = 15 A, t_p= 2.5 µs.
3. $\Delta V_{BR} = \alpha T^* (T_{amb} - 25\ °C) * V_{BR}$ (25 °C)

Figure 3. Variation of peak pulse power versus initial junction temperature

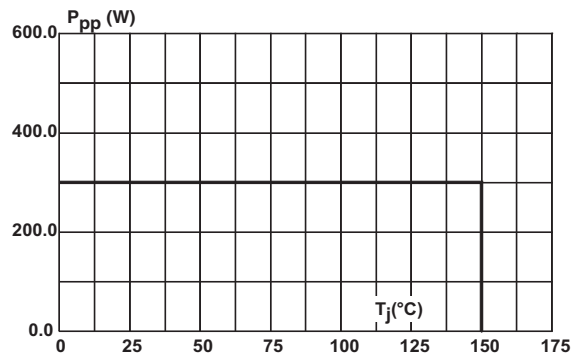


Figure 4. Peak pulse power versus exponential pulse duration (typical values)

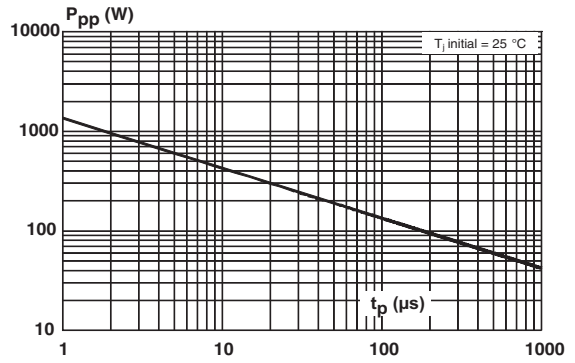


Figure 5. Variation of clamping voltage versus peak pulse current (max. values, 8/20 µs waveform)

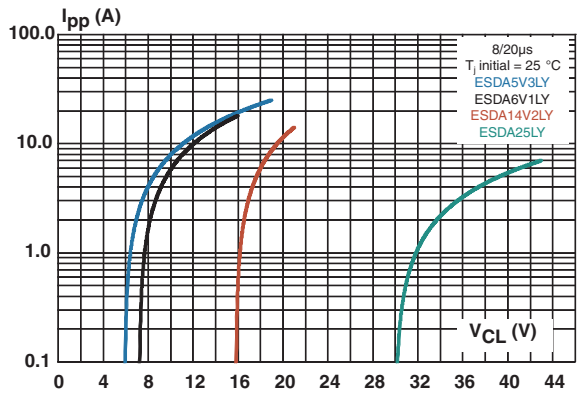


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

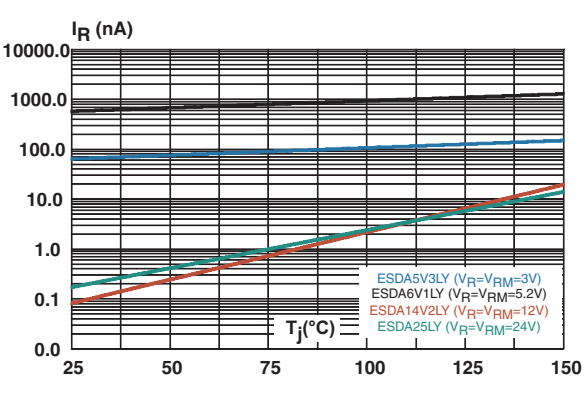


Figure 7. ISO 7637-2 pulse 1 response (V_S = -100 V)

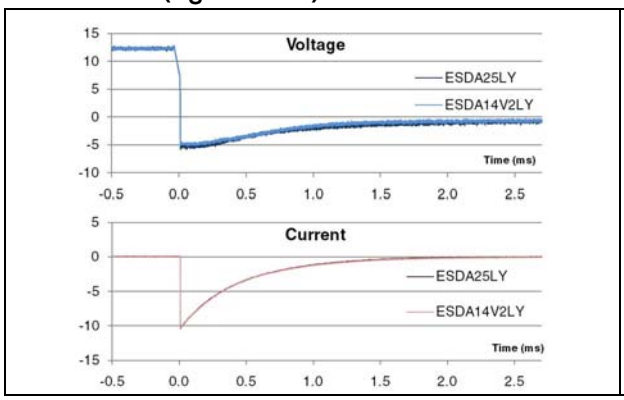


Figure 8. ISO 7637-2 pulse 2a response (V_S = 50 V)

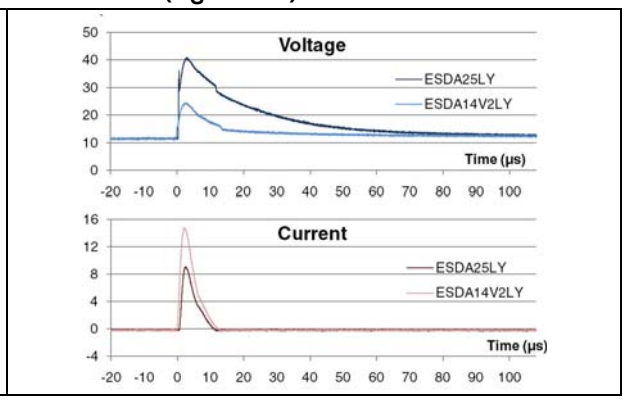


Figure 9. ISO 7637-2 pulse 3a response (V_S = -150 V)

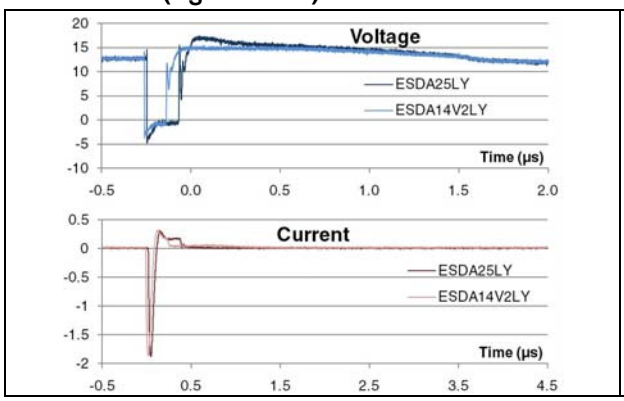
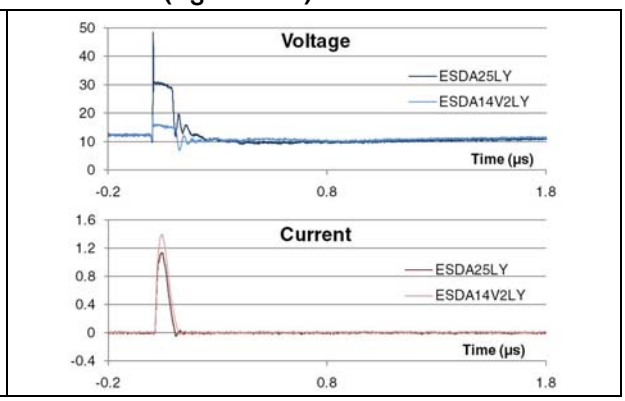


Figure 10. ISO 7637-2 pulse 3b response (V_S = 100 V)



Note: ISO7637-2 pulse responses are not applicable for products with a breakdown voltage lower than the average battery voltage (13.5 V) like ESDA5V3LY and ESDA6V1LY.

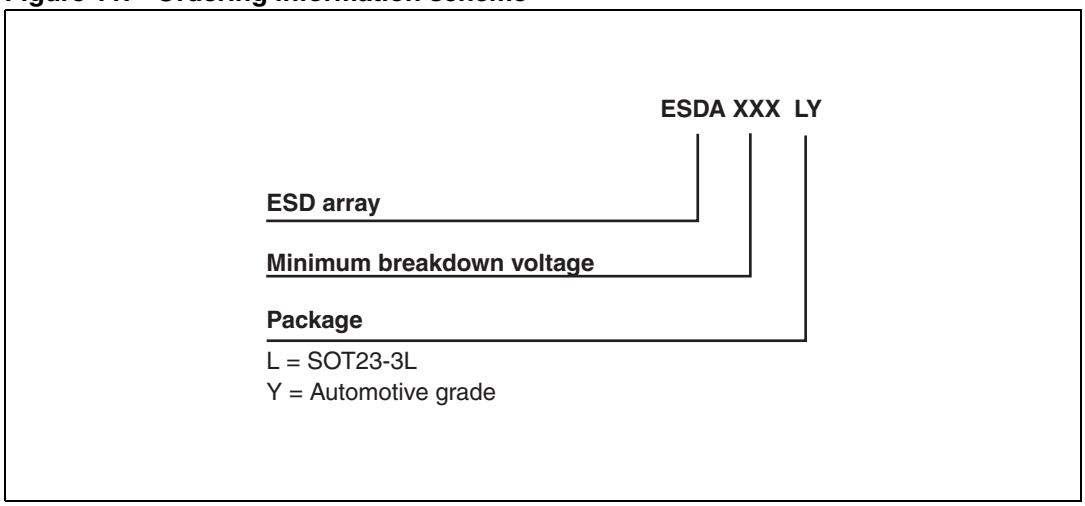
2 Application and design guidelines

More information is available in the application note:

AN2689, “Protection of automotive electronics from electrical hazards, guidelines for design and component selection”.

3 Ordering information scheme

Figure 11. Ordering information scheme

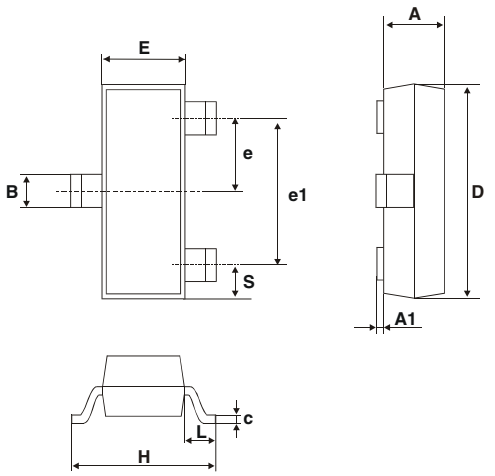


4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. SOT23-3L dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.89	1.4	0.035	0.055
A1	0	0.1	0	0.004
B	0.3	0.51	0.012	0.02
c	0.085	0.18	0.003	0.007
D	2.75	3.04	0.108	0.12
e	0.85	1.05	0.033	0.041
e1	1.7	2.1	0.067	0.083
E	1.2	1.6	0.047	0.063
H	2.1	2.75	0.083	0.108
L	0.6 typ.		0.024 typ.	
S	0.35	0.65	0.014	0.026

Figure 12. Footprint (dimensions in mm)

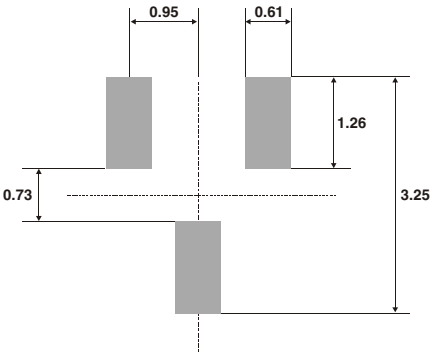
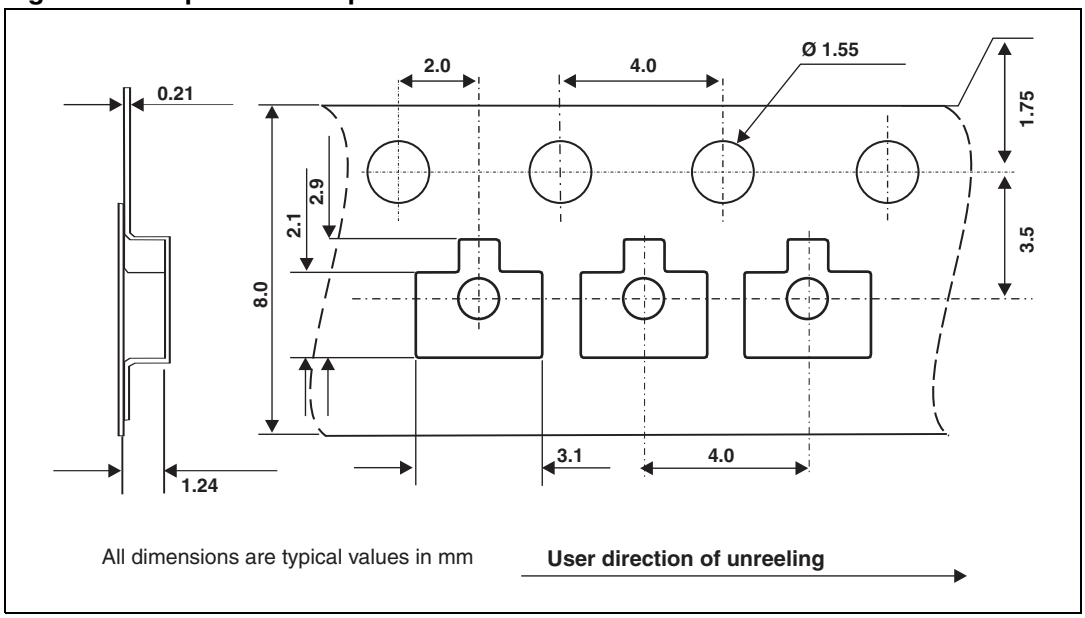


Figure 13. Tape and reel specifications



5 Recommendation on PCB assembly

5.1 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

5.2 Placement

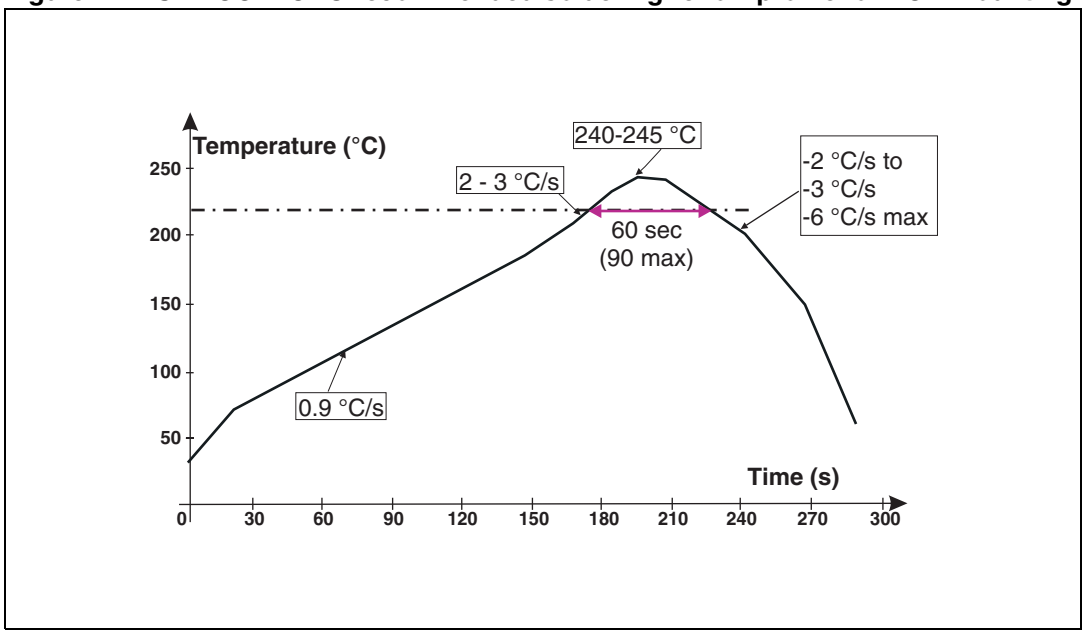
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.4 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Order code	Marking[1]	Package	Weight	Base qty	Delivery mode
ESDA5V3LY	EL5Y	SOT23-3L	8.7 mg	3000	Tape and reel
ESDA6V1LY	EL6Y				
ESDA14V2LY	EL1Y				
ESDA25LY	EL2Y				

1. The marking can be rotated by multiples of 90° to differentiate assembly location

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
16-Feb-2012	1	Initial version. This document merges and updates the content of the datasheet ESDA25LY Revision 1, 01-Feb-2010.

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