

Flash

3V Only 4 Mbit Serial Flash Memory

■ FEATURES

- Single supply voltage 2.7~3.6V
- Speed
 - Read max frequency : 33MHz
 - Fast Read max frequency : 50MHz; 75MHz; 100MHz
- Low power consumption
 - Active current :40mA
 - Standby current : 25 μ A
- Reliability
 - 100,000 program/erase cycles typically
 - 10 years Data Retention
- Program
 - Byte program time 8 μ s(typical)
- Erase
 - Chip erase time 11s(typical)
 - Sector erase time 0.7s(typical)
- Auto Address Increment (AAI) Programming
 - Decrease total chip programming time over Byte-Program operations
- SPI Serial Interface
 - SPI Compatible : Mode 0 and Mode3
- End of program or erase detection
- Write Protect (\overline{WP})
- Hold Pin (\overline{HOLD})
- Package available
 - 8-pin SOIC 150-mil

ORDERING INFORMATION

| Part No. | Speed | Package | COMMENTS |
|-----------------|--------|-------------|----------|
| F25L04UA -50PG | 50MHz | 8 lead SOIC | Pb-free |
| F25L04UA -75PG | 75MHz | 8 lead SOIC | Pb-free |
| F25L04UA -100PG | 100MHz | 8 lead SOIC | Pb-free |

GENERAL DESCRIPTION

The F25L04UA is a 4Megabit, 3V only CMOS Serial Flash memory device. ESMT's memory devices reliably store memory data even after 100,000 program and erase cycles.

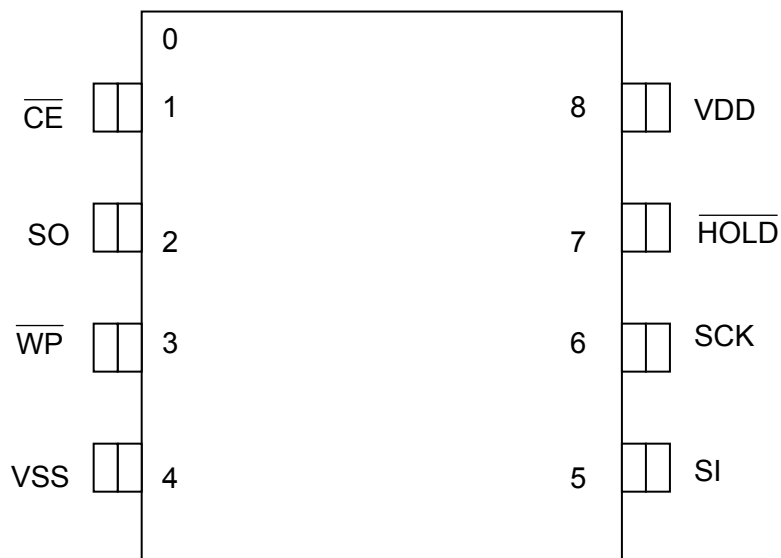
The F25L04UA features a sector erase architecture. The device memory array is divided into one 8K bytes, two 4K bytes, one 16K bytes, one 32K bytes, and seven 64K bytes. Sectors can be

erased individually without affecting the data in other sectors. Whole chip erase capabilities provide the flexibility to revise the data in the device.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

PIN CONFIGURATIONS

8-PIN SOIC



PIN Description

| Symbol | Pin Name | Functions |
|-------------------|--------------------|---|
| SCK | Serial Clock | To provide the timing for serial input and output operations |
| SI | Serial Data Input | To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK. |
| SO | Serial Data Output | To transfer data serially out of the device. Data is shifted out on the falling edge of SCK. |
| \overline{CE} | Chip Enable | To activate the device when \overline{CE} is low. |
| \overline{WP} | Write Protect | The Write Protect (\overline{WP}) pin is used to enable/disable BPL bit in the status register. |
| \overline{HOLD} | Hold | To temporarily stop serial communication with SPI flash memory without resetting the device. |
| VDD | Power Supply | To provide power. |
| VSS | Ground | |

SECTOR STRUCTURE

Table1 : F25L04UA Sector Address Table

| Symbol | Sector Size (Kbytes) | Address range | Sector Address | | | | | | |
|--------|----------------------|-----------------|----------------|-----|-----|-----|-----|-----|-----|
| | | | A18 | A17 | A16 | A15 | A14 | A13 | A12 |
| 11 | 8KB | 7E000H – 7FFFFH | 1 | 1 | 1 | 1 | 1 | 1 | X |
| 10 | 4KB | 7D000H – 7DFFFH | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 9 | 4KB | 7C000H – 7CFFFH | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 8 | 16KB | 78000H – 7BFFFH | 1 | 1 | 1 | 1 | 0 | X | X |
| 7 | 32KB | 70000H – 77FFFH | 1 | 1 | 1 | 0 | X | X | X |
| 6 | 64KB | 60000H – 6FFFFH | 1 | 1 | 0 | X | X | X | X |
| 5 | 64KB | 50000H – 5FFFFH | 1 | 0 | 1 | X | X | X | X |
| 4 | 64KB | 40000H – 4FFFFH | 1 | 0 | 0 | X | X | X | X |
| 3 | 64KB | 30000H – 3FFFFH | 0 | 1 | 1 | X | X | X | X |
| 2 | 64KB | 20000H – 2FFFFH | 0 | 1 | 0 | X | X | X | X |
| 1 | 64KB | 10000H – 1FFFFH | 0 | 0 | 1 | X | X | X | X |
| 0 | 64KB | 00000H – 0FFFFH | 0 | 0 | 0 | X | X | X | X |

Table2 : F25L04UA Block Protection Table

| Protection Level | BP1 | BP0 | Protected Memory Area |
|---------------------|-----|-----|-----------------------|
| 0 | 0 | 0 | None |
| 1(1/8 memory array) | 0 | 1 | 70000H – 7FFFFH |
| 2(1/4 memory array) | 1 | 0 | 60000H – 7FFFFH |
| 3(all memory array) | 1 | 1 | 00000H – 7FFFFH |

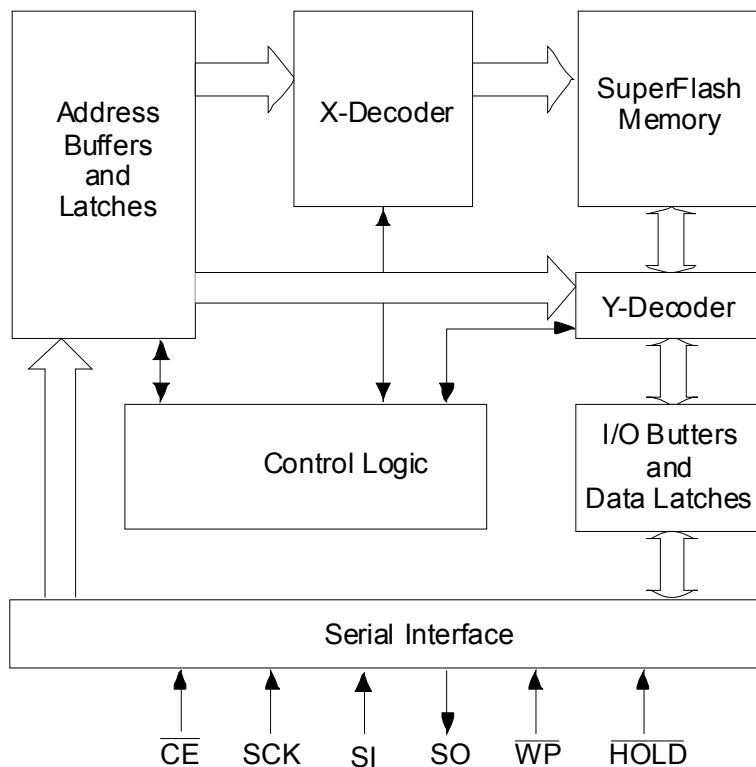
Block Protection (BP1, BP0)

The Block-Protection (BP1, BP0) bits define the size of the memory area, as defined in Table2 to be software protected against any memory Write (Program or Erase) operations. The Write-Status-Register (WRSR) instruction is used to program the BP1 and BP0 bits as long as \overline{WP} is high or the Block-Protection-Lock (BPL) bit is 0. Chip-Erase can only be executed if Block-Protection bits are both 0. After power-up, BP1 and BP0 are set to 1.

Block Protection Lock-Down (BPL)

\overline{WP} pin driven low (V_{IL}), enables the Block-Protection -Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP1, and BP0 bits. When the \overline{WP} pin is driven high (V_{IH}), the BPL bit has no effect and its value is "Don't Care". After power-up, the BPL bit is reset to 0.

FUNTIONAL BLOCK DIAGRAM



Hold Operation

$\overline{\text{HOLD}}$ pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the $\overline{\text{HOLD}}$ mode, $\overline{\text{CE}}$ must be in active low state. The $\overline{\text{HOLD}}$ mode begins when the SCK active low state coincides with the falling edge of the $\overline{\text{HOLD}}$ signal. The HOLD mode ends when the $\overline{\text{HOLD}}$ signal's rising edge coincides with the SCK active low state.

If the falling edge of the $\overline{\text{HOLD}}$ signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state.

Similarly, if the rising edge of the $\overline{\text{HOLD}}$ signal does not

coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 3 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH} .

If $\overline{\text{CE}}$ is driven active high during a Hold condition, it resets the internal logic of the device. As long as $\overline{\text{HOLD}}$ signal is low, the memory remains in the Hold condition. To resume communication with the device, $\overline{\text{HOLD}}$ must be driven active high, and $\overline{\text{CE}}$ must be driven active low. See Figure 17 for Hold timing.

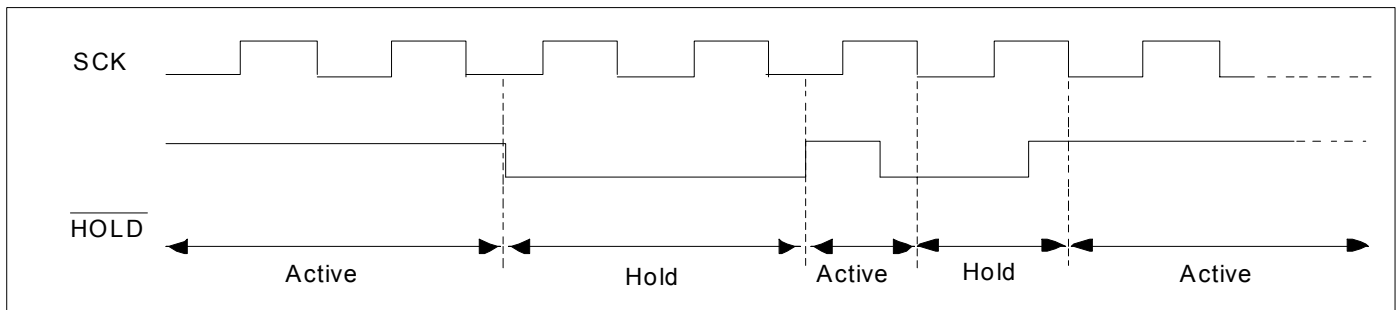


Figure 3 : HOLD CONDITION WAVEFORM

Write Protection

F25L04UA provides software Write protection.

The Write Protect pin ($\overline{\text{WP}}$) enables or disables the lockdown function of the status register. The Block-Protection bits (BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 2 for Block-Protection description.

Write Protect Pin ($\overline{\text{WP}}$)

The Write Protect ($\overline{\text{WP}}$) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When $\overline{\text{WP}}$ is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 3). When $\overline{\text{WP}}$ is high, the lock-down function of the BPL bit is disabled.

TABLE3: CONDITIONS TO EXECUTE WRITE-STATUS- REGISTER (WRSR) INSTRUCTION

| $\overline{\text{WP}}$ | BPL | Execute WRSR Instruction |
|------------------------|-----|--------------------------|
| L | 1 | Not Allowed |
| L | 0 | Allowed |
| H | X | Allowed |

Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation,

the status register may be read only to determine the completion of an operation in progress.

Table 4 describes the function of each bit in the software status register.

TABLE 4: SOFTWARE STATUS REGISTER

| Bit | Name | Function | Default at Power-up | Read/Write |
|-----|------|--|---------------------|------------|
| 0 | BUSY | 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress | 0 | R |
| 1 | WEL | 1 = Device is memory Write enabled 0 = Device is not memory Write enabled | 0 | R |
| 2 | BP0 | Indicate current level of block write protection (See Table 2) | 1 | R/W |
| 3 | BP1 | Indicate current level of block write protection (See Table 2) | 1 | R/W |
| 4:5 | RES | Reserved for future use | 0 | N/A |
| 6 | AAI | Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode | 0 | R |
| 7 | BPL | 1 = BP1, BP0 are read-only bits 0 = BP1, BP0 are read/writable | 0 | R/W |

Note1 : Only BP0,BP1 and BPL are writable

Note2 : All register bits are volatility

Note3 : All area are protected at power-on (BP1=1,BP0=1)

Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. A "1" for the Busy bit indicates the device is busy with an operation in progress. A "0" indicates the device is ready for the next valid operation.

Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If the Write-Enable-Latch bit is set to "1", it indicates the device is Write enabled. If the bit is set to "0" (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Byte-Program instruction completion
- Auto Address Increment (AAI) programming reached its highest memory address
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion

Instructions

Instructions are used to Read, Write (Erase and Program), and configure the F25L04UA. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Byte-Program, Auto Address Increment (AAI) programming, Sector-Erase, Block-Erase, or Chip-Erase instructions, the Write-Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of \overline{CE} . Inputs will be accepted on the rising edge of

SCK starting with the most significant bit. \overline{CE} must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID and Read-Status-Register instructions). Any low to high transition on \overline{CE} , before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

TABLE 5: DEVICE OPERATION INSTRUCTIONS

| Cycle Type/ Operation ^{1,2} | Max Freq MHz | Bus Cycle ⁴ | | | | | | | | | | | |
|--|--------------------|------------------------|------------------|----------------------------------|------------------|---------------------------------|-------------------|--------------------------------|-------------------|-----------------|-------------------|-----------------|------------------|
| | | 1 | | 2 | | 3 | | 4 | | 5 | | 6 | |
| | | S _{IN} | S _{OUT} | S _{IN} | S _{OUT} | S _{IN} | S _{OUT} | S _{IN} | S _{OUT} | S _{IN} | S _{OUT} | S _{IN} | S _{OUT} |
| Read | 33 | 03H | Hi-Z | A ₂₃ -A ₁₆ | Hi-Z | A ₁₅ -A ₈ | Hi-Z | A ₇ -A ₀ | Hi-Z | X | D _{OUT} | | |
| High-Speed-Read | | 0BH | Hi-Z | A ₂₃ -A ₁₆ | Hi-Z | A ₁₅ -A ₈ | Hi-Z | A ₇ -A ₀ | Hi-Z | X | X | X | D _{OUT} |
| Sector-Erase ^{4,5} | | 20H | Hi-Z | A ₂₃ -A ₁₆ | Hi-Z | A ₁₅ -A ₈ | Hi-Z | A ₇ -A ₀ | Hi-Z | - | - | | |
| Chip-Erase ⁹ | | 60H | Hi-Z | - | - | - | - | - | - | - | - | | |
| Byte-Program ⁵ | 50 | 02H | Hi-Z | A ₂₃ -A ₁₆ | Hi-Z | A ₁₅ -A ₈ | Hi-Z | A ₇ -A ₀ | Hi-Z | D _{IN} | Hi-Z | | |
| Auto Address Increment - word programming (AAI) ⁶ | and | AFH | Hi-Z | A ₂₃ -A ₁₆ | Hi-Z | A ₁₅ -A ₈ | Hi-Z | A ₇ -A ₀ | Hi-Z | D _{IN} | Hi-Z | | |
| Read-Status-Register (RDSR) | 75 | 05H | Hi-Z | X | D _{OUT} | - | Note ⁷ | - | Note ⁷ | - | Note ⁷ | | |
| Enable-Write-Status-Register (EWSR) ⁸ | and | 50H | Hi-Z | - | - | - | - | - | - | - | - | | |
| Write-Status-Register (WRSR) ⁸ | 100 | 01H | Hi-Z | Data | Hi-Z | - | - | - | - | - | - | | |
| Write-Enable (WREN) ¹¹ | | 06H | Hi-Z | - | - | - | - | - | - | - | - | | |
| Write-Disable (WRDI) | | 04H | Hi-Z | - | - | - | - | - | - | - | - | | |
| Jedec-Read-ID (JEDEC-ID) ¹⁰ | | 9FH | Hi-Z | X | 8CH | X | 8CH | X | 8CH | - | - | | |

1. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out
2. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary)
3. One bus cycle is eight clock periods.
4. Sector addresses: use AMS-A12, remaining addresses can be V_{IL} or V_{IH}
5. Prior to any Byte-Program, AAI-Program, Sector-Erase, or Chip-Erase operation, the Write-Enable (WREN) instruction must be executed.
6. To continue programming to the next sequential address location, enter the 8-bit command, AFH, followed by the data to be programmed.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on \overline{CE} .
8. The Enable-Write-Status-Register (EWSR) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the EWSR instruction to make both instructions effective.
9. The Jedec-Read-ID is continuous with on going clock cycles until terminated by a low to high transition on \overline{CE} .
10. The Jedec-Read-ID is output first byte 8CH as manufacture ID; second byte 8CH as top memory type; third byte 8CH as memory capacity.
11. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. Both EWSR and WREN can enable WRSR, user just need to execute one of it. A successful WRSR can reset WREN.

Read (33 MHz)

The Read instruction supports up to 33 MHz, it outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on \overline{CE} . The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning

(wrap-around) of the address space, i.e. for 4 Mbit density, once the data from address location 7FFFFH had been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A₂₃-A₀]. \overline{CE} must remain active low for the duration of the Read cycle. See Figure 4 for the Read sequence.

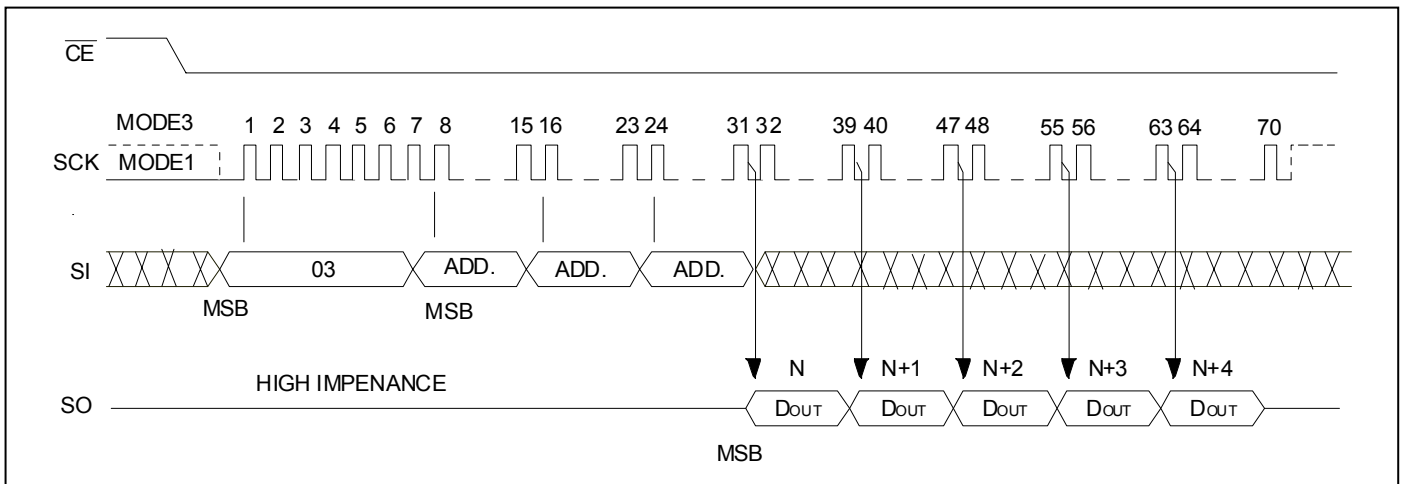


Figure 4 : READ SEQUENCE

Fast-Read (50 MHz ; 75 MHz; 100 MHz)

The High-Speed-Read instruction supporting up to 100 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [A₂₃-A₀] and a dummy byte. \overline{CE} must remain active low for the duration of the High-Speed-Read cycle. See Figure 5 for the High-Speed-Read sequence. Following a dummy byte (8 clocks input dummy cycle), the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous

through all addresses until terminated by a low to high transition on \overline{CE} . The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 4 Mbit density, once the data from address location 07FFFFH has been read, the next output will be from address location 000000H.

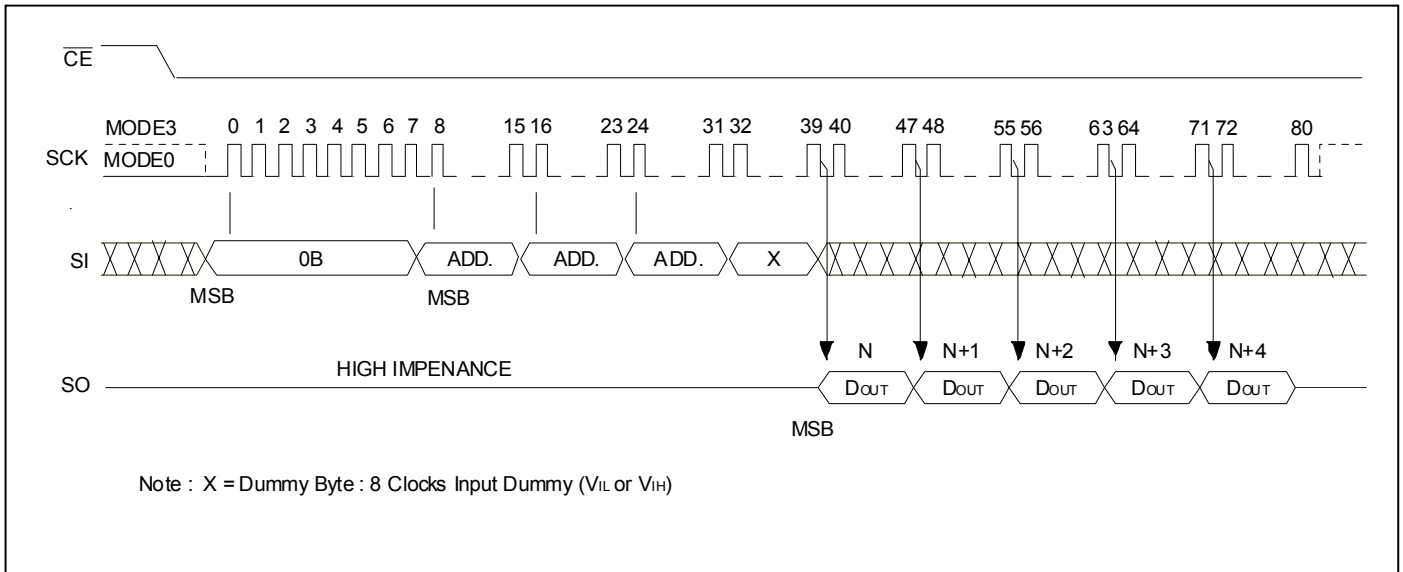


Figure 5 : HIGH-SPEED-READ SEQUENCE

Byte-Program

The Byte-Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte-Program instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. \overline{CE} must remain active low for the duration of the Byte-Program instruction. The Byte-Program

instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A₂₃-A₀]. Following the address, the data is input in order from MSB (bit 7) to LSB (bit 0). \overline{CE} must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait TBP for the completion of the internal self-timed Byte-Program operation. See Figure 6 for the Byte-Program sequence.

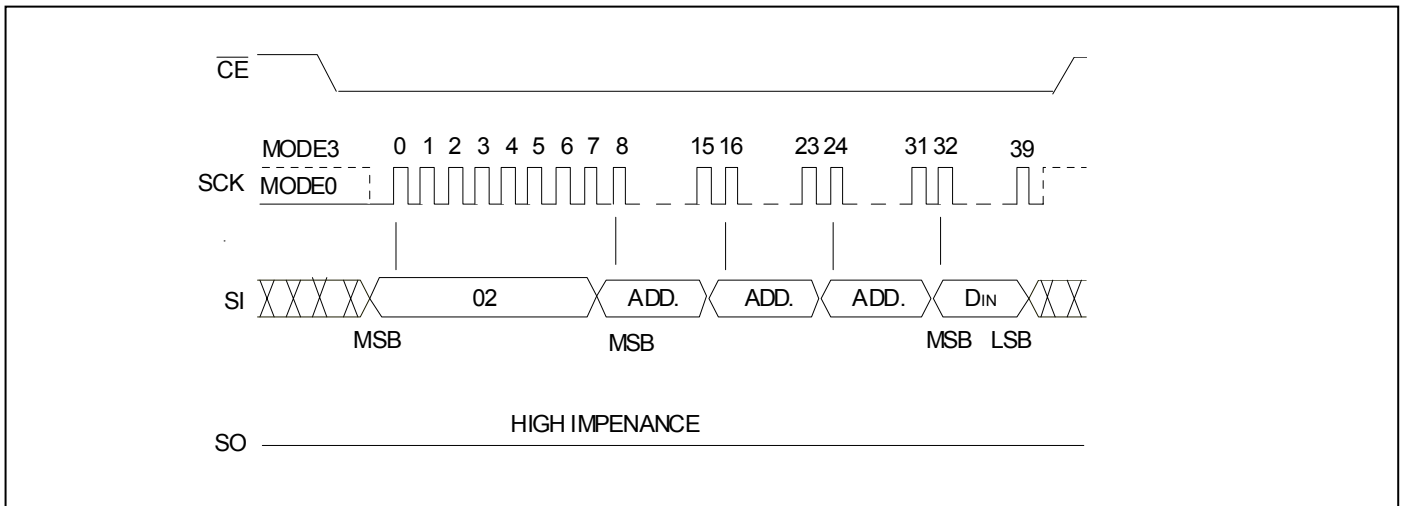


Figure 6 : BYTE-PROGRAM SEQUENCE

Auto Address Increment (AAI) Program

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when the entire memory array is to be programmed. An AAI program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI program instruction.

Prior to any write operation, the Write-Enable (WREN) instruction must be executed. The AAI program instruction is initiated by executing an 8-bit command, AFH, followed by address bits [A₂₃-A₀]. Following the addresses, the data is input sequentially from MSB (bit 7) to LSB (bit 0). \overline{CE} must be driven high before the AAI program instruction is executed. The user must poll the

BUSY bit in the software status register or wait TBP for the completion of each internal self-timed Byte-Program cycle. Once the device completes programming byte, the next sequential address may be program, enter the 8-bit command, AFH, followed by the data to be programmed. When the last desired byte had been programmed, execute the Write-Disable (WRDI) instruction, 04H, to terminate AAI. After execution of the WRDI command, the user must poll the Status register to ensure the device completes programming. See Figure 7 for AAI programming sequence.

There is no wrap mode during AAI programming; once the highest unprotected memory address is reached, the device will exit AAI operation and reset the Write-Enable-Latch bit (WEL = 0).

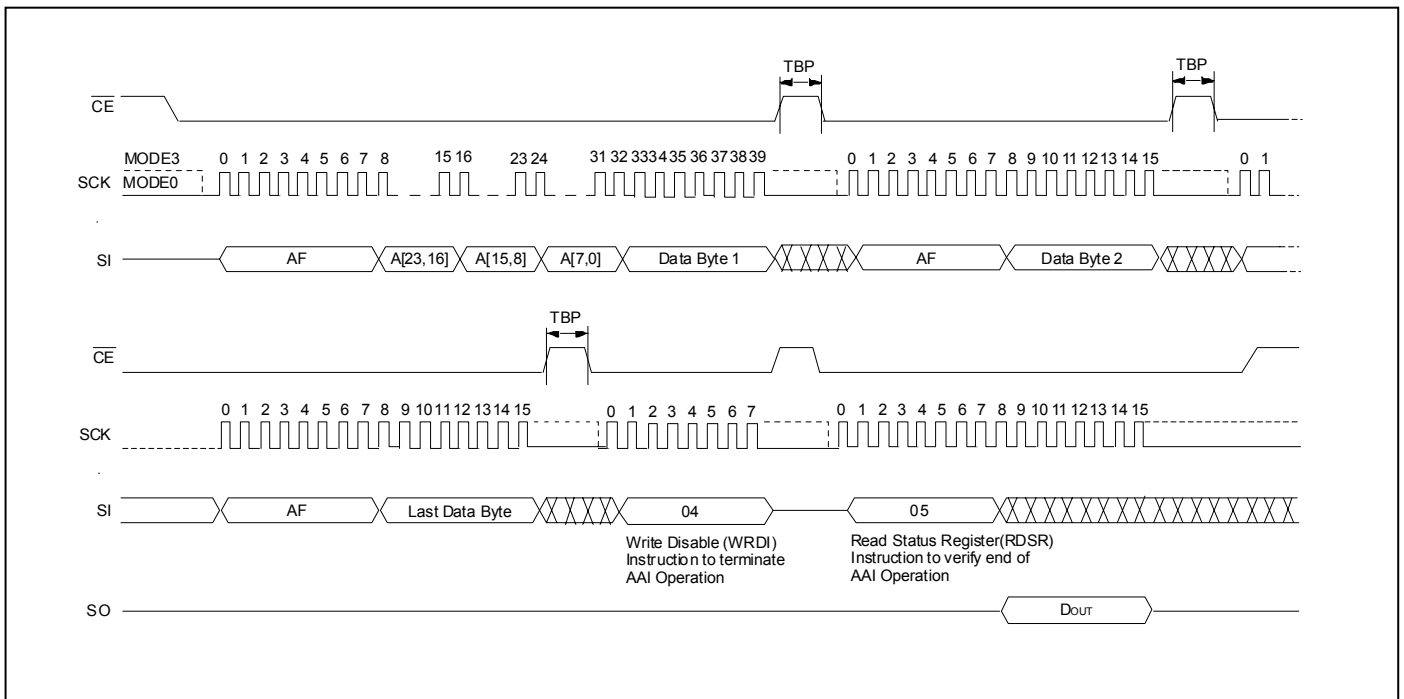


Figure 7 : AUTO ADDRESS INCREMENT (AAI) PROGRAM SEQUENCE

Sector-Erase

The Sector-Erase instruction clears all bits in the selected sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. \overline{CE} must remain active low for the duration of the any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A₂₃-A₀]. Address bits

[A_{MS}-A₁₂] (A_{MS} = Most Significant address) are used to determine the sector address (SA_x), remaining address bits can be VIL or VIH. \overline{CE} must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait TSE for the completion of the internal self-timed Sector-Erase cycle. See Figure 8 for the Sector-Erase sequence.

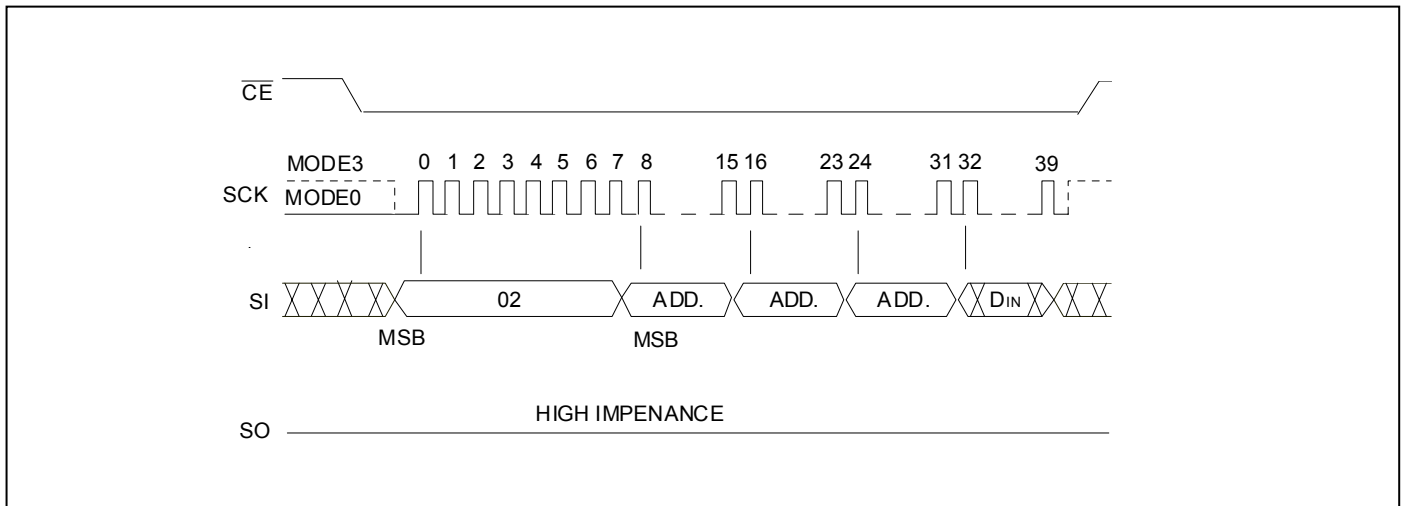


FIGURE 8 : SECTOR-ERASE SEQUENCE

Chip-Erase

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. \overline{CE} must remain active low for the duration of the Chip-Erase instruction sequence. The Chip-Erase instruction is initiated by executing an 8-bit command,

60H. \overline{CE} must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T_{CE} for the completion of the internal self-timed Chip-Erase cycle.

See Figure 9 for the Chip-Erase sequence.

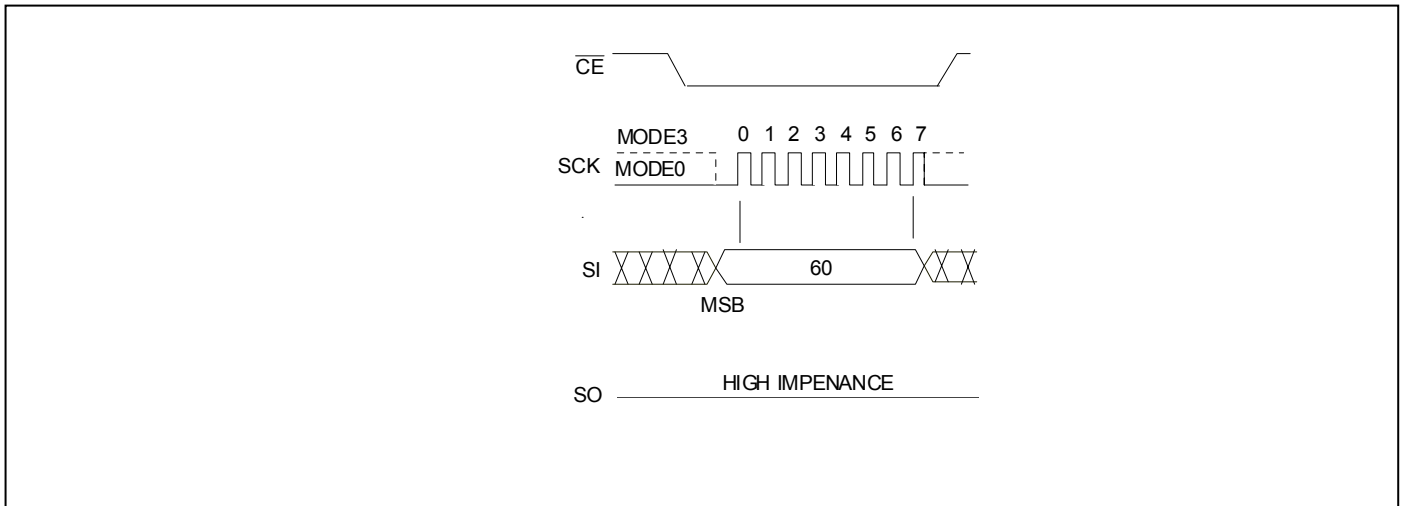


FIGURE 9 : CHIP-ERASE SEQUENCE

Read-Status-Register (RDSR)

The Read-Status-Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation.

When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

\overline{CE} must be driven low before the RDSR instruction is entered

and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles

until it is terminated by a low to high transition of the \overline{CE}

See Figure 10 for the RDSR instruction sequence.

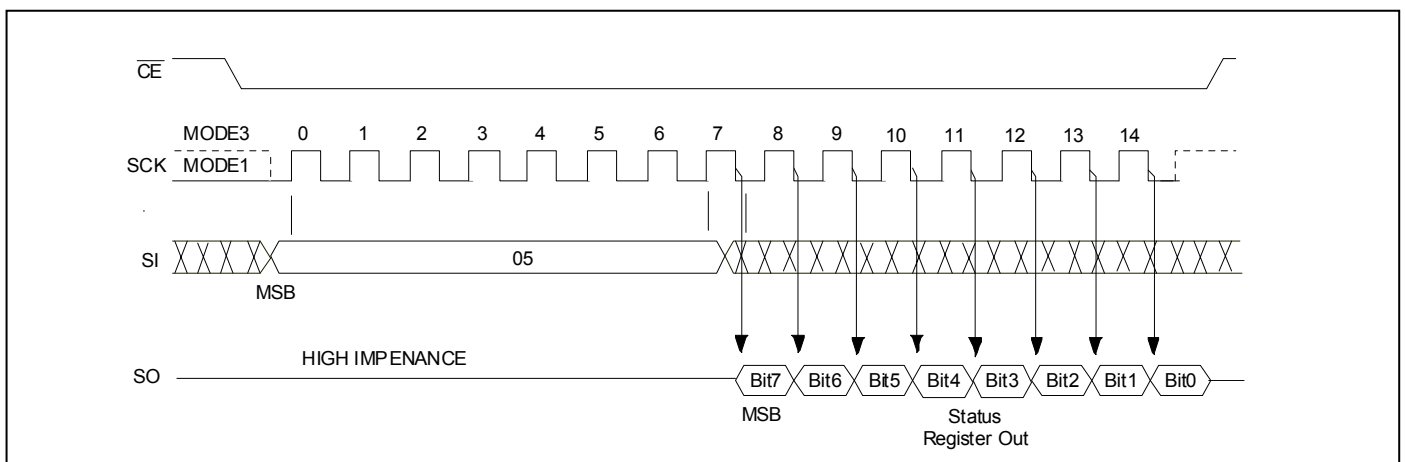


Figure10 : READ-STATUS-REGISTER (RDSR) SEQUENCE

Write-Enable (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit to 1 allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. \overline{CE} must be driven high before the WREN instruction is executed.

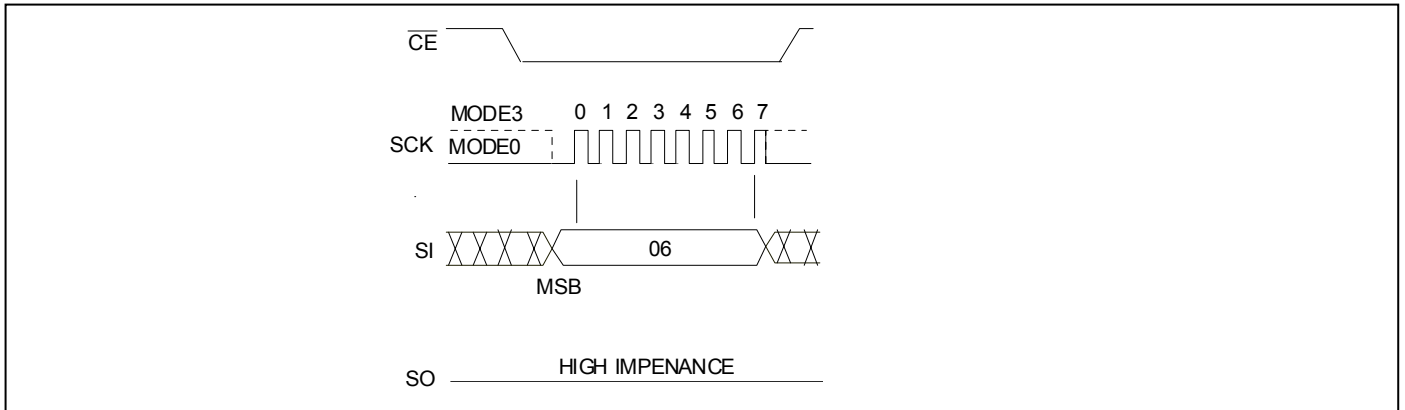


FIGURE 11 : WRITE ENABLE (WREN) SEQUENCE

Write-Disable (WRDI)

The Write-Disable (WRDI) instruction resets the Write-Enable-Latch bit and AAI bit to 0 disabling any new Write operations from occurring. \overline{CE} must be driven high before the WRDI instruction is executed.

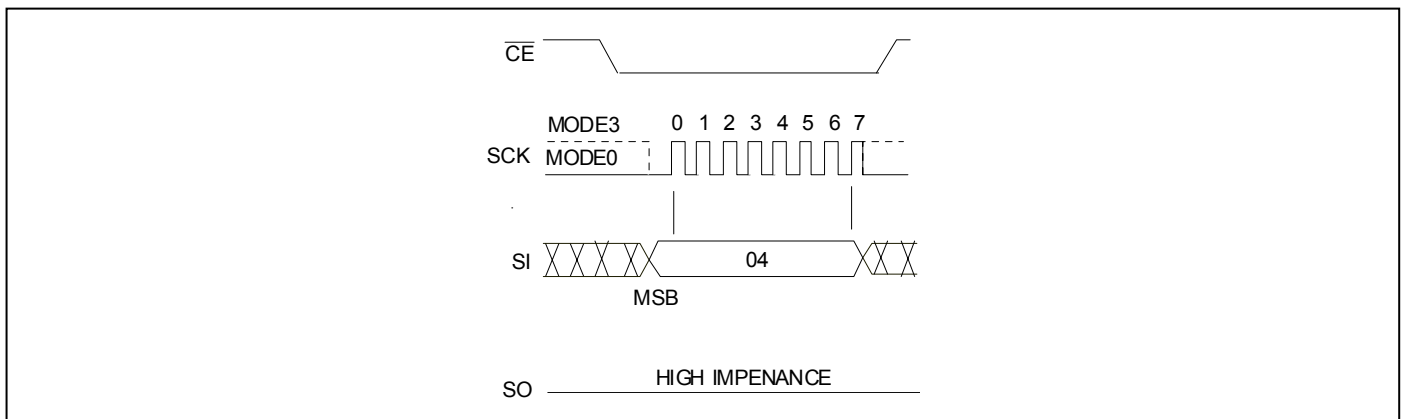


Figure 12 : WRITE DISABLE (WRDI) SEQUENCE

Enable-Write-Status-Register (EWSR)

The Enable-Write-Status-Register (EWSR) instruction arms the Write-Status-Register (WRSR) instruction and opens the status register for alteration. The Enable-Write-Status-Register instruction does not have any effect and will be wasted, if it is not followed immediately by the Write-Status-Register (WRSR) instruction. \overline{CE} must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Write-Status-Register (WRSR)

The Write-Status-Register instruction works in conjunction with the Enable-Write-Status-Register (EWSR) instruction to write new values to the BP1, BP0, and BPL bits of the status register. The Write-Status-Register instruction must be executed immediately after the execution of the Enable-Write-Status-Register instruction (very next instruction bus cycle). This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like SDP (software data protection) command structure which prevents any accidental alteration of the status register values. The Write-Status-Register instruction will be ignored when \overline{WP} is low and BPL bit is set to "1". When the \overline{WP} is low, the BPL bit can only be set from "0" to "1" to lockdown the status register, but cannot be reset from "1" to "0".

When \overline{WP} is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, and BP1 bits in the status register can all be changed. As long as BPL bit is set to 0 or \overline{WP} pin is driven high (V_{IH}) prior to the low-to-high transition of the \overline{CE} pin at the end of the WRSR instruction, the BP0, BP1, and BPL bit in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to "1" to lock down the status register as well as altering the BP0 and BP1 bit at the same time. See Table 3 for a summary description of \overline{WP} and BPL functions. \overline{CE} must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 13 for EWSR and WRSR instruction sequences.

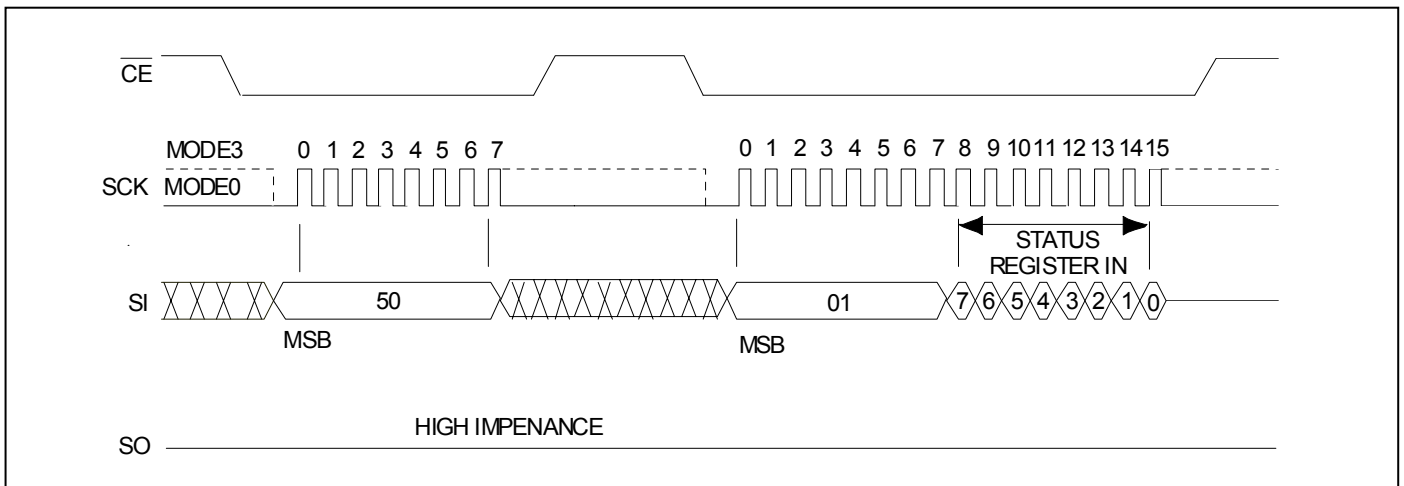
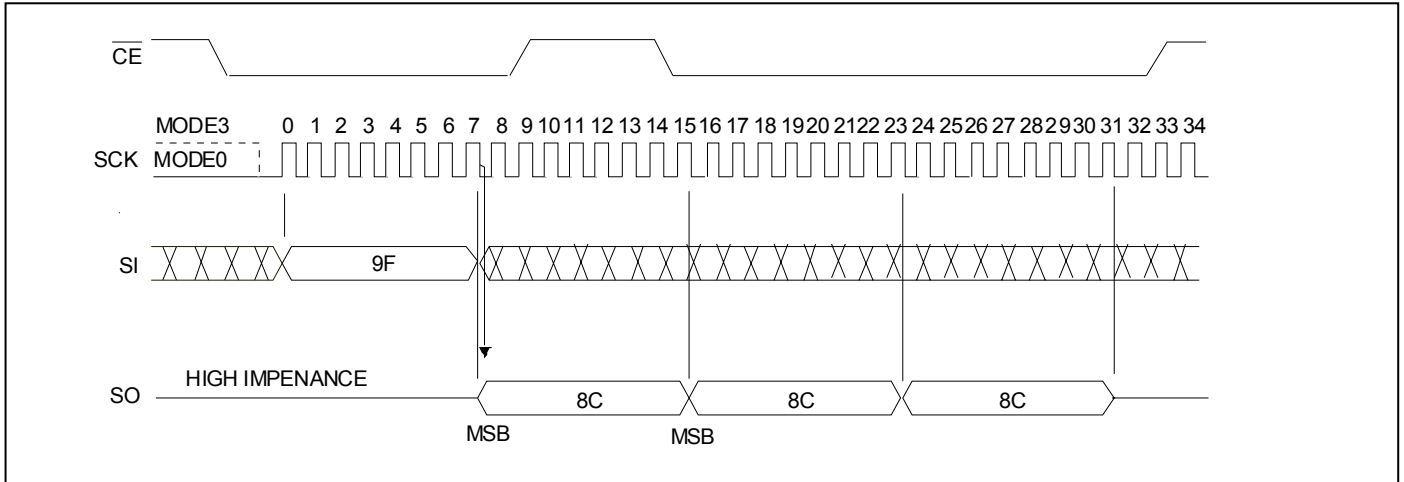


Figure 13 : ENABLE-WRITE-STATUS-REGISTER (EWSR) AND WRITE-STATUS-REGISTER (WRSR) SEQUENCE

Jedec-Read-ID (JEDEC-ID)

The Jedec-Read-ID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The ESMT Manufacturer ID is 8CH.,the memory type ID is 8CH as the first-byte device ID, the memory capacity ID is 8CH as the second-byte device ID. The instruction sequence is shown in Fig14. The Jedec-Read-ID instruction is terminated by a low to high transition on CE at any time during data output.

Figure 14 : Jedec-Read-ID (JEDEC-ID)



Jedec-Read-ID DATA

| Manufacture's ID | Device ID | |
|------------------|-------------|-----------------|
| | Memory Type | Memory Capacity |
| Byte1 | Byte2 | Byte3 |
| 8CH | 8CH | 8CH |

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings

(Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|---|-------------------|
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to VDD+0.5V |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -2.0V to VDD+2.0V |
| Package Power Dissipation Capability (Ta = 25°C) | 1.0W |
| Surface Mount Lead Soldering Temperature (3 Seconds) | 240°C |
| Output Short Circuit Current (Note1) | 50 mA |

Note : 1. Output shorted for no more than one second. No more than one output shorted at a time.

AC CONDITIONS OF TEST

| | |
|----------------------------|-----------------------|
| Input Rise/Fall Time | <5 ns |
| Output Load | CL = 15 pF for ≥75MHz |
| | CL = 30 pF for ≤50MHz |
| See Figures 19 and 20 | |

OPERATING RANGE

| Parameter | Symbol | Value | Unit |
|-------------------------------|-------------------------|---------|------|
| Operating Supply Voltage | VDD (for FCLK ≤ 75MHz) | 2.7~3.6 | V |
| | VDD (for FCLK = 100MHz) | 3.2~3.6 | |
| Ambient Operating Temperature | TA | 0~70 | °C |

TABLE 7: DC OPERATING CHARACTERISTICS

| Symbol | Parameter | Limits | | | Test Conditions |
|--------|---------------------------|---------|-----|-------|--|
| | | Min | Max | Units | |
| IDDR | Read Current | | 15 | mA | CE = 0.1 VDD/0.9 VDD @ 33 MHz, SO=open |
| IDDW | Program and Erase Current | | 40 | mA | CE = VDD |
| ISB | Standby Current | | 25 | µA | CE = VDD, VIN = VDD or VSS |
| ILI | Input Leakage Current | | 1 | µA | VIN = GND to VDD, VDD = VDD Max |
| ILO | Output Leakage Current | | 1 | µA | VOU = GND to VDD, VDD = VDD Max |
| VIL | Input Low Voltage | | 0.8 | V | VDD = VDD Min |
| VIH | Input High Voltage | 0.7 VDD | | V | VDD = VDD Max |
| VOL | Output Low Voltage | | 0.2 | V | IOL = 100 µA, VDD = VDD Min |
| VOH | Output High Voltage | VDD-0.2 | | V | IOH = -100 µA, VDD = VDD Min |

TABLE 8 : RECOMMENDED SYSTEM POWER-UP TIMINGS

| Symbol | Parameter | Minimum | Units |
|------------------------------------|----------------------------|---------|-------|
| T _{PU-READ} ¹ | VDD Min to Read Operation | 10 | µs |
| T _{PU-WRITE} ¹ | VDD Min to Write Operation | 10 | µs |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: CAPACITANCE (TA = 25°C, f=1 Mhz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------------------------|------------------------|-----------------------|---------|
| C _{OUT} ¹ | Output Pin Capacitance | V _{OUT} = 0V | 12 pF |
| C _{IN} ¹ | Input Capacitance | V _{IN} = 0V | 6 pF |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Typical Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 100,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 10 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | 100 + IDD | mA | JEDEC Standard 78 |

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11 : AC OPERATING CHARACTERISTICS

| Symbol | Parameter | Normal 33MHz | | Fast 50 MHz | | Fast 75 MHz | | Fast 100 MHz | | Units |
|-------------|--|--------------|-----|-------------|-----|-------------|-----|--------------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| F_{CLK} | Serial Clock Frequency | | 33 | | 50 | | 75 | | 100 | MHz |
| T_{SCKH} | Serial Clock High Time | 13 | | 9 | | 6 | | 5 | | ns |
| T_{SCKL} | Serial Clock Low Time | 13 | | 9 | | 6 | | 5 | | ns |
| T_{CES}^1 | \overline{CE} Active Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{CEH}^1 | \overline{CE} Active Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{CHS}^1 | \overline{CE} Not Active Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{CHH}^1 | \overline{CE} Not Active Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{CPH} | \overline{CE} High Time | 100 | | 100 | | 100 | | 100 | | ns |
| T_{CHZ} | \overline{CE} High to High-Z Output | | 9 | | 9 | | 9 | | 9 | ns |
| T_{CLZ} | SCK Low to Low-Z Output | 0 | | 0 | | 0 | | 0 | | ns |
| T_{DS} | Data In Setup Time | 3 | | 3 | | 3 | | 3 | | ns |
| T_{DH} | Data In Hold Time | 3 | | 3 | | 3 | | 3 | | ns |
| T_{HLS} | \overline{HOLD} Low Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{HHS} | \overline{HOLD} High Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{HLH} | \overline{HOLD} Low Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{HHH} | \overline{HOLD} High Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| T_{HZ} | \overline{HOLD} Low to High-Z Output | | 9 | | 9 | | 9 | | 9 | ns |
| T_{LZ} | \overline{HOLD} High to Low-Z Output | | 9 | | 9 | | 9 | | 9 | ns |
| T_{OH} | Output Hold from SCK Change | 0 | | 0 | | 0 | | 0 | | ns |
| T_V | Output Valid from SCK | | 12 | | 9 | | 9 | | 7 | ns |

1. Relative to SCK.

ERASE AND PROGRAMMING PERFORMANCE

| Parameter | Symbol | Limits | | Unit |
|-------------------------|-----------------|---------|---------|--------|
| | | Typ.(2) | Max.(3) | |
| Sector Erase Time | T _{SE} | 0.7 | 15 | sec |
| Chip Erase Time | T _{CE} | 11 | 50 | sec |
| Byte Programming Time | T _{BP} | 9 | 300 | us |
| Chip Programming Time | | 4.5 | 13.5 | sec |
| Erase/Program Cycles(1) | | 100,000 | - | Cycles |

Notes:

1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 3V.
3. Maximum values measured at 85°C, V_{DD}(min).

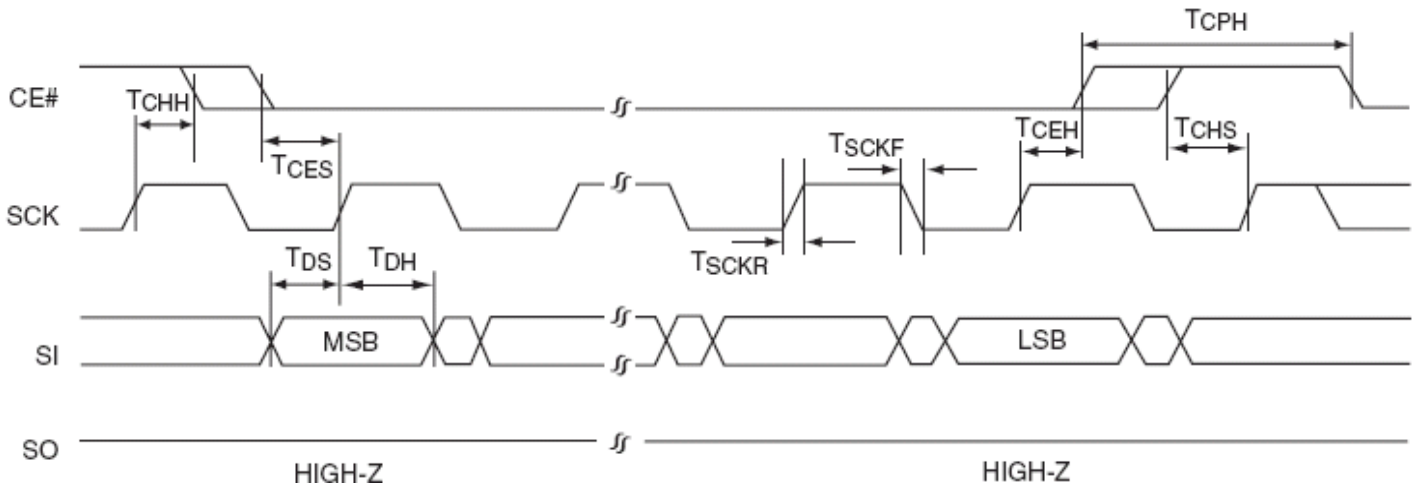


FIGURE 15: SERIAL INPUT TIMING DIAGRAM

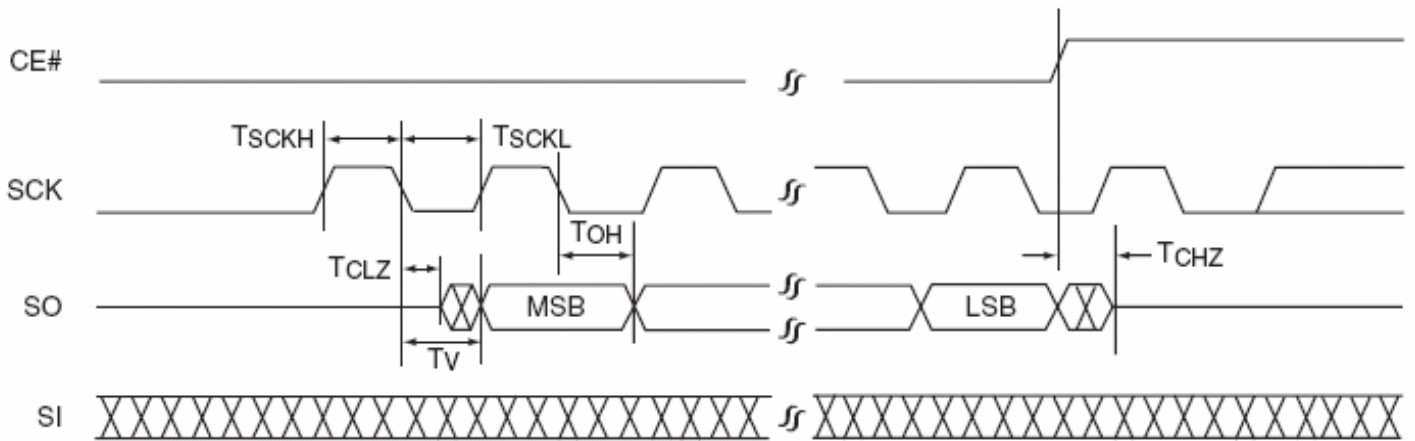


FIGURE 16: SERIAL OUTPUT TIMING DIAGRAM

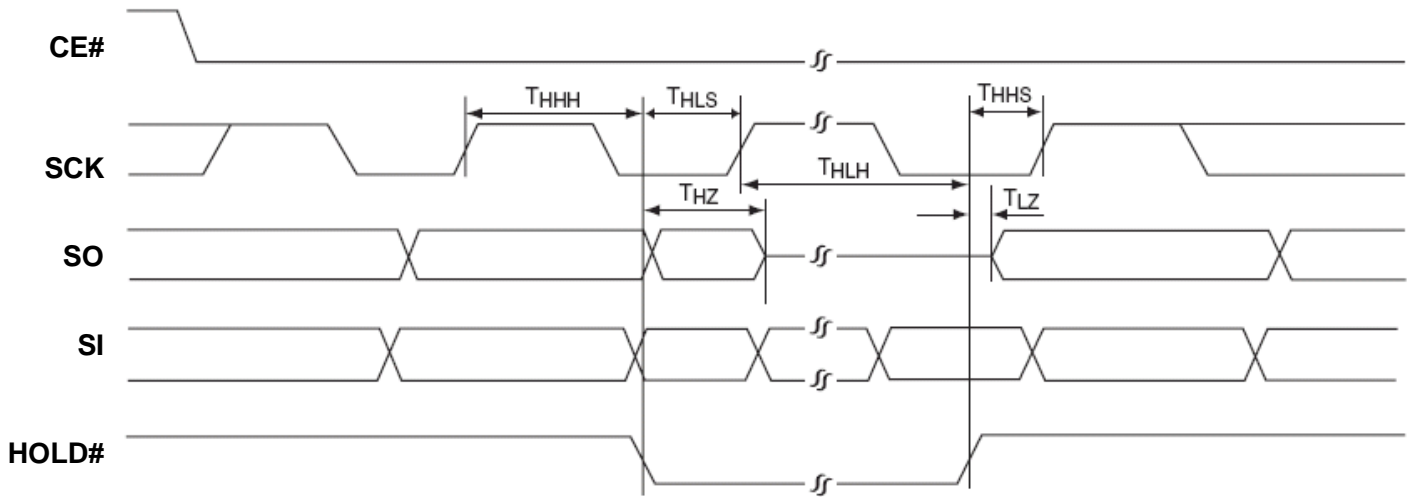


FIGURE 17: HOLD TIMING DIAGRAM

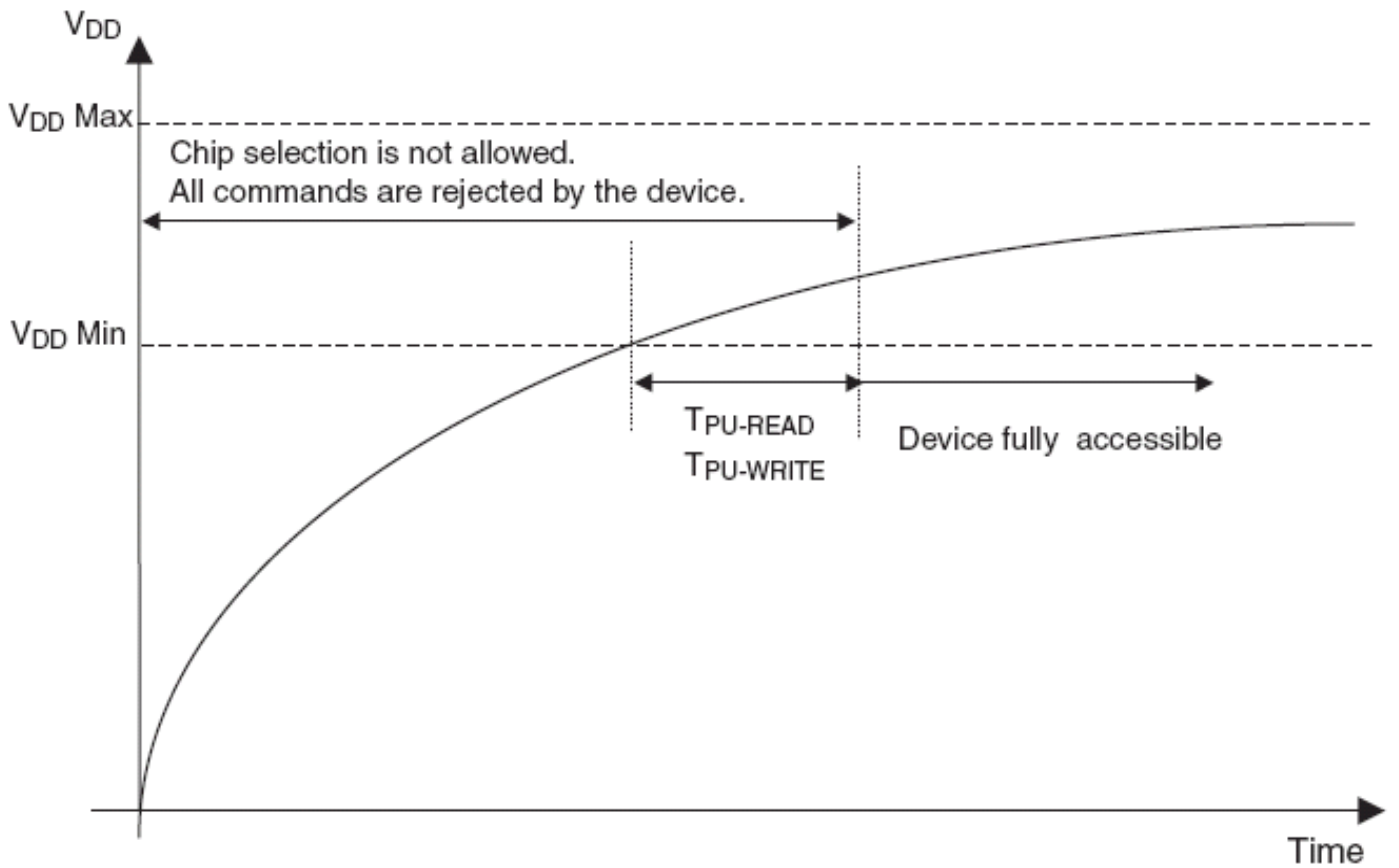


FIGURE 18: POWER-UP TIMING DIAGRAM

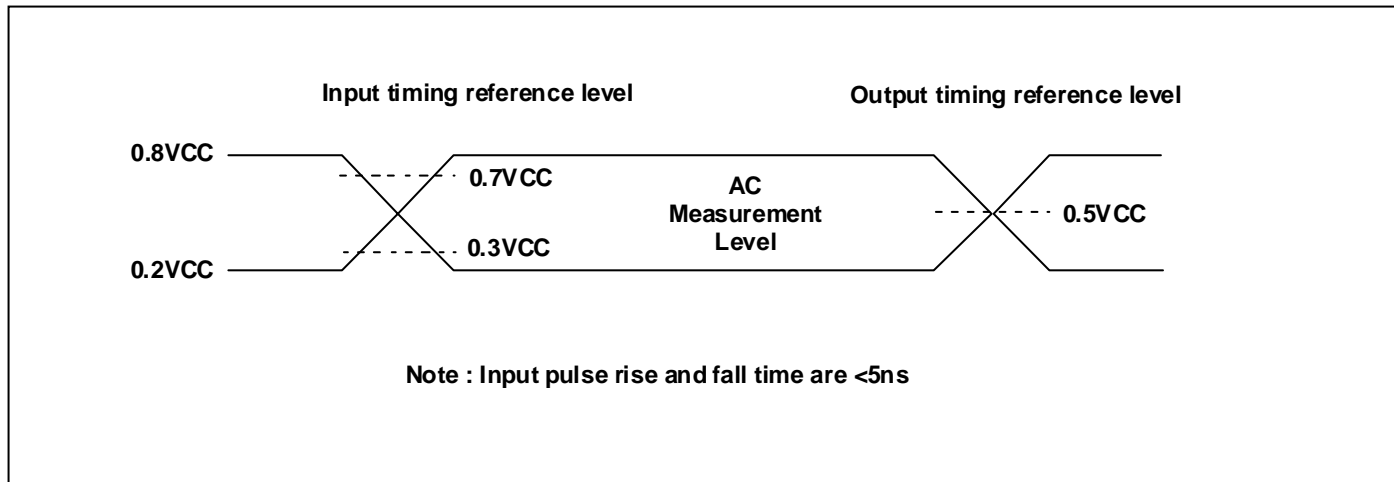


FIGURE 19: AC INPUT/OUTPUT REFERENCE WAVEFORMS

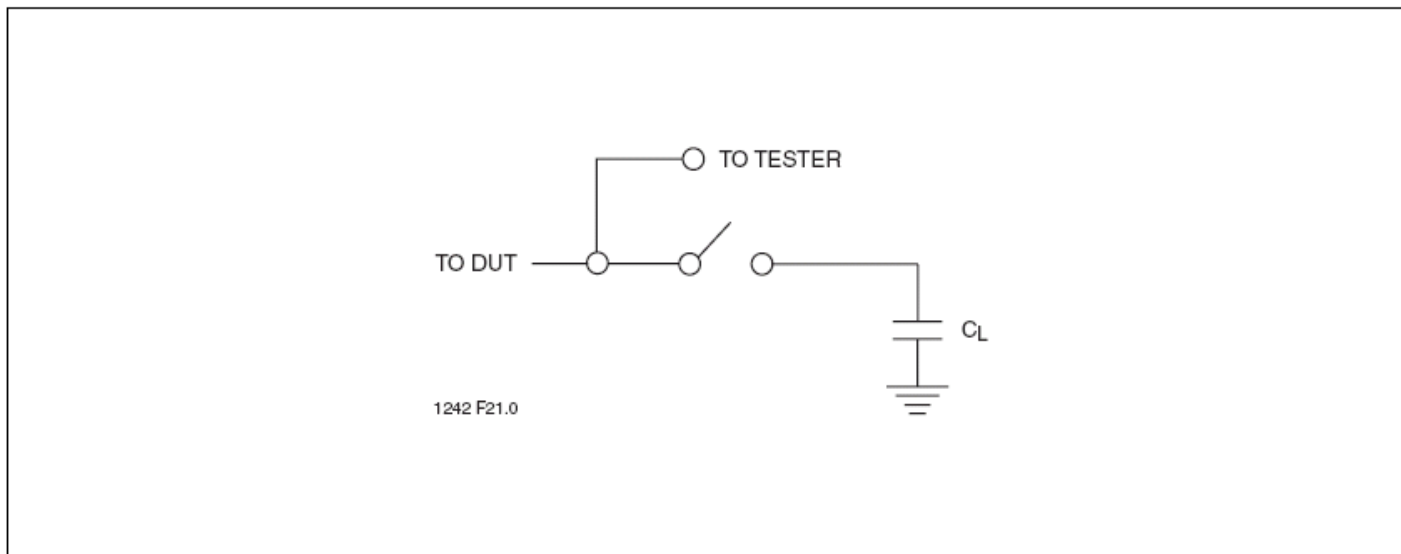
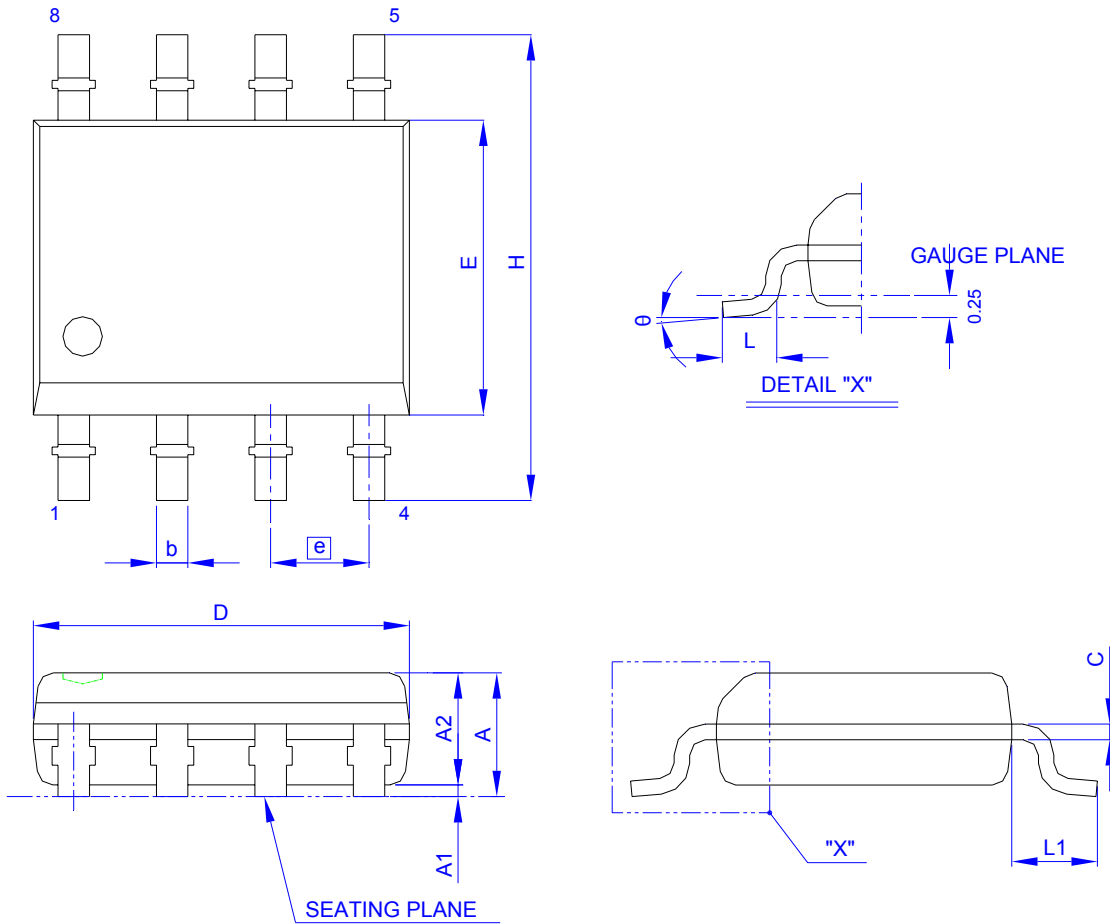


FIGURE 20: A TEST LOAD EXAMPLE

PACKAGING DIAGRAMS

8-LEAD SOIC (150 mil)



| Symbol | Dimension in mm | | | Dimension in inch | | | Symbol | Dimension in mm | | | Dimension in inch | | |
|----------------|-----------------|-------|------|-------------------|-------|-------|----------------|-----------------|------|------|-------------------|-------|-------|
| | Min | Norm | Max | Min | Norm | Max | | Min | Norm | Max | Min | Norm | Max |
| A | 1.35 | 1.60 | 1.75 | 0.053 | 0.063 | 0.069 | D | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| A ₁ | 0.10 | 0.15 | 0.25 | 0.004 | 0.006 | 0.010 | E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| A ₂ | 1.25 | 1.45 | 1.55 | 0.049 | 0.057 | 0.061 | L | 0.40 | 0.66 | 0.86 | 0.016 | 0.026 | 0.034 |
| b | 0.33 | 0.406 | 0.51 | 0.013 | 0.016 | 0.020 | e | 1.27 BSC | | | 0.050 BSC | | |
| c | 0.19 | 0.203 | 0.25 | 0.0075 | 0.008 | 0.010 | L ₁ | 1.00 | 1.05 | 1.10 | 0.039 | 0.041 | 0.043 |
| H | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 | θ | 0° | --- | 8° | 0° | --- | 8° |

Controlling dimension : millimeter

Revision History

| Revision | Date | Description |
|-----------------|-------------|---|
| 1.0 | 2006.02.15 | Original |
| 1.1 | 2006.09.05 | 1. Erase/Program cycles (min) = 100,000 cycles 2. Delete min. 3. Add Erase/program cycle note 1 4. Modify Note3 from 25° C to 85° C |
| 1.2 | 2008.01.13 | 1. Correct the size of "L" in the packaging diagram of SOIC 150 mil 2. Add operating range table 3. Delete the rating of Temperature Under Bias 4. Add the symbol for erase and byte programming time 5. Correct typo error 6. Modify headline 7. Add Revision History 8. Correct part no. |

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