

Flash**3.3V 1 Gbit****SPI-NAND Flash Memory****PRODUCT LIST**

| Parameters | Values |
|-------------------------|--------------------------|
| V _{CC} | 3.3V |
| Width | x1, x2 ¹ , x4 |
| Frequency | 104MHz |
| Internal ECC Correction | 1-bit |
| Transfer Rate | 9.6ns |
| Loading Throughput | 104MT/s |
| Power-up Ready Time | 1ms (maximum value) |
| Max Reset Busy Time | 1ms (maximum value) |

Note: 1. x2 PROGRAM operation is not defined.

FEATURES

- Voltage Supply: 3.3V (2.7V~3.6V)
- Organization
 - Memory Cell Array: (128M + 4M) x 8bit
 - Data Register: (2K + 64) x 8bit
- Automatic Program and Erase
 - Page Program: (2K + 64) Byte
 - Block Erase: (128K + 4K) Byte
- Page Read Operation
 - Page Size: (2K + 64) Byte
 - Read from Cell to Register with Internal ECC: 100us
- Memory Cell: 1bit/Memory Cell
- Support SPI-Mode 0 and SPI-Mode 3¹
- Fast Write Cycle Time
 - Program time:400us
 - Block Erase time: 4ms
- Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
 - Internal ECC Requirement: 1bit/512Byte
 - Endurance: 100K Program/Erase cycles
 - Data Retention: 10 years
- Command Register Operation
- NOP: 4 cycles
- OTP Operation
- Bad-Block-Protect
- Boot Read

Note: 1. Mode 0: CPOL = 0, CPHA = 0; Mode 3: CPOL = 1, CPHA = 1

ORDERING INFORMATION

| Product ID | Speed | Package | | Comments |
|---------------------|--------|---|-------|----------|
| F50L1G41LB-104YG2M | 104MHz | 8-contact WSON | 8x6mm | Pb-free |
| F50L1G41LB-104YG2ME | 104MHz | 8-contact WSON (without expose metal pad) | 8x6mm | Pb-free |

GENERAL DESCRIPTION

The serial electrical interface follows the industry-standard serial peripheral interface (SPI), providing a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. The device is a 1Gb SLC SPI-NAND Flash memory device based on the standard parallel NAND Flash, but new command protocols and registers are defined for SPI operation. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

The command set resembles common SPI-NOR command set, modified to handle NAND-specific functions and new features. New features include user-selectable internal ECC. With internal ECC enabled, ECC code is generated internally when a page is written to the memory array. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

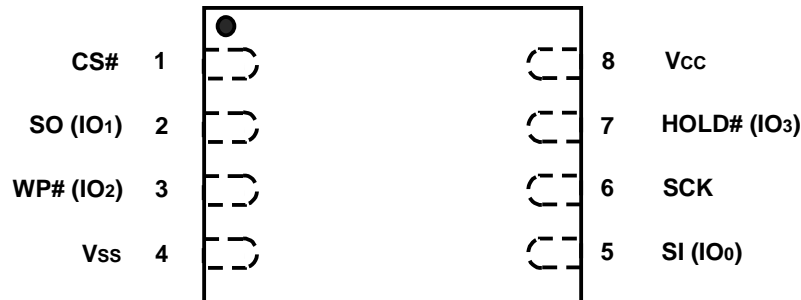
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Each page consists 2112-Byte and is further divided into a 2048-Byte data storage area with a separate 64-Byte spare area. The 64-Byte area is typically used for memory and error management.

The pins serve as the ports for signals. The device has six signal lines plus V_{CC} and ground (GND, V_{SS}). The signal lines are SCK (serial clock), SI (command and data input), SO (response and data output), and control signals CS#, HOLD#, WP#.

PIN CONFIGURATION (TOP VIEW)

8-Contact WSON

(WSON 8C, 8mmx6 mm Body, 1.27mm Contact Pitch)



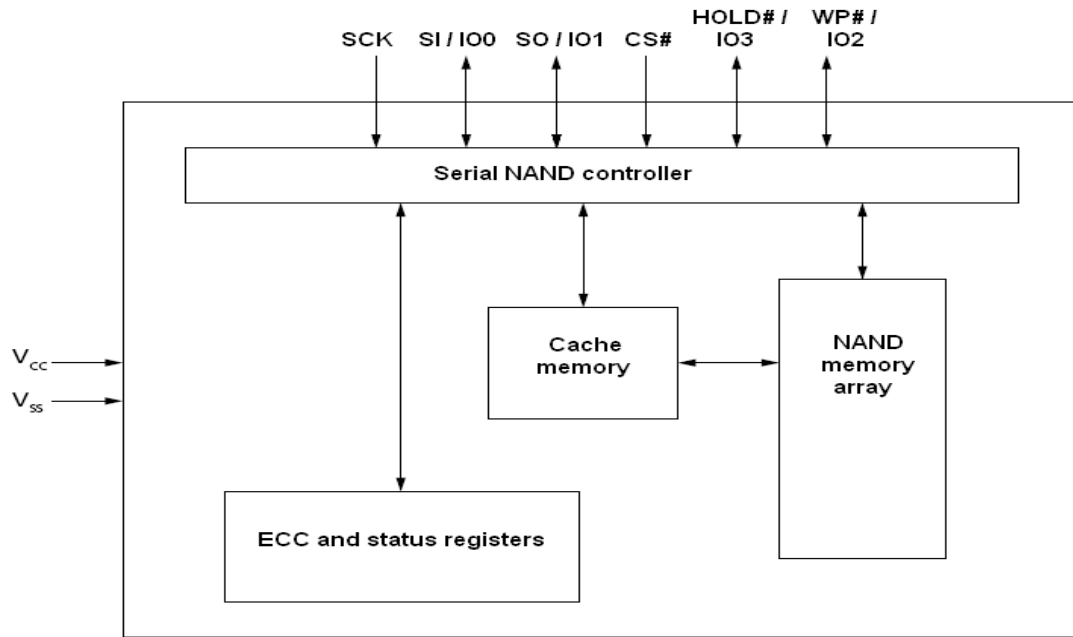
Pin Description

| Pin Name | Functions |
|--------------------------------|---|
| CS# | Chip Select (Input) The device is activated ⁽¹⁾ /deactivated ⁽²⁾ as CS# is driven LOW/HIGH. After power-on, the device requires a falling-edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. |
| HOLD# / IO ₃ | Hold (Input) / IO₃ (Input/Output) Hold pauses any serial communication with the device without deselecting it ⁽³⁾ . When driven LOW, SO is at high impedance (Hi-Z), and all inputs in SI and SCK are ignored; CS# also should be driven LOW. HOLD# must not be driven during x4 operation; it means HOLD function is only available for standard and x2 SPI. |
| WP# / IO ₂ | Write Protect (Input) / IO₂ (Input/Output) WP# is driven LOW to prevent writing the Feature Registers. The WP-E bit in Protection Register controls the function of WP#, and the other bits in Register can protect a specific portion by hardware. When WP-E=1, the device is in the Hardware-protection mode that WP# functions as a dedicated active low input pin for the Write Protect of the device. If WP-E=1 and WP# goes LOW, the device will become READ-only. When WP-E=0, the device is in the Software-protection mode that only Protection Register can be protected. WP# functions as a data I/O pin. WP# must not be driven during x4 operation; it means Write Protect function is only available for standard and x2 SPI. |
| SCK | Serial Clock (Input) SCK provides serial interface timing. Address, commands, and data in SI are latched on the rising edge of SCK. Output (data in SO) is triggered after the falling-edge of SCK. The clock is valid only when the device is active. ⁽⁴⁾ |
| SI / IO ₀ | Serial Data Input (Input) / IO₀ (Input/Output) SI transfers data serially into the device. Device latches addresses, commands, and program data in SI on the rising-edge of SCK. SI must not be driven during x2 or x4 READ operation. |
| SO / IO ₁ | Serial Data Output (Output) / IO₁ (Input/Output) SO transfers data serially out of the device on the falling-edge of SCK. SO must not be driven during x2 or x4 PROGRAM operation. |
| V _{CC} ⁽⁵⁾ | Power V _{CC} is the power supply for device. |
| V _{SS} ⁽⁵⁾ | Ground |
| NC | No Connection Not internally connected. |

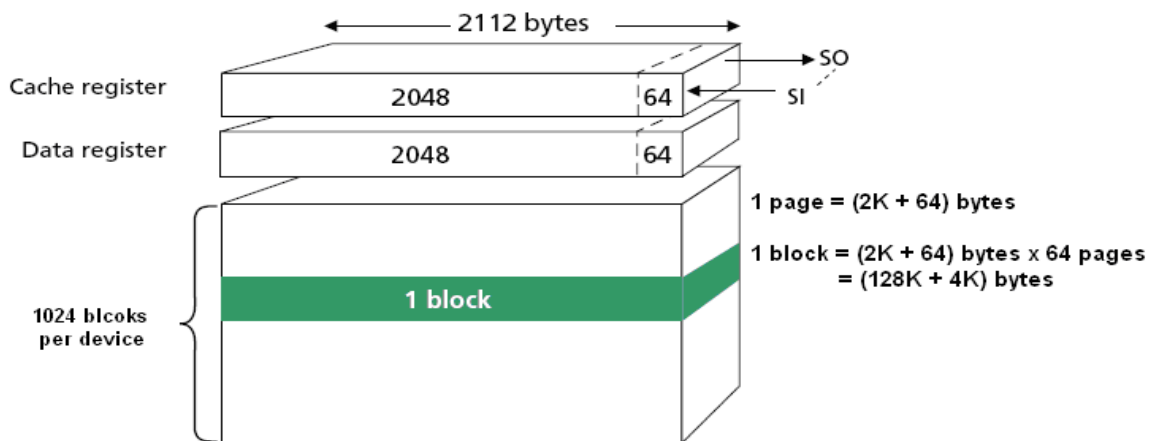
Note:

1. CS# places the device in active power mode.
2. CS# deselects the device and places SO at high impedance.
3. It means HOLD# input doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.
4. SI and SO can be triggered only when the clock is valid.
5. Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

BLOCK DIAGRAM



ARRAY ORGANIZATION



Array Address

| Data Bits | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Address |
|----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|
| 1 st byte | A ₀ | A ₁ | A ₂ | A ₃ | A ₄ | A ₅ | A ₆ | A ₇ | Column Address |
| 2 nd byte | A ₈ | A ₉ | A ₁₀ | A ₁₁ | X | X | X | X | Column Address |
| 3 rd byte | A ₁₂ | A ₁₃ | A ₁₄ | A ₁₅ | A ₁₆ | A ₁₇ | A ₁₈ | A ₁₉ | Row Address |
| 4 th byte | A ₂₀ | A ₂₁ | A ₂₂ | A ₂₃ | A ₂₄ | A ₂₅ | A ₂₆ | A ₂₇ | Row Address |
| 5 th byte | X | X | X | X | X | X | X | X | Dummy Address |

Note:

Column Address: Starting Address of the Register.
 X = don't care.
 The device ignores any additional input of address cycles than required.

COMMAND SET

| Function | Op Code | Address Byte | Dummy Byte | Data Bytes |
|--|----------|--------------|------------|------------|
| BLOCK ERASE | D8h | 3 | 0 | 0 |
| GET FEATURE ⁽¹⁾ | 0Fh | 1 | 0 | 1 |
| SET FEATURE | 1Fh | 1 | 0 | 1 |
| WRITE DISABLE | 04h | 0 | 0 | 0 |
| WRITE ENABLE | 06h | 0 | 0 | 0 |
| PROGRAM LOAD | 02h | 2 | 0 | 1 to 2112 |
| PROGRAM LOAD x4 ⁽²⁾ | 32h | 2 | 0 | 1 to 2112 |
| PROGRAM LOAD RANDOM DATA | 84h | 2 | 0 | 1 to 2112 |
| PROGRAM LOAD RANDOM DATA x4 ⁽²⁾ | 34h | 2 | 0 | 1 to 2112 |
| PROGRAM EXECUTE | 10h | 3 | 0 | 0 |
| PAGE READ | 13h | 3 | 0 | 0 |
| READ FROM CACHE | 03h, 0Bh | 2 | 1 | 1 to 2112 |
| READ FROM CACHE with 4Byte Address | 0Ch | 2 | 3 | 1 to 2112 |
| READ FROM CACHE x2 | 3Bh | 2 | 1 | 1 to 2112 |
| READ FROM CACHE x2 with 4Byte Address | 3Ch | 2 | 3 | 1 to 2112 |
| READ FROM CACHE x4 ⁽²⁾ | 6Bh | 2 | 1 | 1 to 2112 |
| READ FROM CACHE x4 with 4Byte Address ⁽²⁾ | 6Ch | 2 | 3 | 1 to 2112 |
| FAST READ X2 IO | BBh | 2 | 1 | 1 to 2112 |
| FAST READ X2 IO with 4Byte Address | BCh | 2 | 3 | 1 to 2112 |
| FAST READ X4 IO | EBh | 2 | 2 | 1 to 2112 |
| FAST READ X4 IO with 4Byte Address | ECh | 2 | 5 | 1 to 2112 |
| READ ID ⁽³⁾ | 9Fh | 1 | 0 | 2 |
| RESET | FFh | 0 | 0 | 0 |

Note:

1. Refer to Feature Register.
2. Command/Address is 1-bit input per clock period, data is 4-bit input/output per clock period.
3. Address is 00h to get JEDEC ID

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|------------|--------------------------------|------|
| Voltage on any pin relative to V_{SS} | V_{CC} | -0.6 to +4.6 | V |
| | V_{IN} | -0.6 to +4.6 | |
| | V_{IO} | -0.6 to $V_{CC} + 0.3$ (< 4.6) | |
| Temperature Under Bias | T_{BIAS} | -40 to +125 | °C |
| Storage Temperature | T_{STG} | -65 to +150 | °C |
| Short Circuit Current | I_{OS} | 5 | mA |

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, $T_A = 0$ to 70°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------|----------|------|------|------|------|
| Supply Voltage | V_{CC} | 2.7 | 3.3 | 3.6 | V |
| Supply Voltage | V_{SS} | 0 | 0 | 0 | V |

DC and Operation Conditions

(Recommended operating conditions otherwise noted)

| Parameter | | Symbol | Test Conditions | Min. | Typ. ² | Max. | Unit |
|-------------------------------|------------------------------|------------|--|---------------------|-------------------|----------------------|------|
| Operating Current | Page Read with Serial Access | I_{CC1} | $f_C=104\text{MHz}$, $CS\#=V_{IL}$, $I_{OUT}=0\text{mA}$ | - | 16 | 20 | mA |
| | Program | I_{CC2} | - | - | 16 | | |
| | Erase | I_{CC3} | - | - | 16 | | |
| Stand-by Current (TTL) | | I_{SB1} | $CS\#=V_{IH}$, $WP\#=0V/V_{CC}$ | - | - | 1 | mA |
| Stand-by Current (CMOS) | | I_{SB2} | $CS\#=V_{CC}-0.2$, $WP\#=0V/V_{CC}$ | - | 10 | 50 | uA |
| Input Leakage Current | | I_{LI} | $V_{IN}=0$ to V_{CC} (max) | - | - | ± 10 | uA |
| Output Leakage Current | | I_{LO} | $V_{OUT}=0$ to V_{CC} (max) | - | - | ± 10 | uA |
| Input High Voltage | | V_{IH}^1 | - | $0.7 \times V_{CC}$ | - | $V_{CC} + 0.3$ | V |
| Input Low Voltage, All inputs | | V_{IL}^1 | - | -0.3 | - | $0.2 \times V_{CC}$ | V |
| Output High Voltage Level | | V_{OH} | $I_{OH}=-20\text{uA}$ | $0.7 \times V_{CC}$ | - | - | V |
| Output Low Voltage Level | | V_{OL} | $I_{OL}=1\text{mA}$ | - | - | $0.15 \times V_{CC}$ | V |

Note:

- V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to $V_{CC}+0.4V$ for durations of 20ns or less.
- Typical value are measured at $V_{CC}=3.3V$, $T_A=25^\circ\text{C}$. Not 100% tested.

Valid Block and Error Management

| Description | Requirement |
|---|----------------------------------|
| Minimum / Maximum number of valid block number of block | 1004 / 1024 |
| Bad block mark | Non FFh |
| Mark location | Column 2048 of page 0 and page 1 |

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

AC Test Condition

($T_A=0$ to 70°C , $V_{CC}=2.7\text{V}\sim 3.6\text{V}$)

| Parameter | Condition |
|--------------------------------|----------------------------------|
| Input Pulse Levels | $0.2V_{CC}$ to $0.8V_{CC}$ |
| Input Rise and Fall Times | Max: 2.4ns |
| Input and Output Timing Levels | $V_{CC}/2$ |
| Output Load | 1 TTL Gate and $C_L=15\text{pF}$ |

Capacitance

($T_A=25^\circ\text{C}$, $V_{CC}=3.3\text{V}$, $f=1.0\text{MHz}$)

| Item | Symbol | Test Condition | Min. | Max. | Unit |
|----------------------------|-----------|----------------------|------|------|------|
| Input / Output Capacitance | $C_{I/O}$ | $V_{IL} = 0\text{V}$ | - | 8 | pF |
| Input Capacitance | C_{IN} | $V_{IN} = 0\text{V}$ | - | 8 | pF |

Note: Capacitance is periodically sampled and not 100% tested.

Read / Program / Erase Timing Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|-------------------|------|------|------|-------|
| Average Program Time | t_{PROG} | - | 400 | 900 | us |
| Number of Partial Program Cycles in the Same Page | NOP | - | - | 4 | Cycle |
| Block Erase Time | t_{BERS} | - | 4 | 10 | ms |
| Data Transfer from Cell to Register with Internal ECC | t_{RD} | - | - | 100 | us |

General Timing Characteristic

| Parameter | Symbol | Min. | Max. |
|---|--------------------|---------|--------------|
| Clock frequency | f_C | | 104MHz |
| Hold# non-active hold time relative to SCK | t_{CD} | 4.5ns | |
| Hold# hold time relative to SCK | t_{CH} | 4.5ns | |
| Command deselect time | t_{CS} | 80ns | |
| CS# Setup Time | t_{CSS} | 5ns | |
| CS# Hold Time | t_{CSH} | 5ns | |
| The last valid Clock low to CS# high | t_{CSCL} | 5ns | |
| Output disable time | t_{DIS} | | 20ns |
| Hold# non-active setup time relative to SCK | t_{HC} | 4.5ns | |
| Hold# setup time relative to SCK | t_{HD} | 4.5ns | |
| Data input setup time | t_{SUDAT} | 2ns | |
| Data input hold time | t_{HDDAT} | 3ns | |
| Output hold time | t_{HO} | 1.5ns | |
| Hold# to output Hi-Z | t_{HZ} | | 7ns |
| Hold# to output Low-Z | t_{LZ} | | 7ns |
| Clock low to output valid | t_V | | 8ns |
| Clock high time | t_{WH} | 4.5ns | |
| Clock low time | t_{WL} | 4.5ns | |
| Clock rise time (slew rate) | t_{CRT} | 0.1V/ns | |
| Clock fall time (slew rate) | t_{CFT} | 0.1V/ns | |
| WP# setup time | t_{WPS} | 20ns | |
| WP# hold time | t_{WPH} | 100ns | |
| Resetting time during Idle/Read/Program/Erase | t_{RST} | | 5/5/10/500us |

Note: For first RESET condition after power up, t_{RST} will be 1ms MAX.

Technical Notes

Bus Operation

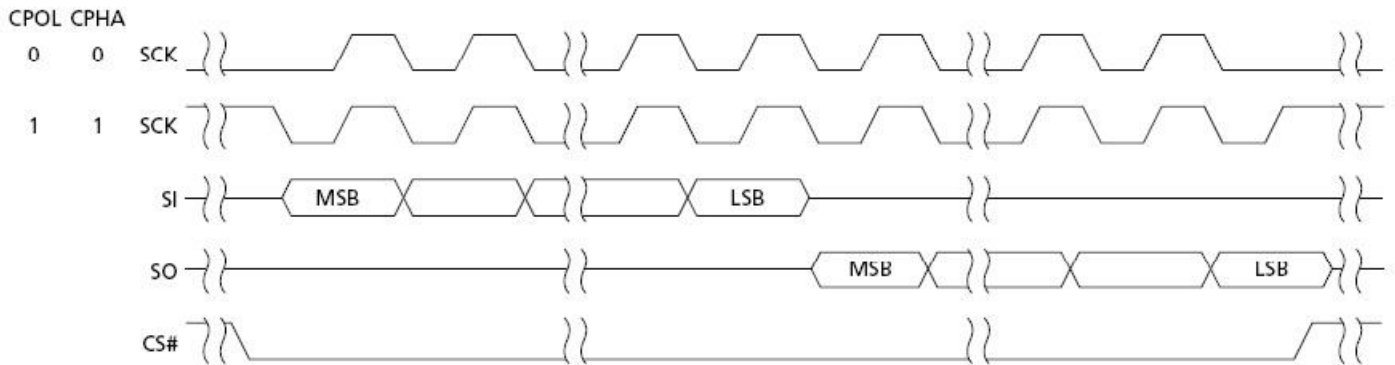
SPI NAND supports two SPI modes:

(Mode 0) CPOL (clock polarity) = 0, CPHA (clock phase) = 0

(Mode 3) CPOL=1, CPHA=1

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes. When CS# is high, keep SCK at V_{CC} (Mode 0) or V_{SS} (Mode 3). Do not begin toggling SCK until after CS# is driven LOW.

SPI Modes Timing



Feature Operations

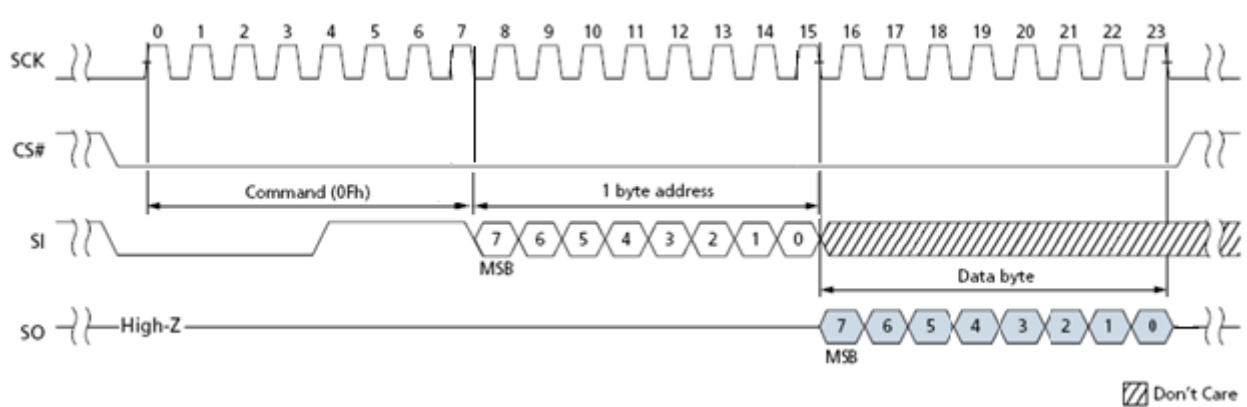
The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-Byte feature address to determine which feature is to be read or modified.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in Feature Setting Table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

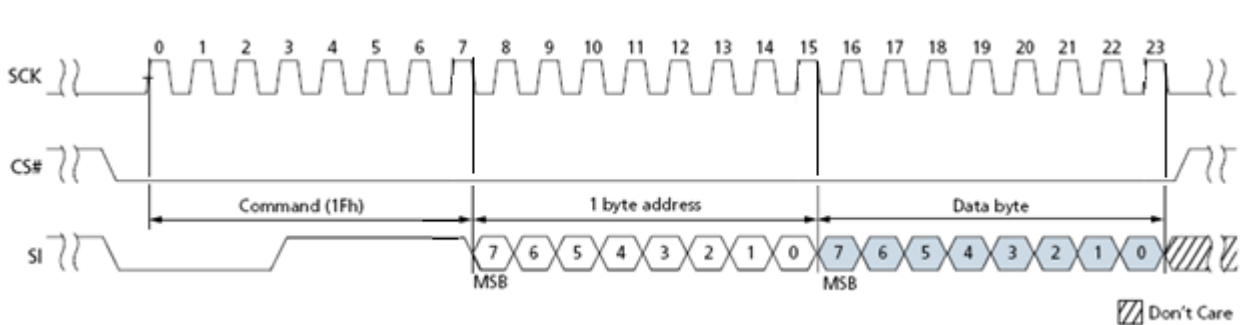
Feature Settings Table

| Register | Acronym | Address | Data Bits | | | | | | | |
|------------------------|---------|---------|-----------|----------|--------|----------|----------|----------|----------|----------|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Protection Register | PR | A0h | PRP0 | BP3 | BP2 | BP1 | BP0 | T/BP | WPE | PRP1 |
| Configuration Register | CR | B0h | OTP-P | OTP-E | PR-L | ECC-E | Reserved | Reserved | Reserved | Reserved |
| Status Register | SR | C0h | Reserved | Reserved | ECC_S1 | ECC_S0 | P_Fail | E_Fail | WEL | OIP |
| Output Driver Register | ODR | D0h | Reserved | DRV_S1 | DRV_S0 | Reserved | Reserved | Reserved | Reserved | Reserved |

GET FEATURE (0Fh) Timing



SET FEATURE (1Fh) Timing



Protection Register

Protection Register Setting Table

| A0h | Data Bits | | | | | | | |
|------------------|-------------------------------|-----------------|-----------------|-----------------|-----------------|----------------------|------------|-------------------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Definition | Protection Register Protect 0 | Block Protect 3 | Block Protect 2 | Block Protect 1 | Block Protect 0 | Top / Bottom Protect | WP# Enable | Protection Register Protect 1 |
| Shipment default | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

- Note:**
- All bits in A0h are volatile writable.
 - Once BP[3:0], T/B-P, and WPE bits are set correctly, PRP0 and PRP1 should both be set to "1" as well to allow PR-L bit being set to "1" to lock the protection in the PR (Protection Register) until next Power cycle.

Related Protection Bits of Protection Register Table

| Software Protection (Controller, X4 Program/ Read is enable) | | | | |
|---|---------|----------|---------|---|
| PRP0 (7) | WPE (1) | PRP1 (0) | WP# IO2 | Description |
| 0 | 0 | 0 | X | No WP# functionality, and WP# pin will always function as IO2 |
| 1 | 0 | 0 | 0 | PR cannot be changed, and WP# pin will function as IO2 for X4 operation |
| 1 | 0 | 0 | 1 | PR can be changed, and WP# pin will function as IO2 for X4 operation |
| 0 | 0 | 1 | X | Power Lock Down PR, and WP# pin will always function as IO2 |
| 1 | 0 | 1 | X | Set PR-L=1 is allowed, and PR is locked until next Power cycle, and WP# pin will always function as IO2 |
| Hardware Protection (System Circuit/ PCB layout, X4 Program/ Read is disable) | | | | |
| PRP0 (7) | WPE (1) | PRP1 (0) | WP# IO2 | Description |
| X | 1 | 0 | VCC | PR can be changed |
| 0 | 1 | 1 | VCC | Power Lock Down ⁽¹⁾ PR |
| 1 | 1 | 1 | VCC | Set PR-L=1 is allowed, and PR is locked until next Power cycle |
| X | 1 | X | GND | All Write operations are blocked, and entire device (Register, Array, and OTP area) is Read-only |

- Note:**
- PR means Protection Register.
 - When PRP1 = "1" and PRP0 = "0", a cycle of power-down to power-up will change the state to PRP1 = "0" and PRP0 = "0"

Block Protect Bits of Protection Register Table

| BP3 (6) | BP2 (5) | BP1 (4) | BP0 (3) | T/BP (2) | Protected Rows |
|---------|---------|---------|---------|----------|-------------------------------------|
| 0 | 0 | 0 | 0 | X | None; all unlocked |
| 0 | 0 | 0 | 1 | 0 | Upper 1/512 locked (BLK1022 & 1023) |
| 0 | 0 | 1 | 0 | 0 | Upper 1/256 locked |
| 0 | 0 | 1 | 1 | 0 | Upper 1/128 locked |
| 0 | 1 | 0 | 0 | 0 | Upper 1/64 locked |
| 0 | 1 | 0 | 1 | 0 | Upper 1/32 locked |
| 0 | 1 | 1 | 0 | 0 | Upper 1/16 locked |
| 0 | 1 | 1 | 1 | 0 | Upper 1/8 locked |
| 1 | 0 | 0 | 0 | 0 | Upper 1/4 locked |
| 1 | 0 | 0 | 1 | 0 | Upper 1/2 locked |
| 0 | 0 | 0 | 1 | 1 | Lower 1/512 locked (BLK0 & 1) |
| 0 | 0 | 1 | 0 | 1 | Lower 1/256 locked |
| 0 | 0 | 1 | 1 | 1 | Lower 1/128 locked |
| 0 | 1 | 0 | 0 | 1 | Lower 1/64 locked |
| 0 | 1 | 0 | 1 | 1 | Lower 1/32 locked |
| 0 | 1 | 1 | 0 | 1 | Lower 1/16 locked |
| 0 | 1 | 1 | 1 | 1 | Lower 1/8 locked |
| 1 | 0 | 0 | 0 | 1 | Lower 1/4 locked |
| 1 | 0 | 0 | 1 | 1 | Lower 1/2 locked |
| 1 | 0 | 1 | X | X | All locked |
| 1 | 1 | X | X | X | All locked |

Note:

1. X = don't care
2. Any Erase or Program command for the protected area will be ignored.

Configuration Register**Configuration Register Setting Table**

| B0h | Data Bits | | | | | | | |
|------------------|-------------------|---------------------------------|--------------------------|---------------------------|----------|----------|----------|----------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Definition | OTP Pages Protect | OTP Pages Enable ⁽¹⁾ | Protection Register Lock | ECC Enable ⁽²⁾ | Reserved | Reserved | Reserved | Reserved |
| Shipment default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

- Note:**
1. To Program/ Read OTP area, and Read Unique ID and Parameter Page, OTP-E must be set to “1”.
 2. 1-bit internal ECC for all READ and PROGRAM operations can be enabled (ECC enable = 1) or disabled (ECC enable = 0).
 3. Once BP[3:0], T/B-P, and WP-E bits are set correctly, PRP0 and PRP1 should both be set to “1” as well to allow PR-L bit being set to “1” to lock the protection in the PR (Protection Register) until next Power cycle.
 4. Bit6 and bit4 are volatile writable.

OTP State Bits of Configuration Register Table

| OTP Protect Bit (7) | OTP Enable Bit (6) | State |
|---------------------|--------------------|-------------------------------|
| 0 | 0 | Normal operation (read array) |
| 0 | 1 | Access OTP space |
| 1 | 0 | Not applicable |
| 1 | 1 | Lock the OTP area |

Status Register

Software can read status register during the NAND device operation by issuing GET FEATURE (0Fh) command, followed by the feature address C0h. The status register will output the status of the operation, refer to Status Register Setting Table, Bits of Status Register Table and ECC Status Bits of Status Register Table.

Status Register Setting Table

| C0h | Data Bits | | | | | | | |
|------------------|-----------|----------|-------------|-------------|--------------|------------|--------------------|-----------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Definition | Reserved | Reserved | ECC_Status1 | ECC_Status0 | Program_Fail | Erase_Fail | Write Enable Latch | Operation In Progress |
| Shipment default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits of Status Register Table

| Bit Name | Mode | Description |
|--|------|---|
| Program fail (Bit 3) | R | P_Fail is set to 1 as a program failure has occurred. P_Fail = 1 will also be set if the user attempts to program an invalid address or a locked region. P_Fail is set to 0 during the PROGRAM EXECUTE command sequence or the RESET command. |
| Erase fail (Bit 2) | R | E_Fail is set to 1 as an erase failure has occurred. E_Fail = 1 will also be set if the user attempts to erase a locked region, or if ERASE operation fails. E_Fail is set to 0 at the start of the BLOCK ERASE command sequence or the RESET command. |
| Write enable latch (Bit 1) | W | WEL must be set to 1 to indicate the current status of the write enable latch, prior to issuing PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing WRITE ENABLE command. WEL is disabled (WEL=0) by issuing the WRITE DISABLE command. |
| Operation in progress (Bit 0) | R | OIP is set to 1 when the device is busy; it means a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing. OIP is cleared to 0 as the interface is in ready state. |
| ECC_status1 (Bit 5) ECC_status0 (Bit 4) | R | ECC Status Bits of Status Register Table shows the ECCS definitions. ECC_S is set to 00h either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECC_S is invalid if ECC is disabled (via a SET FEATURE command to Bit 4 in OTP register). After power-up RESET, ECC_S is set to reflect the contents of block 0, page 0. |

ECC Status Bits of Status Register Table

| ECCS1 (5) | ECCS0 (4) | Description |
|-----------|-----------|--|
| 0 | 0 | No errors |
| 0 | 1 | 1-bit error detected and corrected |
| 1 | 0 | 2-bit or more than 2-bit errors detected and not corrected |
| 1 | 1 | Reserved |

Output Driver Register**Output Driver Register Setting Table**

| D0h | Data Bits | | | | | | | |
|-------------------------|-----------|------------------|------------------|----------|----------|----------|----------|----------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Definition | Reserved | Driver_Strength1 | Deiver_Strength0 | Reserved | Reserved | Reserved | Reserved | Reserved |
| Shipment default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

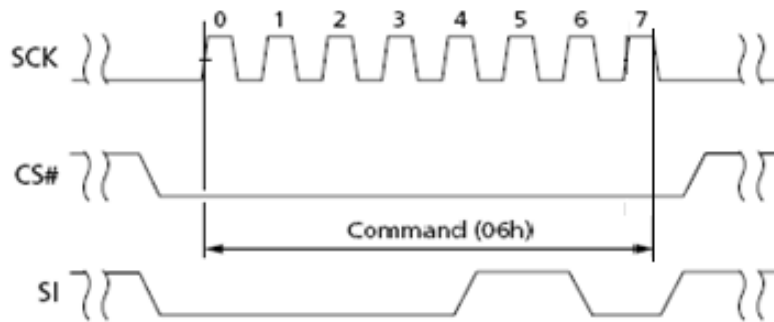
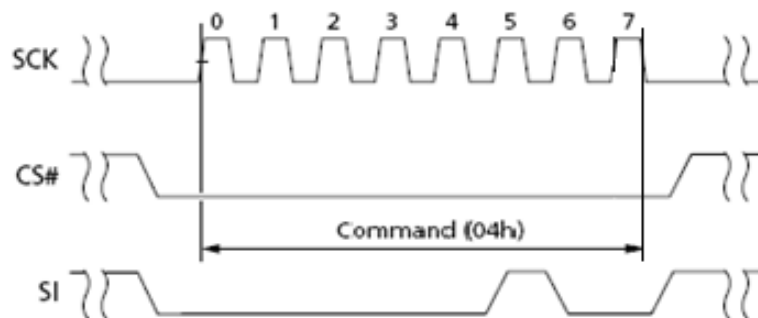
Driver Strength Bits of Output Driver Register Table

| DRV_S1 (6) | DRV_S0 (5) | Driver Strength |
|------------|------------|-----------------|
| 0 | 0 | 100 % |
| 0 | 1 | 75 % |
| 1 | 0 | 50 % |
| 1 | 1 | 25% |

Array Write Enable / Disable

The WRITE ENABLE (06h) command sets the WEL bit (in status register) to 1. This is required in the following WRITE operations that change the contents of the memory array: PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

Contrarily, the WRITE DISABLE (04h) command sets the WEL bit to 0. This disables PAGE PROGRAM, BLOCK ERASE, and OTP PROGRAM.

WRITE ENABLE (06h) Timing**WRITE DISABLE (04h) Timing**

Error Management

Mask Out Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ESMT. The information regarding the initial invalid blocks is called the initial invalid block information. Devices with initial invalid blocks have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block does not affect the performance of valid blocks because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid blocks via address mapping.

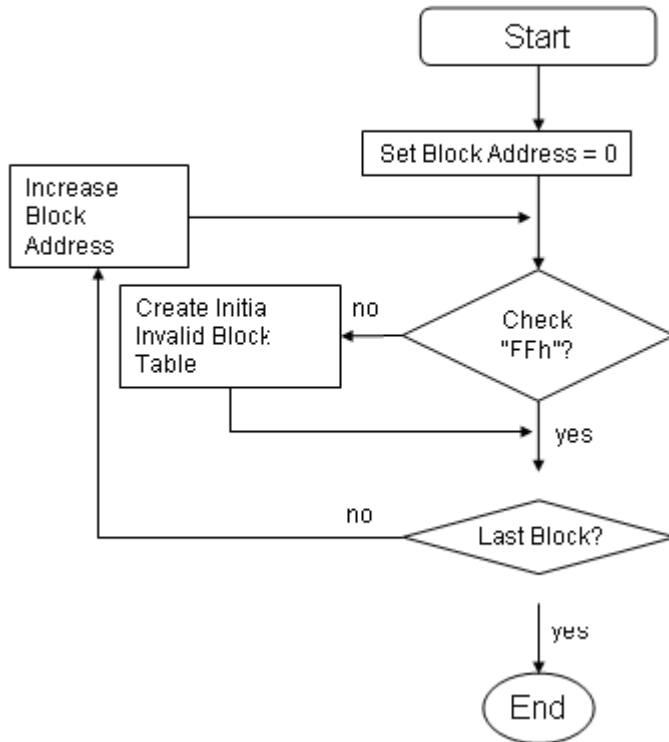
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

Identifying Initial Invalid Blocks

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. ESMT makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the 1st byte column address in the spare area.

Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Algorithm for Bad Block Scanning



Check "FFh" at the 1st Byte column address in the spare area of the 1st and 2nd page in the block.

```

For (i=0; i<Num_of_LUs; i++)
{
  For (j=0; j<Blocks_Per_LU; j++)
  {
    Defect_Block_Found=False;

    Read_Page(lu=i, block=j, page=0);
    If (Data[column=First_Byte_of_Spare_Area]!=FFh) Defect_Block_Found=True;

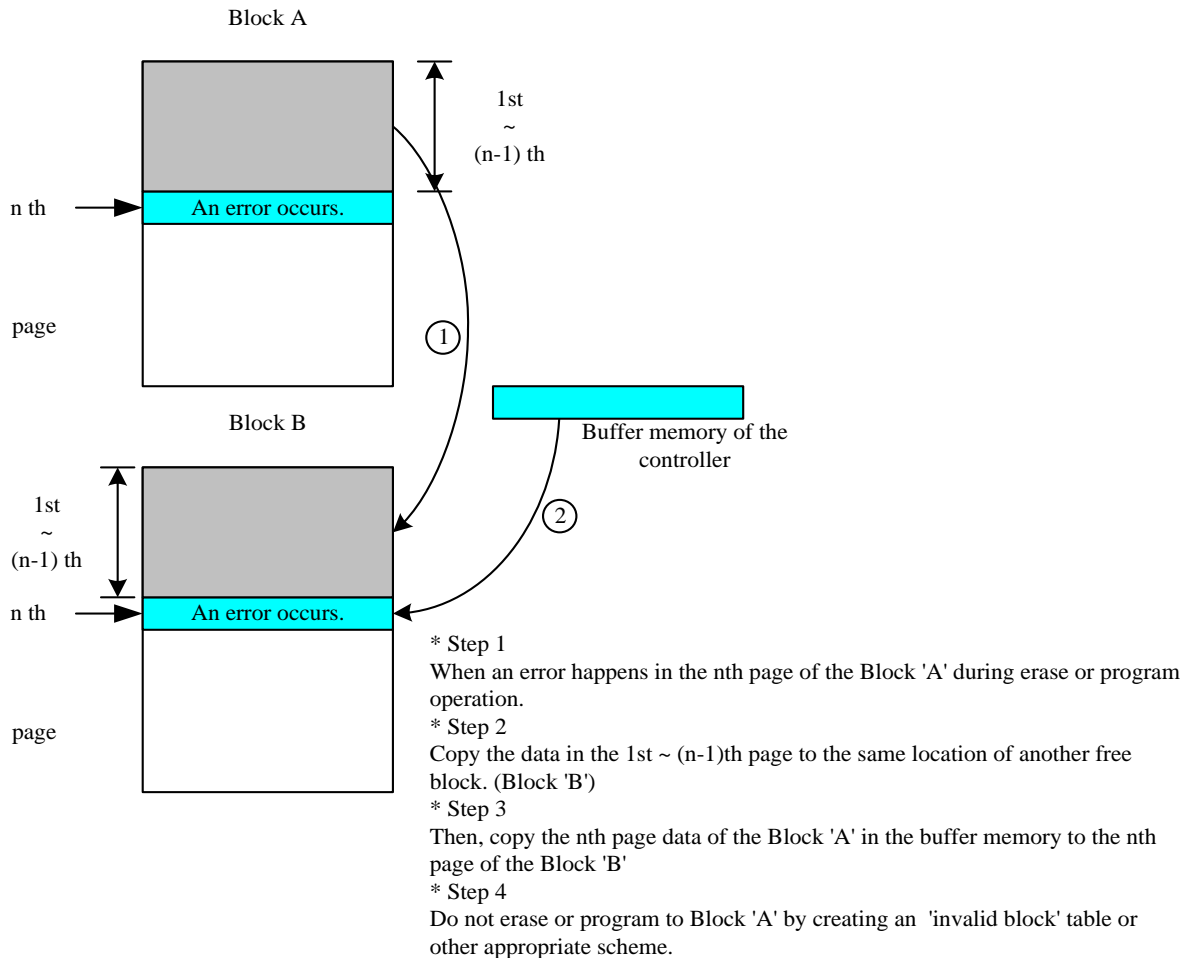
    Read_Page(lu=i, block=j, page=1);
    If (Data[column=First_Byte_of_Spare_Area]!=FFh) Defect_Block_Found=True;

    If (Defect_Block_Found) Mark_Block_as_Defective(lu=i, block=j);
  }
}
  
```

Block Replacement

Within its lifetime, number of invalid blocks may increase with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of failure after ERASE or PROGRAM in status register, block replacement should be done. Because PROGRAM status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.

In case of READ, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.



ECC Protection

ECC is enabled after device power-up, so the default PROGRAM and READ commands operate with internal ECC in the active state. During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page in array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register and only the corrected data is on the output bus.

ECC Protection Table

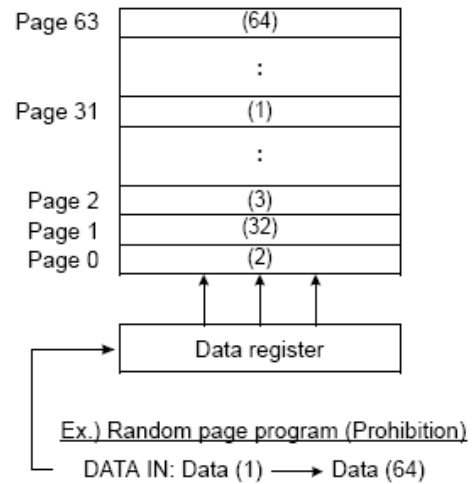
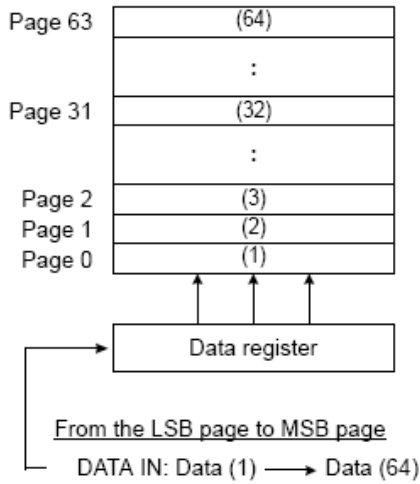
| Max Byte Address | Min Byte Address | ECC Protected | Area | Description |
|------------------|------------------|---------------|---------|-----------------------------|
| 1FFh (511) | 000h (0) | Yes | Main 0 | User data 0 ¹ |
| 3FFh (1023) | 200h (512) | Yes | Main 1 | User data 1 ¹ |
| 5FFh (1535) | 400h (1024) | Yes | Main 2 | User data 2 ¹ |
| 7FFh (2047) | 600h (1536) | Yes | Main 3 | User data 3 ¹ |
| 801h (2049) | 800h (2048) | No | | Reserved (Bad Block Marker) |
| 803h (2051) | 802h (2050) | No | Spare 0 | User Data II |
| 807h (2055) | 804h (2052) | Yes | Spare 0 | User Data I |
| 80Dh (2061) | 808h (2056) | Yes | | ECC for Main 0 |
| 80Fh (2063) | 80Eh (2062) | No | | ECC for Spare 0 |
| 811h | 810h | No | | Reserved |
| 813h | 812h | No | Spare 1 | User Data II |
| 817h | 814h | Yes | Spare 1 | User Data I |
| 81Dh | 818h | Yes | | ECC for Main 1 |
| 81Fh | 81Eh | No | | ECC for Spare 1 |
| 821h | 820h | No | | Reserved |
| 823h | 822h | No | Spare 2 | User Data II |
| 827h | 824h | Yes | Spare 2 | User Data I |
| 82Dh | 828h | Yes | | ECC for Main 2 |
| 82Fh | 82Eh | No | | ECC for Spare 2 |
| 831h | 830h | No | | Reserved |
| 833h | 832h | No | Spare 3 | User Data II |
| 837h | 834h | Yes | Spare 3 | User Data I |
| 83Dh | 838h | Yes | | ECC for Main 3 |
| 83Fh | 83Eh | No | | ECC for Spare 3 |

Note:

1. The user areas must be programmed within a single partial-page programming operation so the NAND Flash device can calculate the proper ECC bytes.
2. When internal ECC is enabled, these areas are prohibited to be programming.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



Operations and Timing Diagrams

Read Operations and Serial Output

The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURE command to read the status)
- 0Bh or 03h (READ FROM CACHE x1); 0Ch (x1) / 3Bh (x2); 3Ch (x2) / 6Bh (x4); 6Ch (x4)
- BBh (x2) TBD; BCh (x2) / EBh (x4) TBD; ECh (x4)

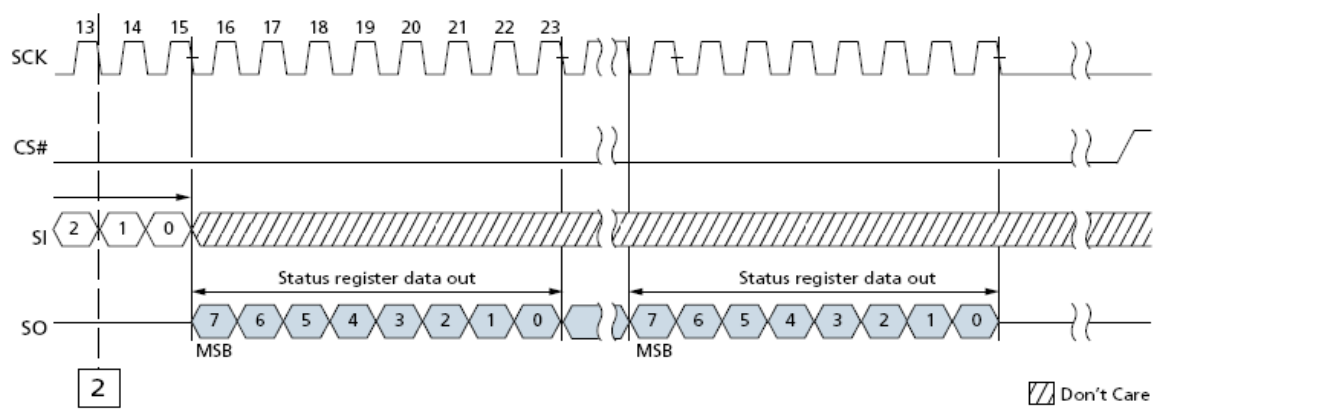
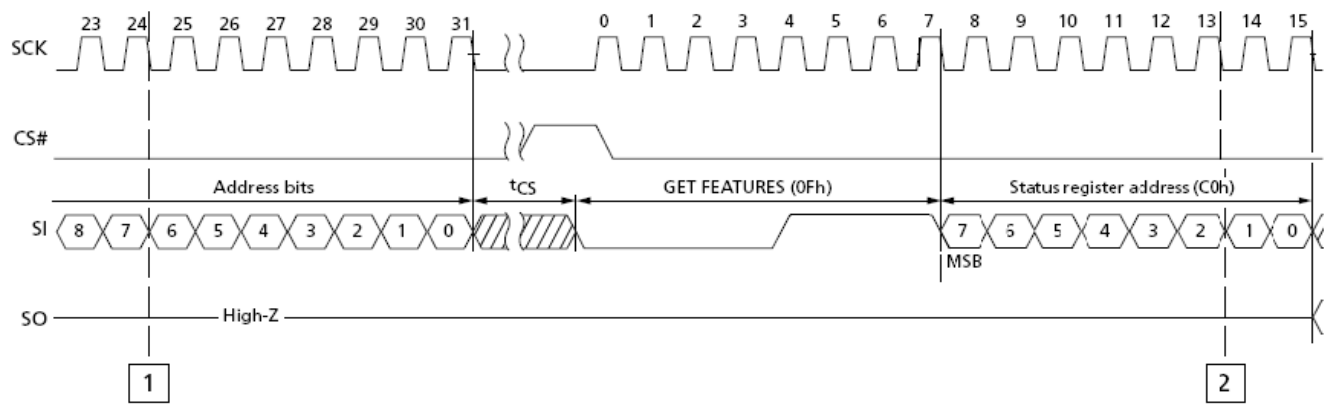
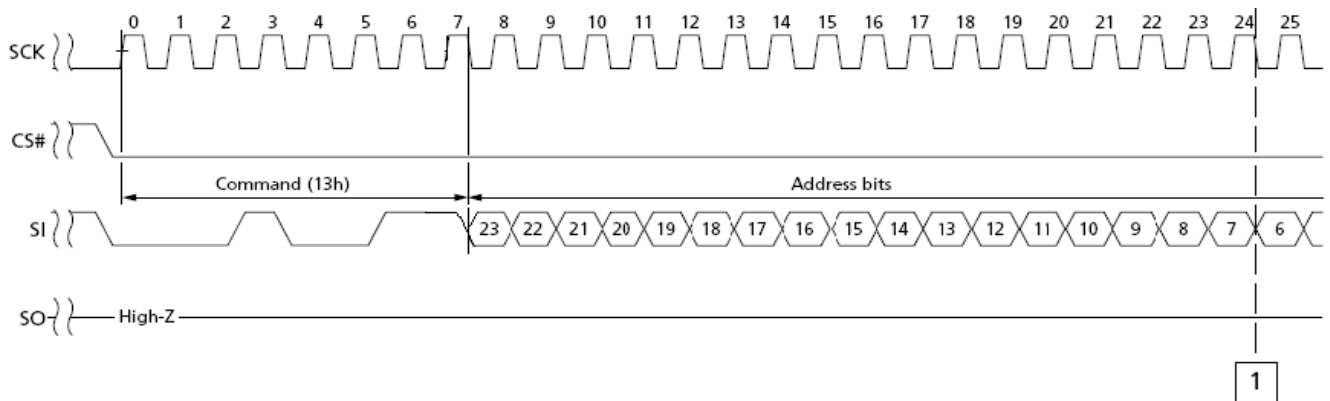
PAGE READ command requires 24-bit address with 8 dummy and a 16-bit row address. After row address is registered, the device starts the transfer from the main array to the cache register, and is busy for t_R time. During this time, GET FEATURE command can be issued to monitor the status of the operation. Following a status of successful completion, READ FROM CACHE command must be issued to read the data out of the cache.

READ FROM CACHE command requires 16-bit address with 4 dummy bits and a 12-bit column address for the starting byte. The starting byte can be 0 to 2011, but after the end of the cache register is reached, the data does not wrap around and SO goes to a Hi-Z state.

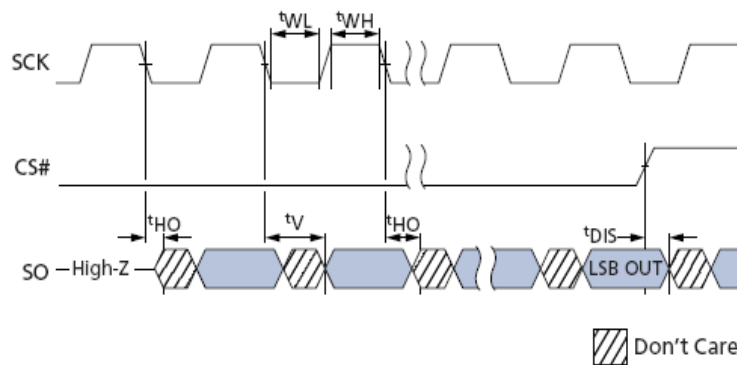
BBh and BCh command allow for improved random access while maintaining two IO pins: SI and SO. It is similar to 3Bh command but with the capability to input Column Address or dummy clocks two bits per clock.

The data output sequence will start from the location specified by the Column Address input and continue to the end of the Page. Once the last byte of data is output, both SI (SO0) and SO (SO1) will become Hi-Z.

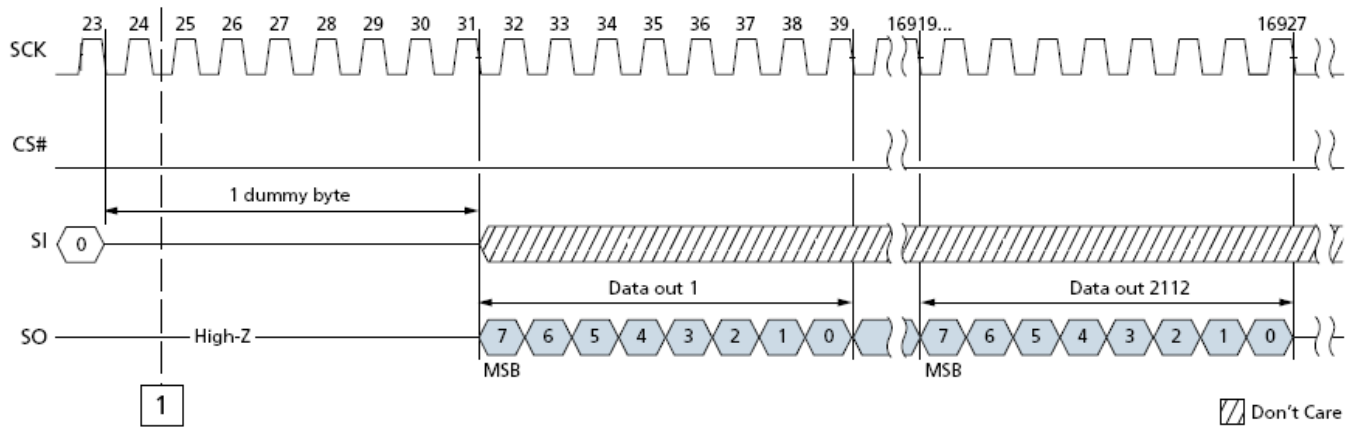
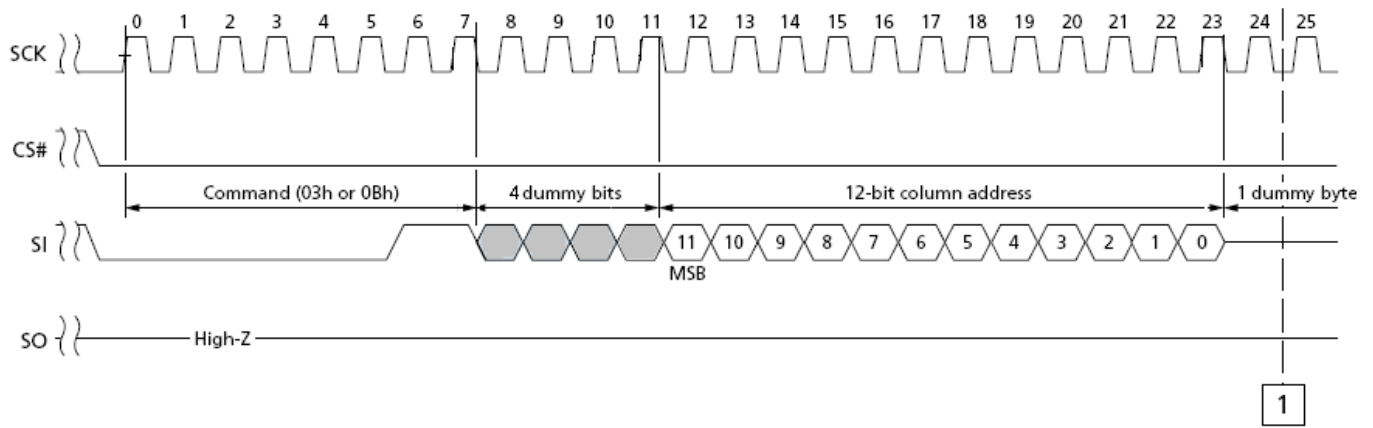
PAGE READ (13h) Timing



Serial Output Timing

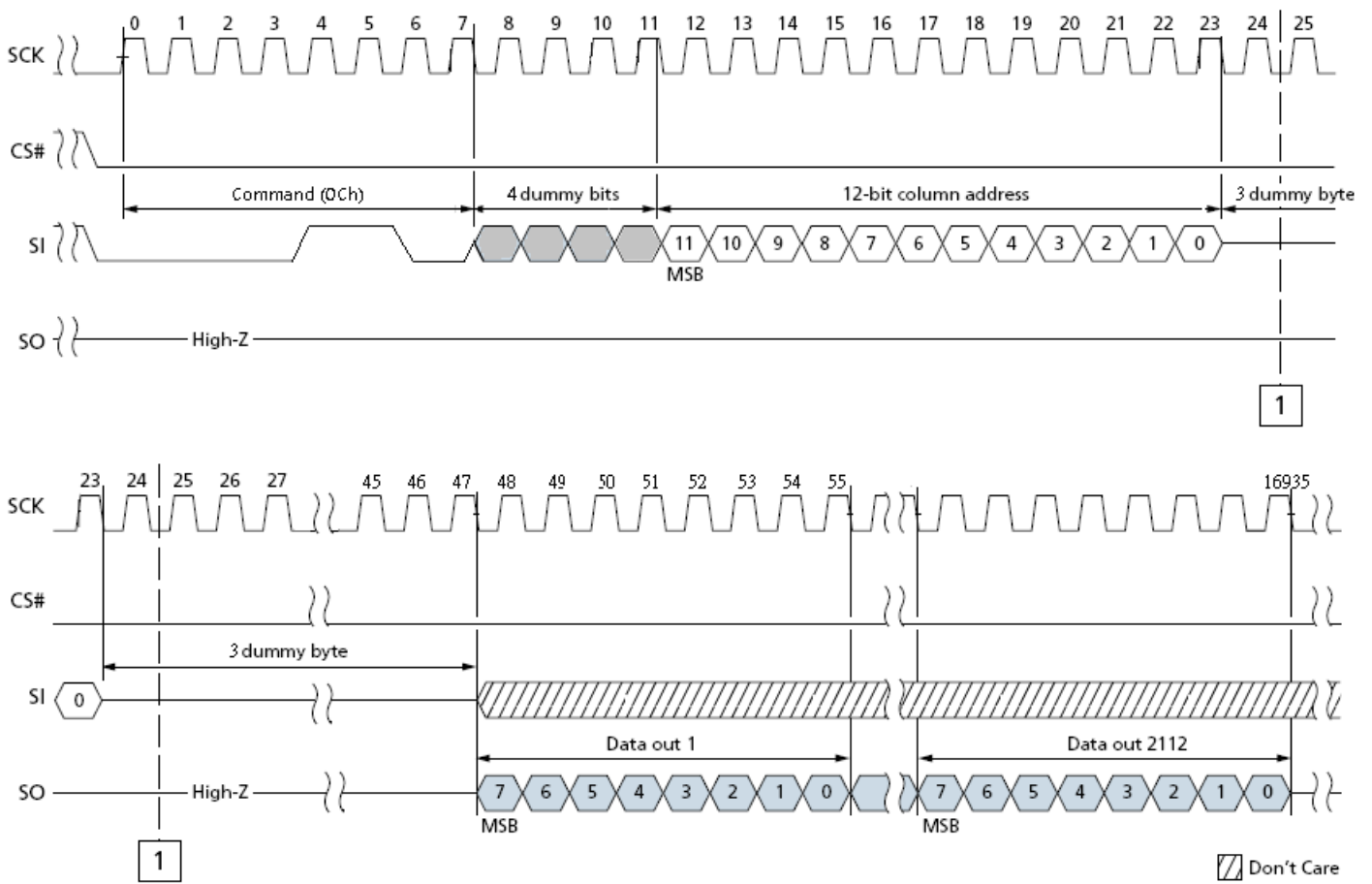


READ FROM CACHE (03h or 0Bh) Timing

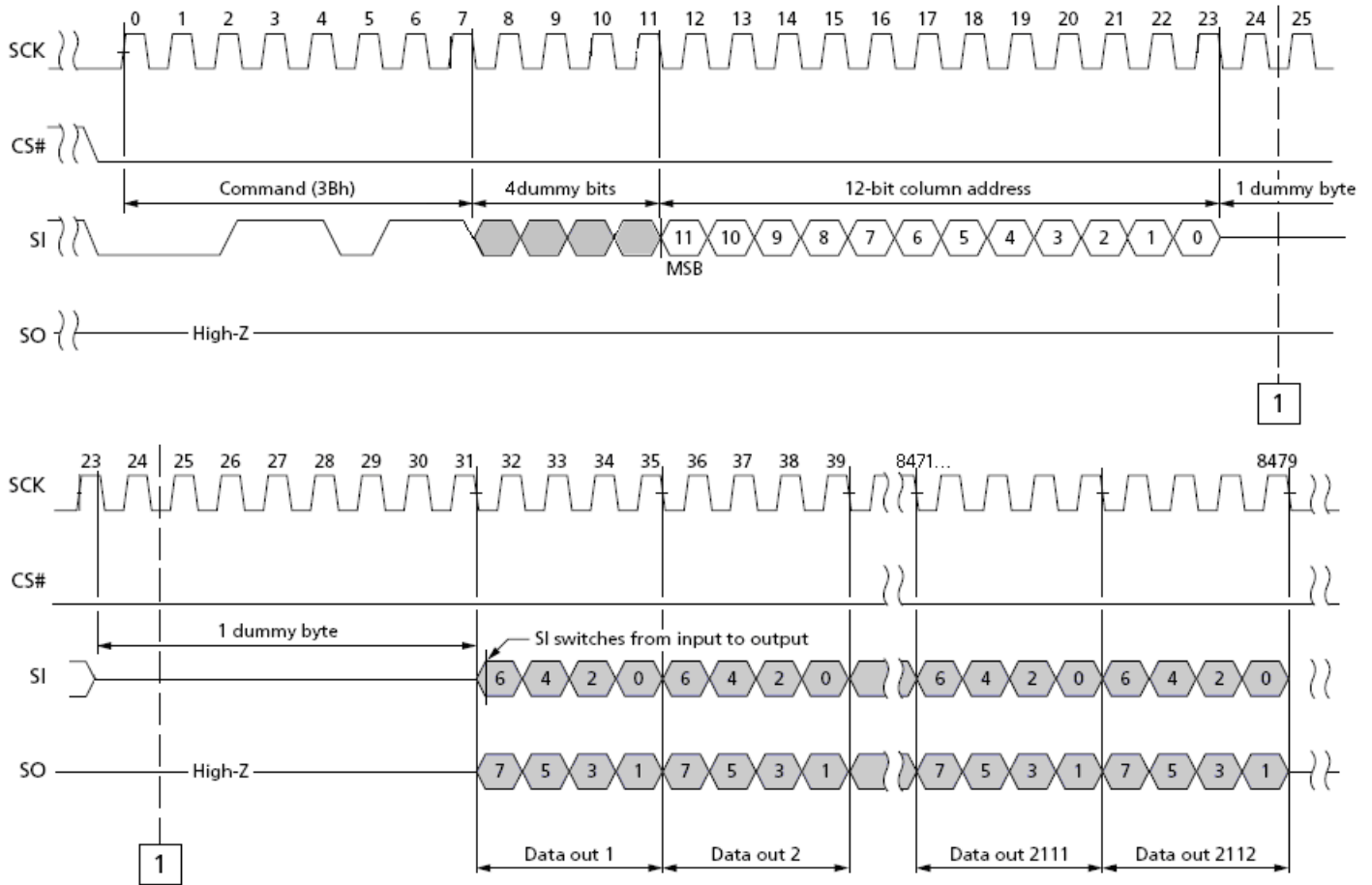


Don't Care

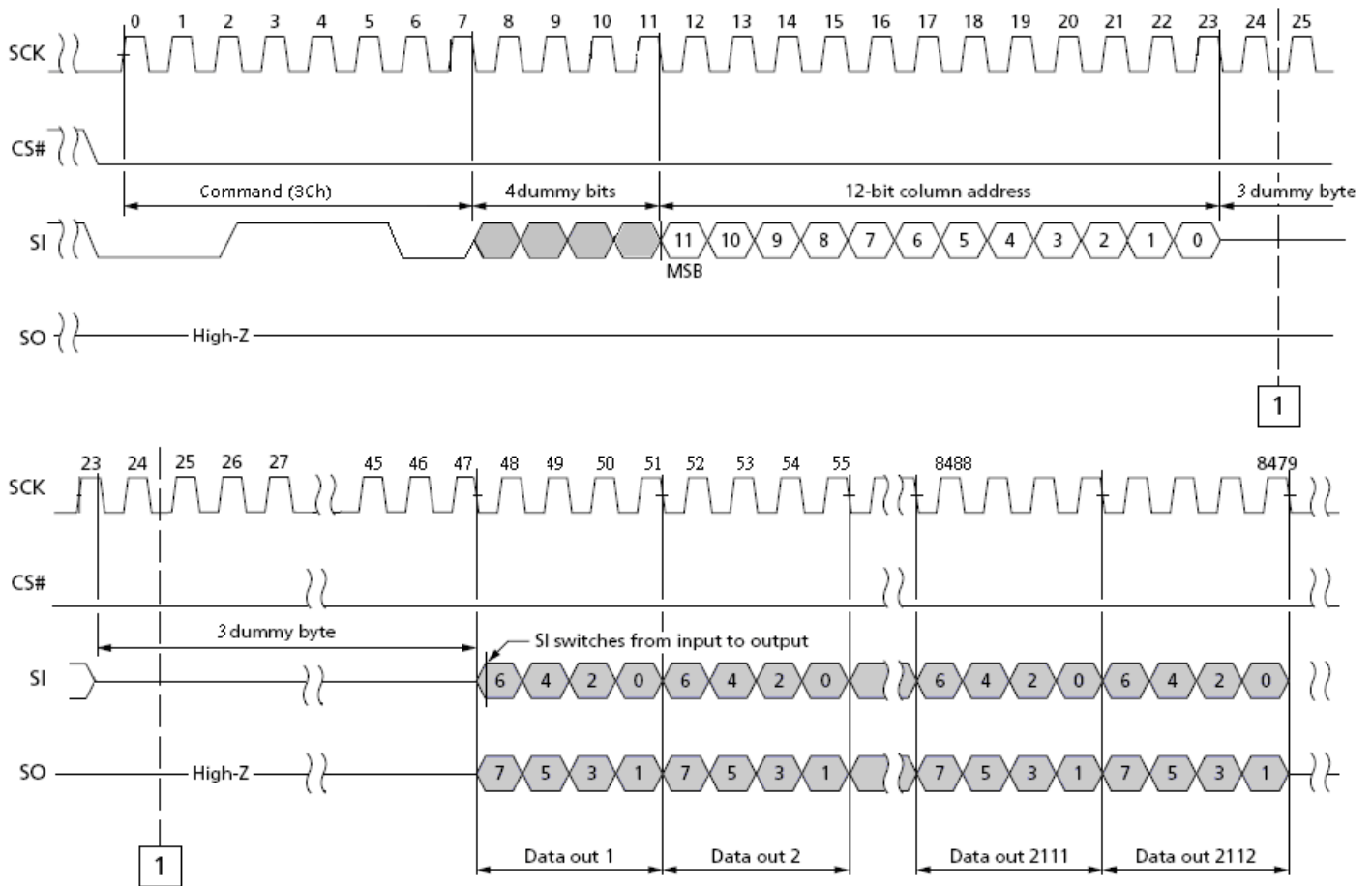
READ FROM CACHE with 4-Byte Address (0Ch) Timing



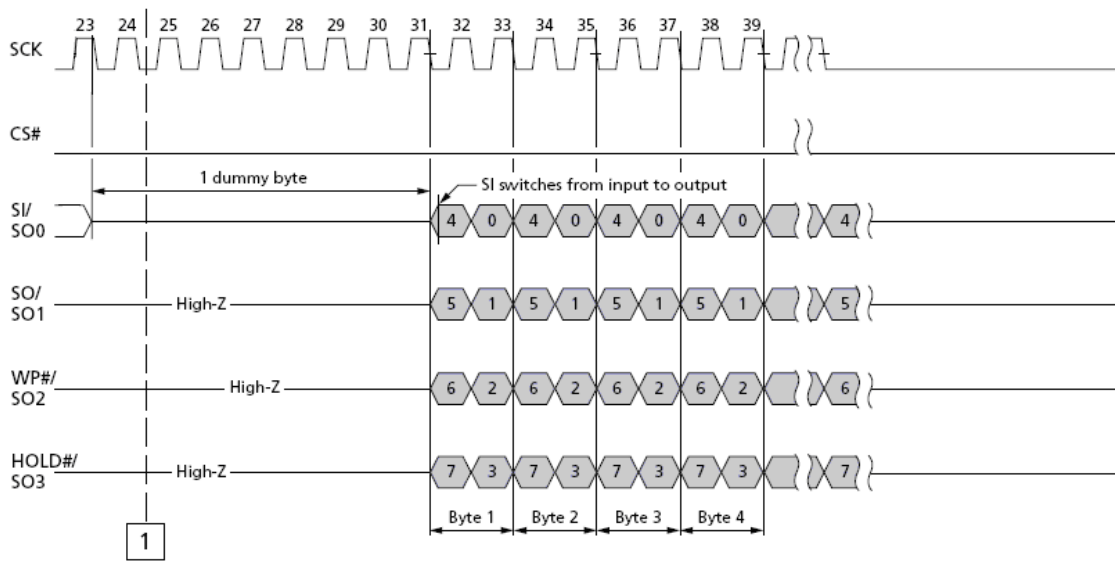
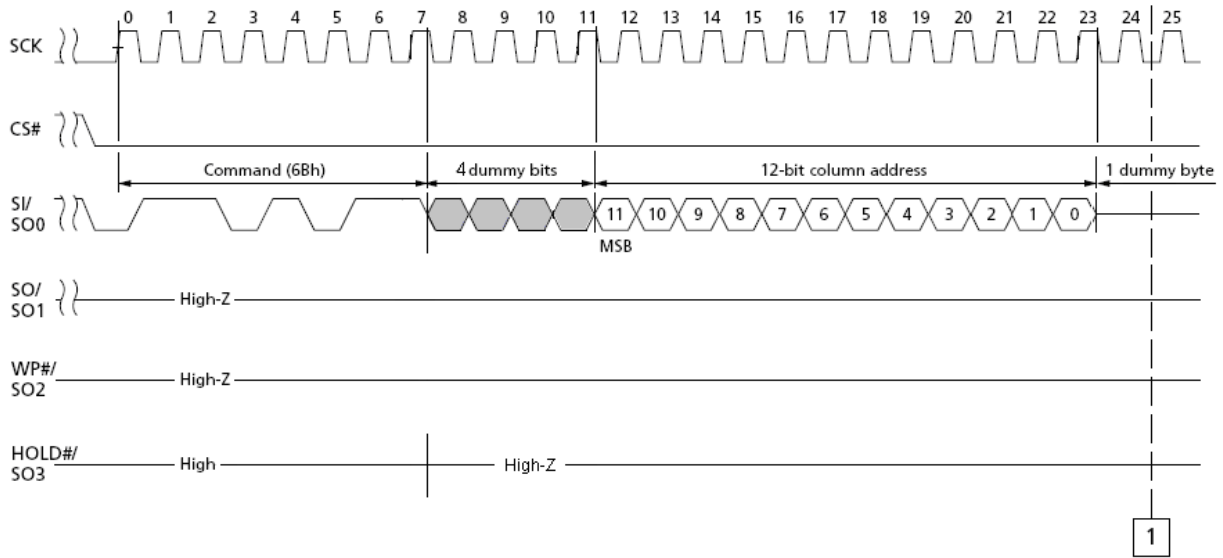
READ FROM CACHE x2 (3Bh) Timing



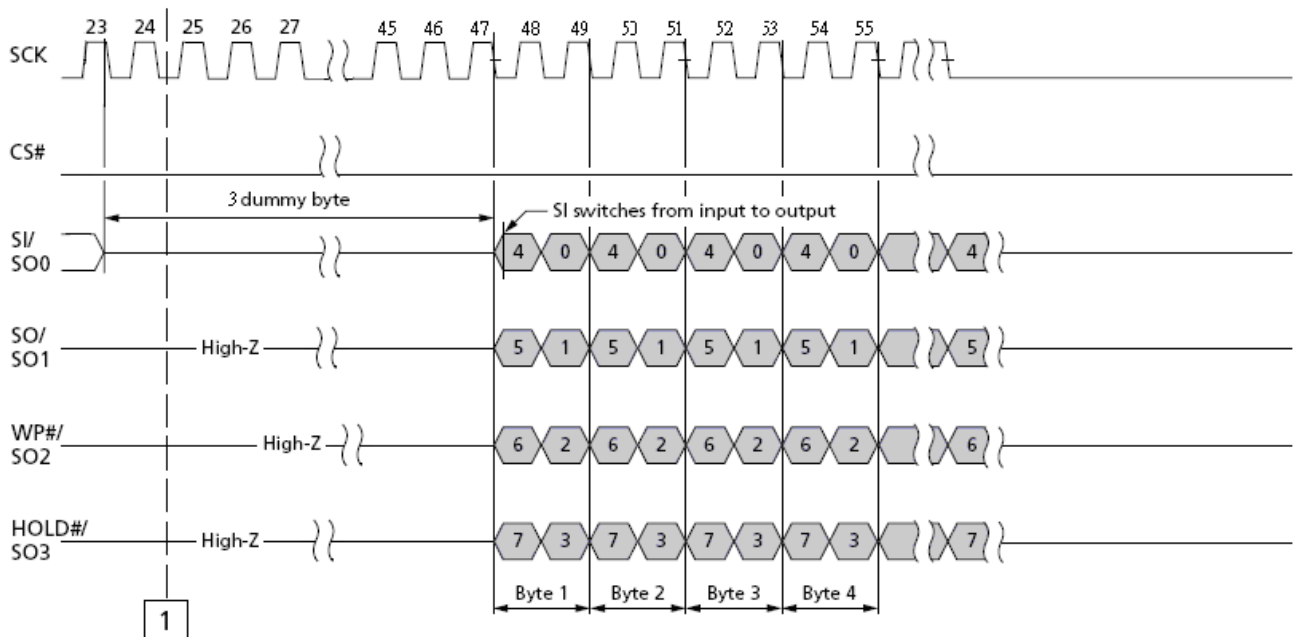
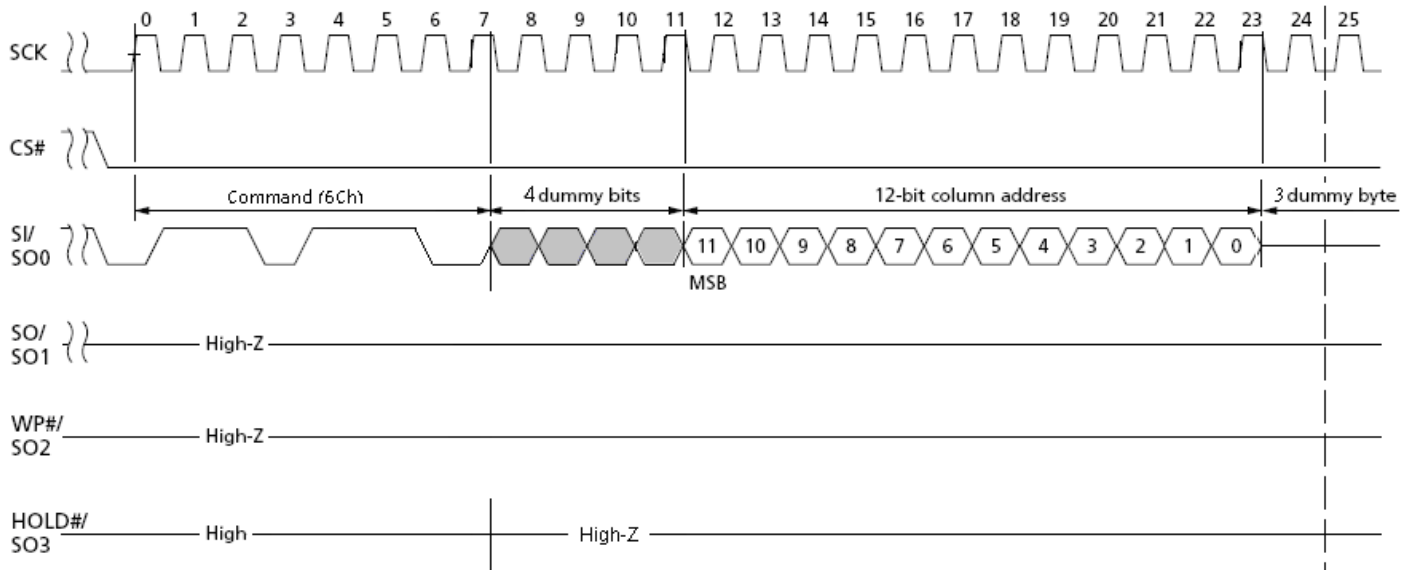
READ FROM CACHE x2 with 4-Byte Address (3Ch) Timing



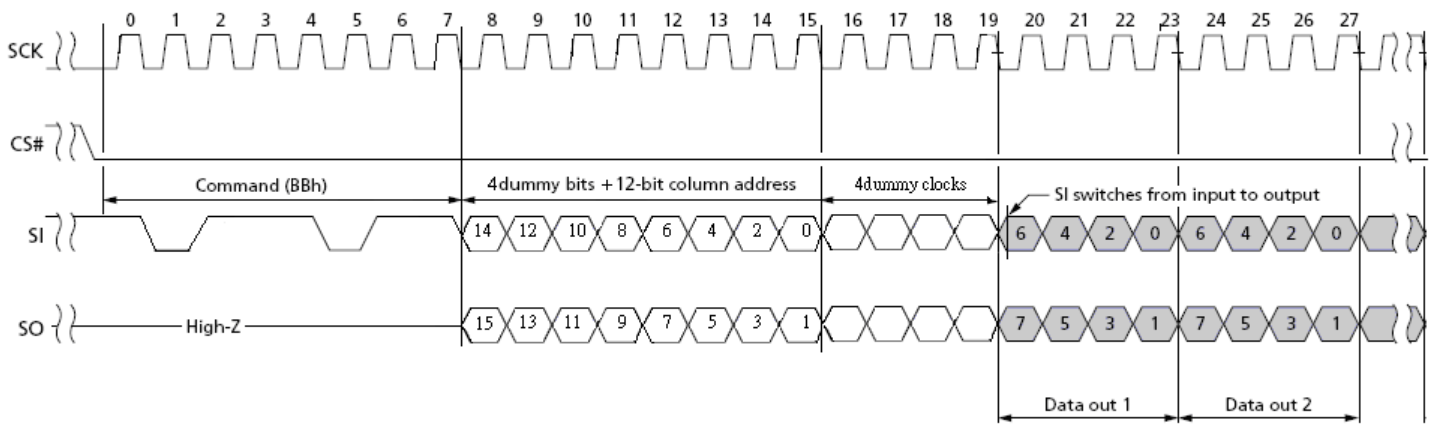
READ FROM CACHE x4 (6Bh) Timing



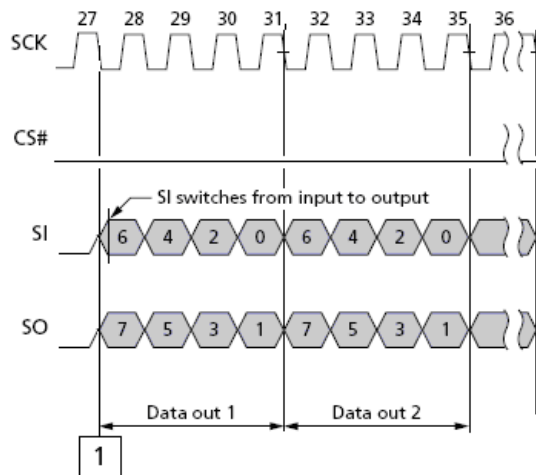
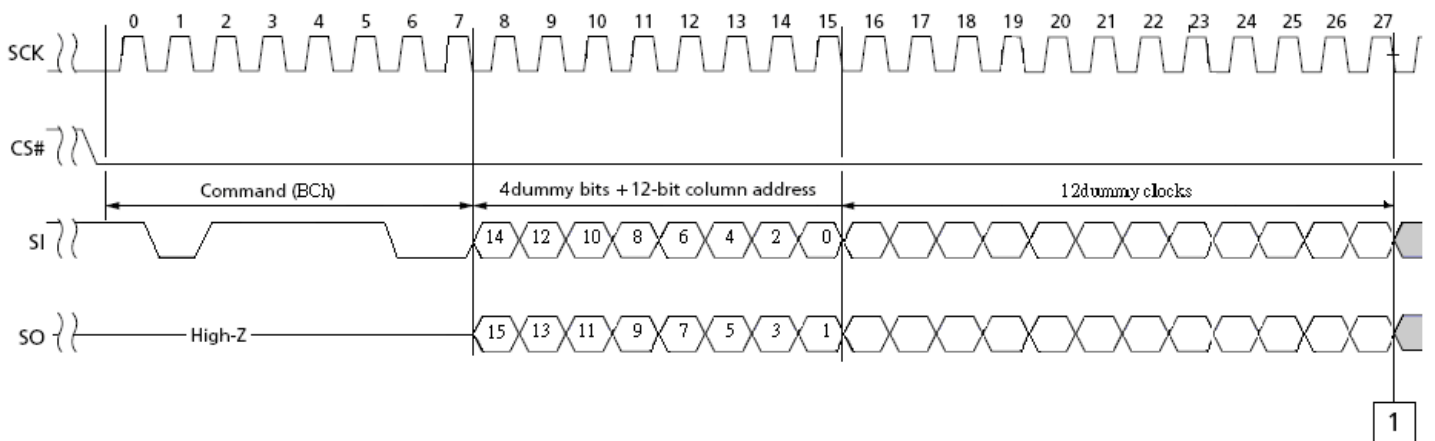
READ FROM CACHE x4 with 4-Byte Address (6Ch) Timing



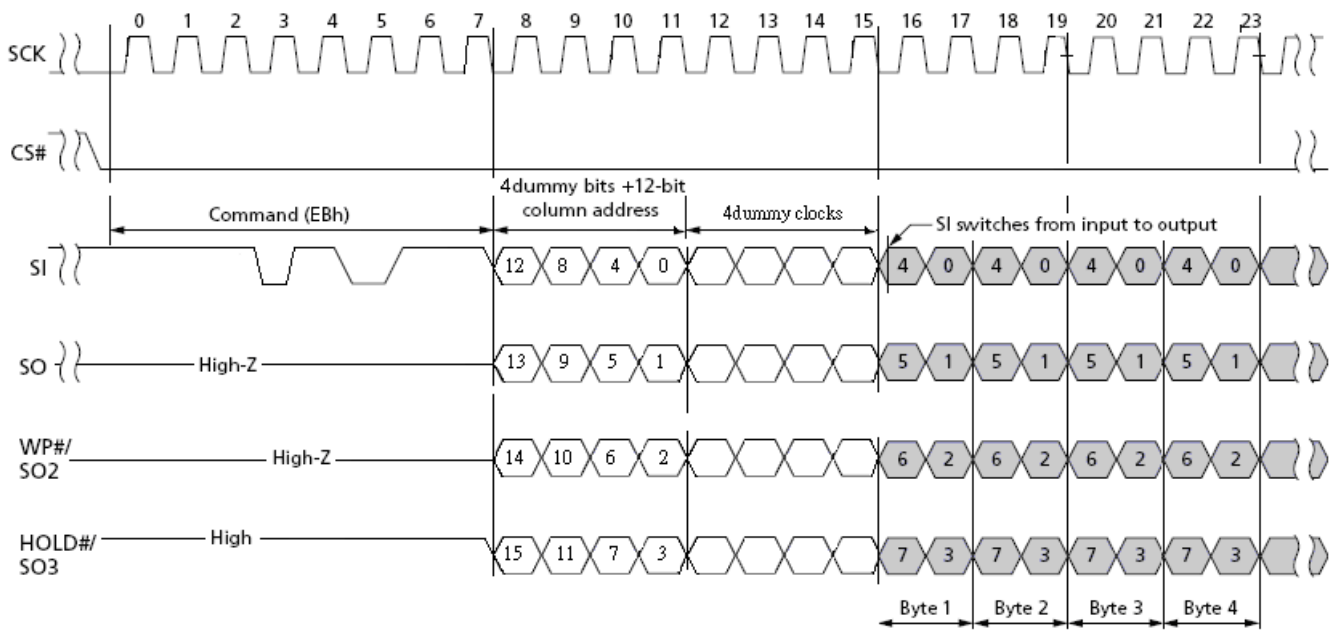
Fast Read X2 IO (BBh) Timing



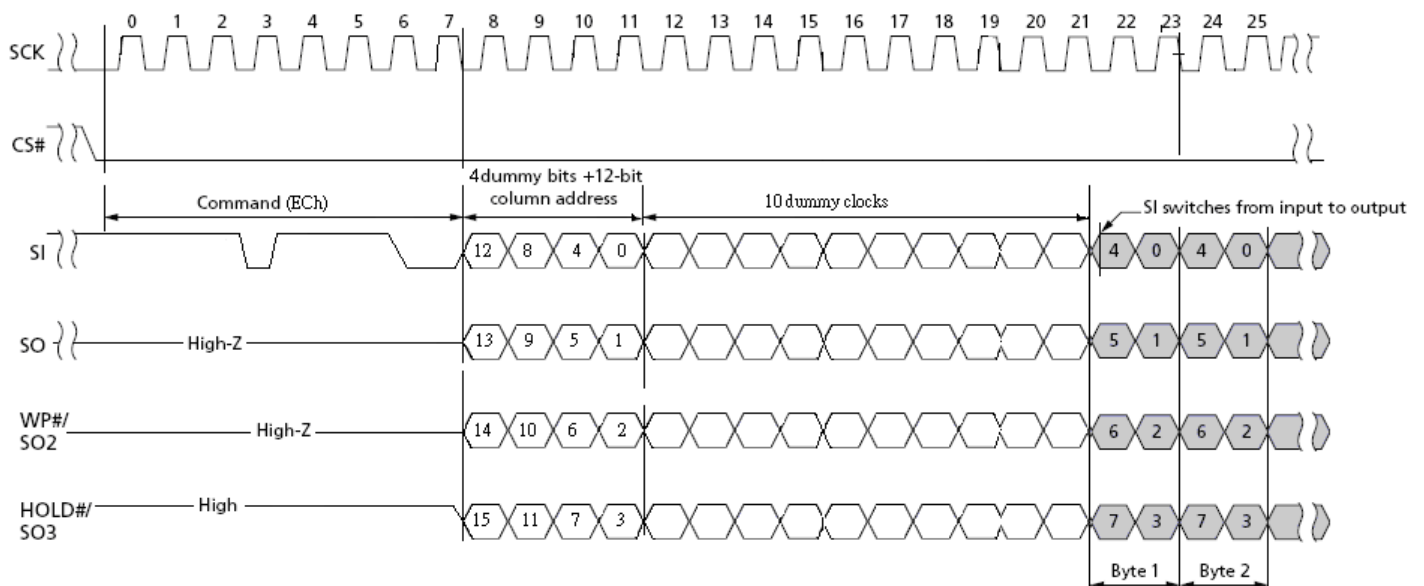
Fast Read X2 IO with 4Byte Address (BCh) Timing



Fast Read X4IO (EBh) Timing



Fast Read X4IO with 4Byte Address (ECh) Timing



Program Operations and Serial Input

Page Program

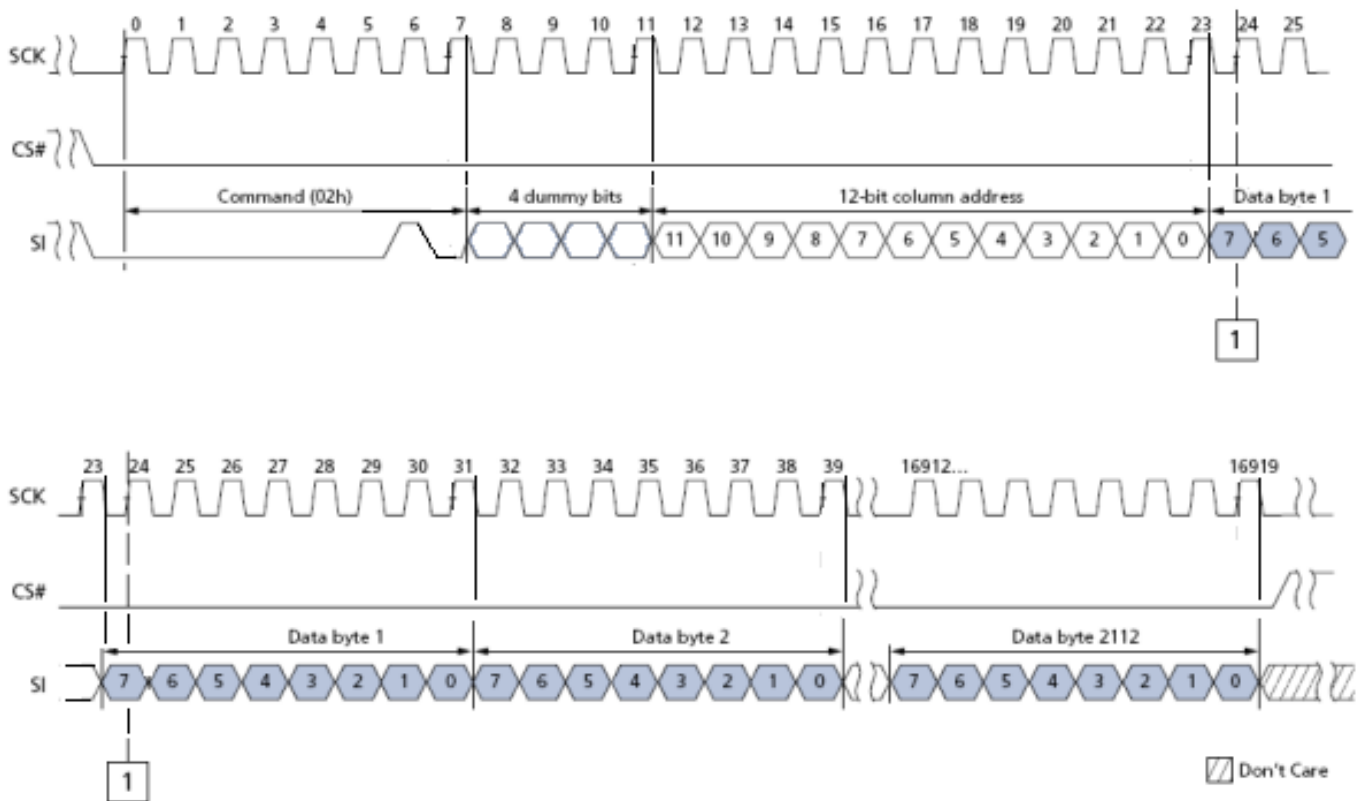
The command sequence is follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD x1) / 32h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

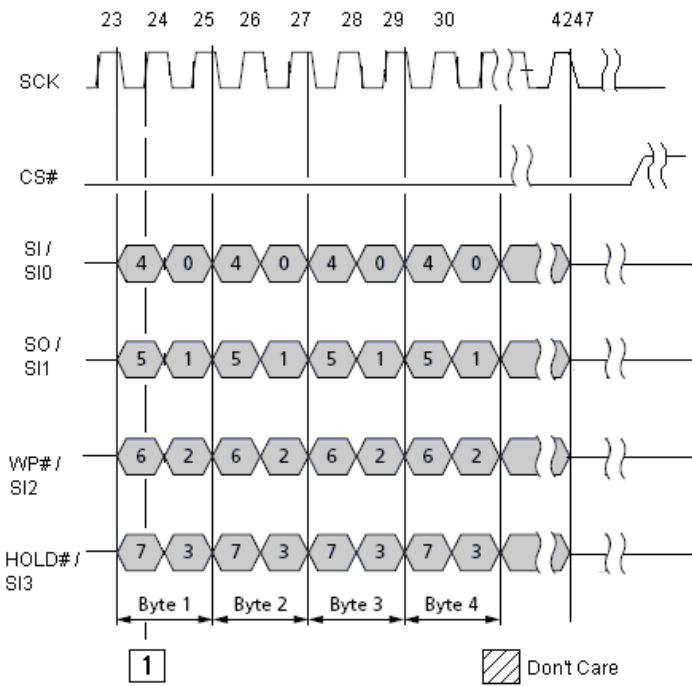
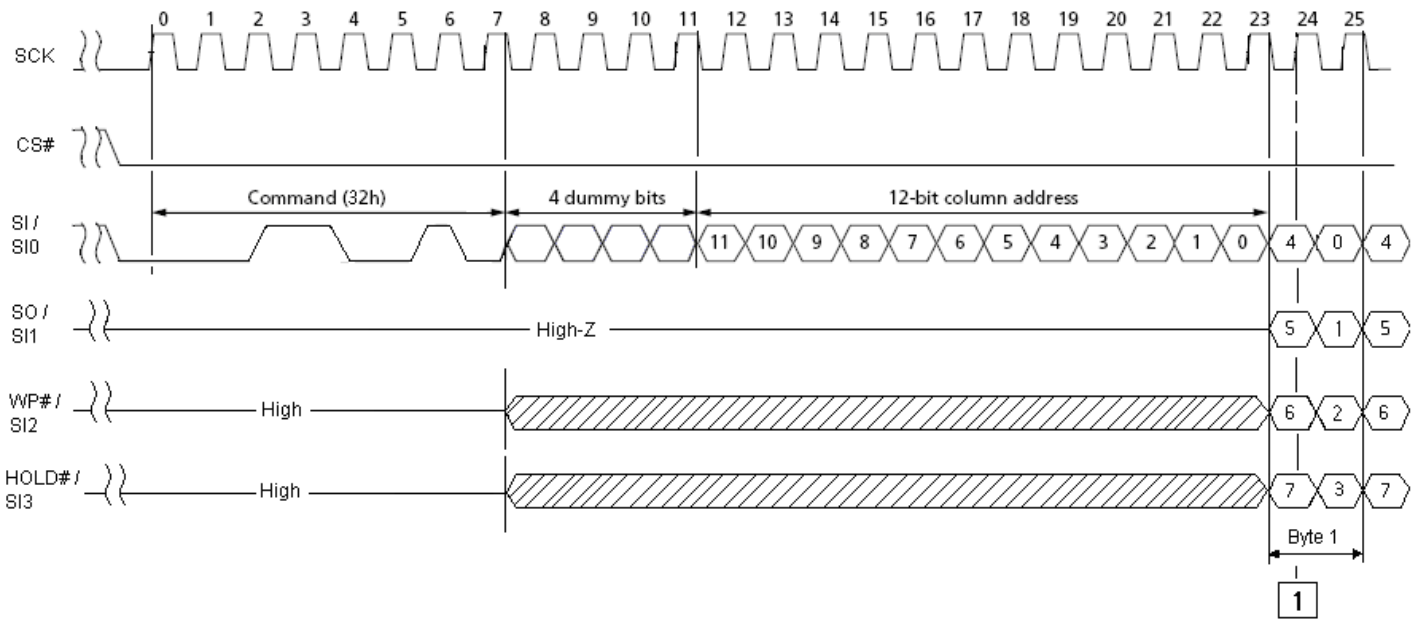
The page program operation sequence programs 1 byte to 2112 bytes of data within a page. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the program sequence is ignored. PROGRAM LOAD command requires 16-bit address with 4 dummy and a 12-bit column address, then the data bytes to be loaded into cache register. Only four partial page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register.

After the data is loaded, PROGRAM EXECUTE command must be issued to transfer the data from cache register to main array, and is busy for t_{PROG} time. PROGRAM EXECUTE command requires 24-bit address with 8 dummy bits and a 16-bit row address.

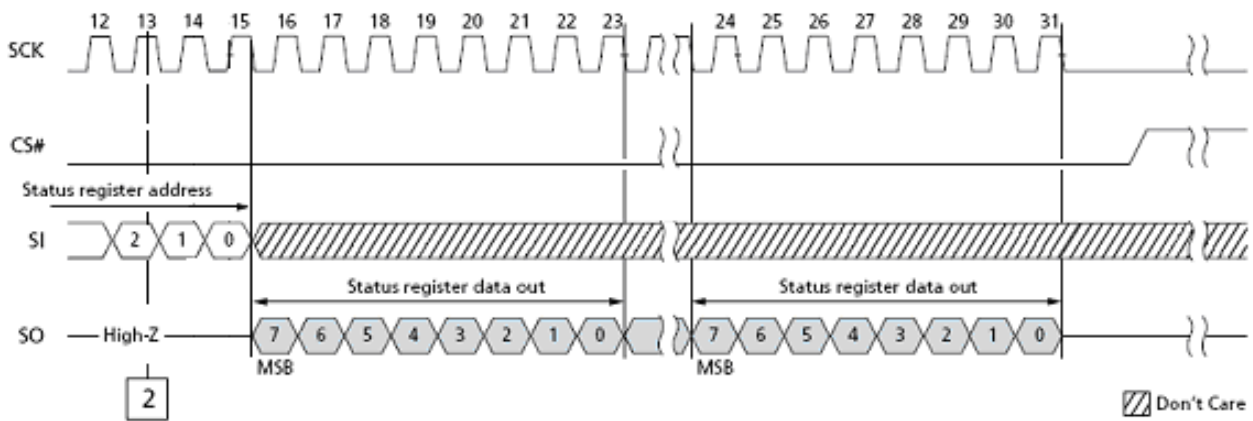
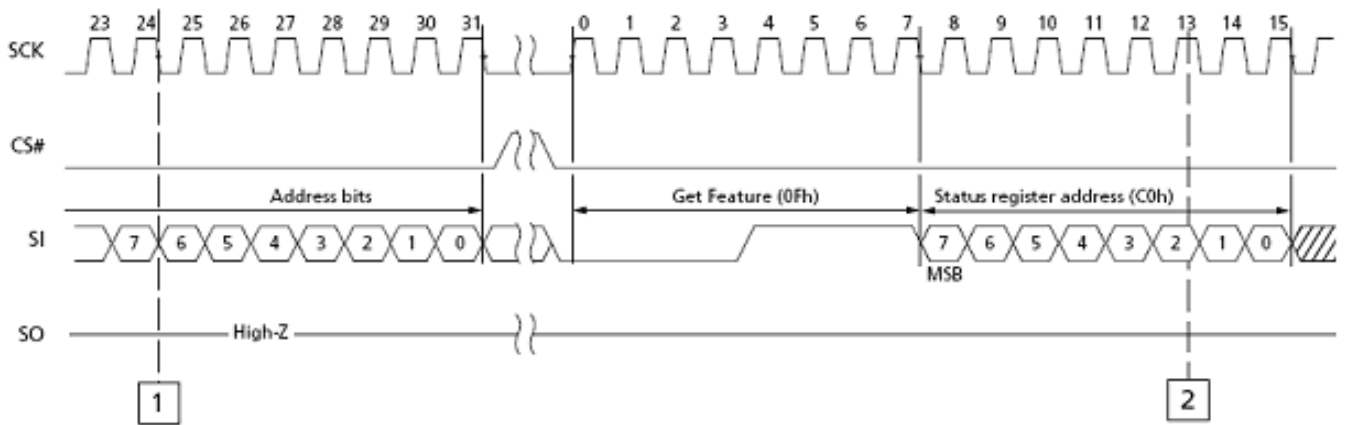
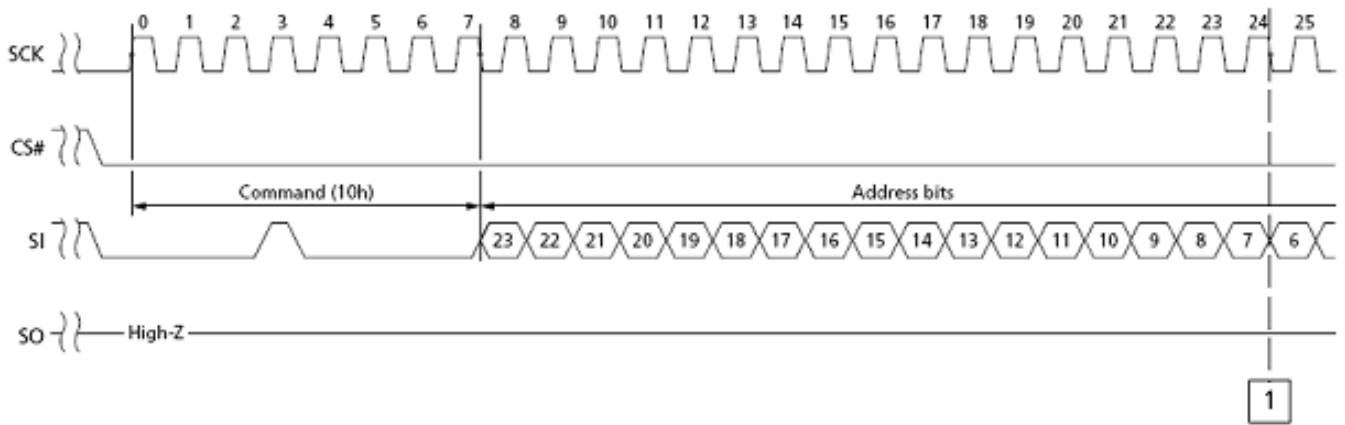
PROGRAM LOAD (02h) Timing



PROGRAM LOAD x4 (32h) Timing



PROGRAM EXECUTE (10h) Timing



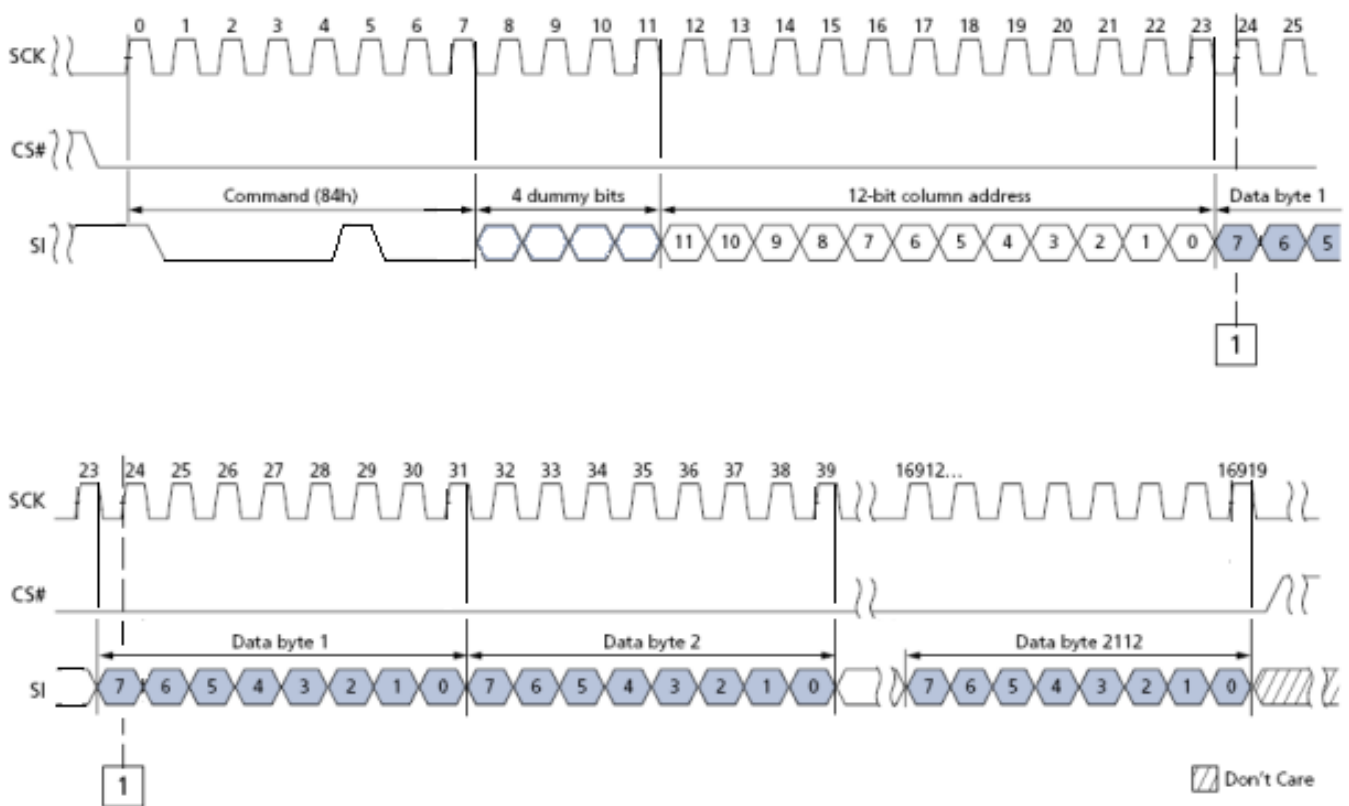
Random Data Program

The command sequence is follows:

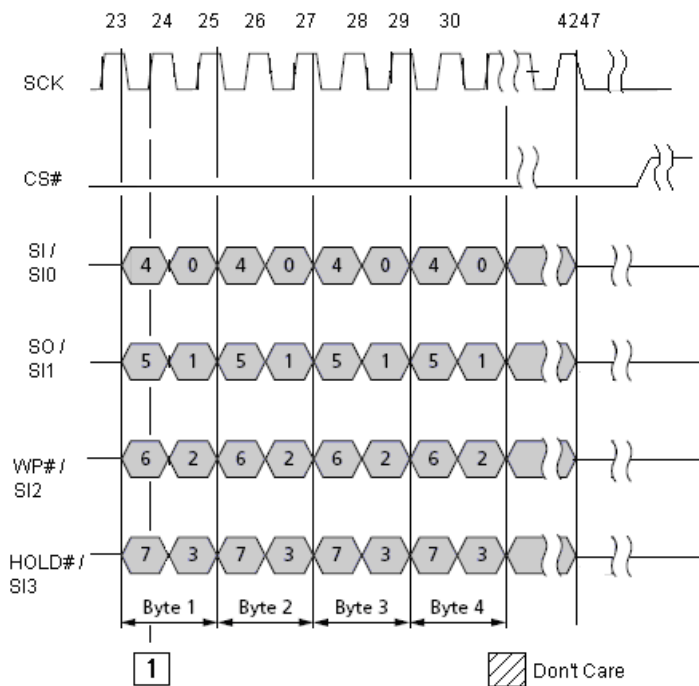
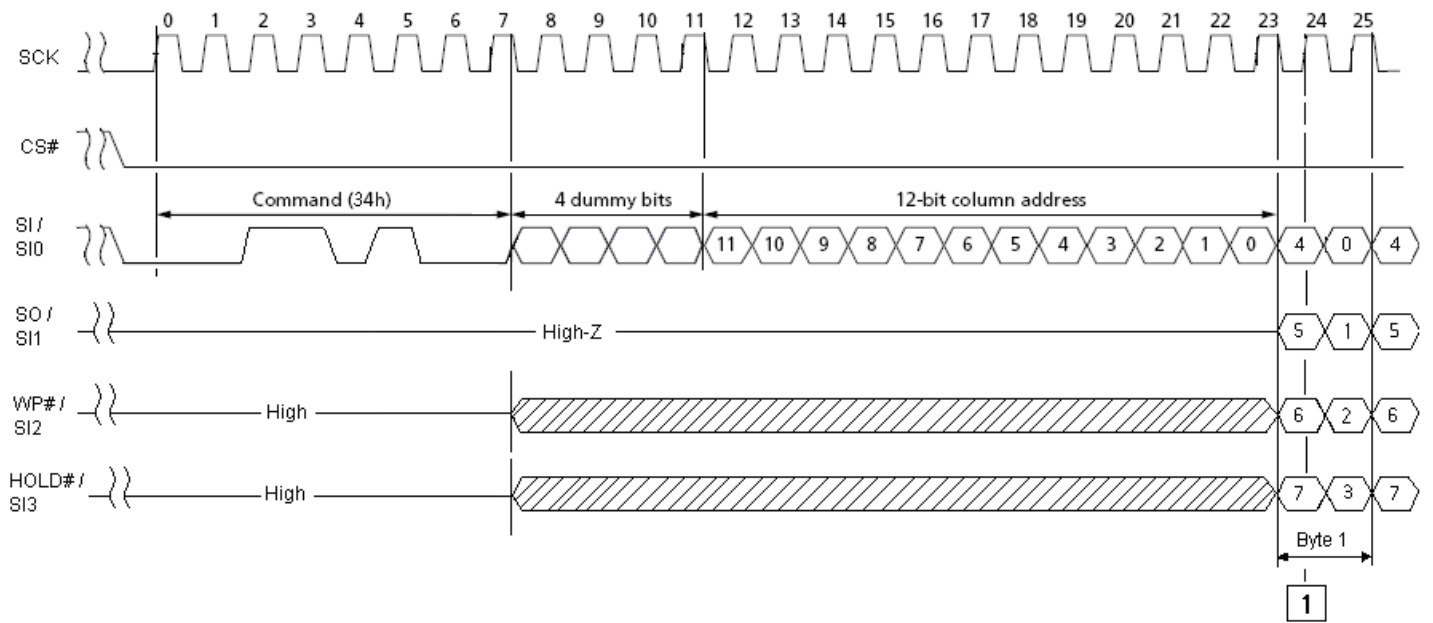
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The random data program operation sequence programs or replaces data in a page with existing data. PROGRAM LOAD RANDOM DATA command requires 16-bit address with 4 dummy bits and a 12-bit column address. New data is loaded in the column address provided. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA command must be issued with a new column address. After the data is loaded, PROGRAM EXECUTE command can be issued to start the programming operation.

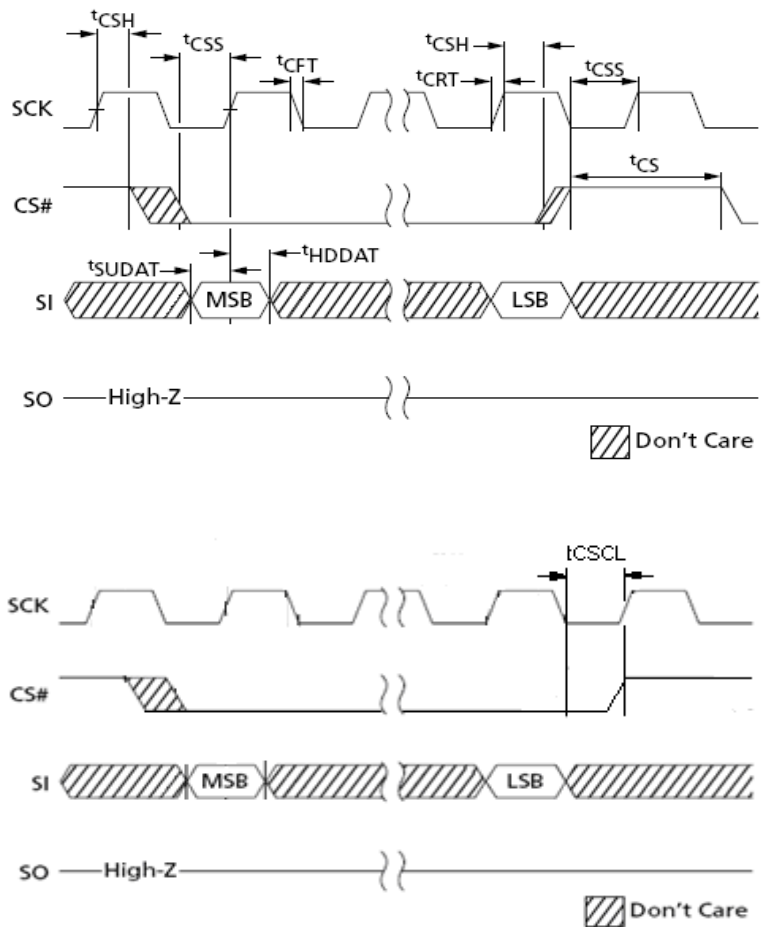
PROGRAM LOAD RANDOM DATA (84h) Timing



PROGRAM LOAD RANDOM DATA x4 (34h) Timing



Serial Input and t_{CSCL} Timing



Internal Data Move

The command sequence is follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA x1) / 34h (x4); this is OPTIONAL in sequence.
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

The INTERNAL DATA MOVE operation sequence programs or replaces data in a page with existing data. Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. PAGE READ command must be followed with a WRITE ENABLE command to change the contents of memory array.

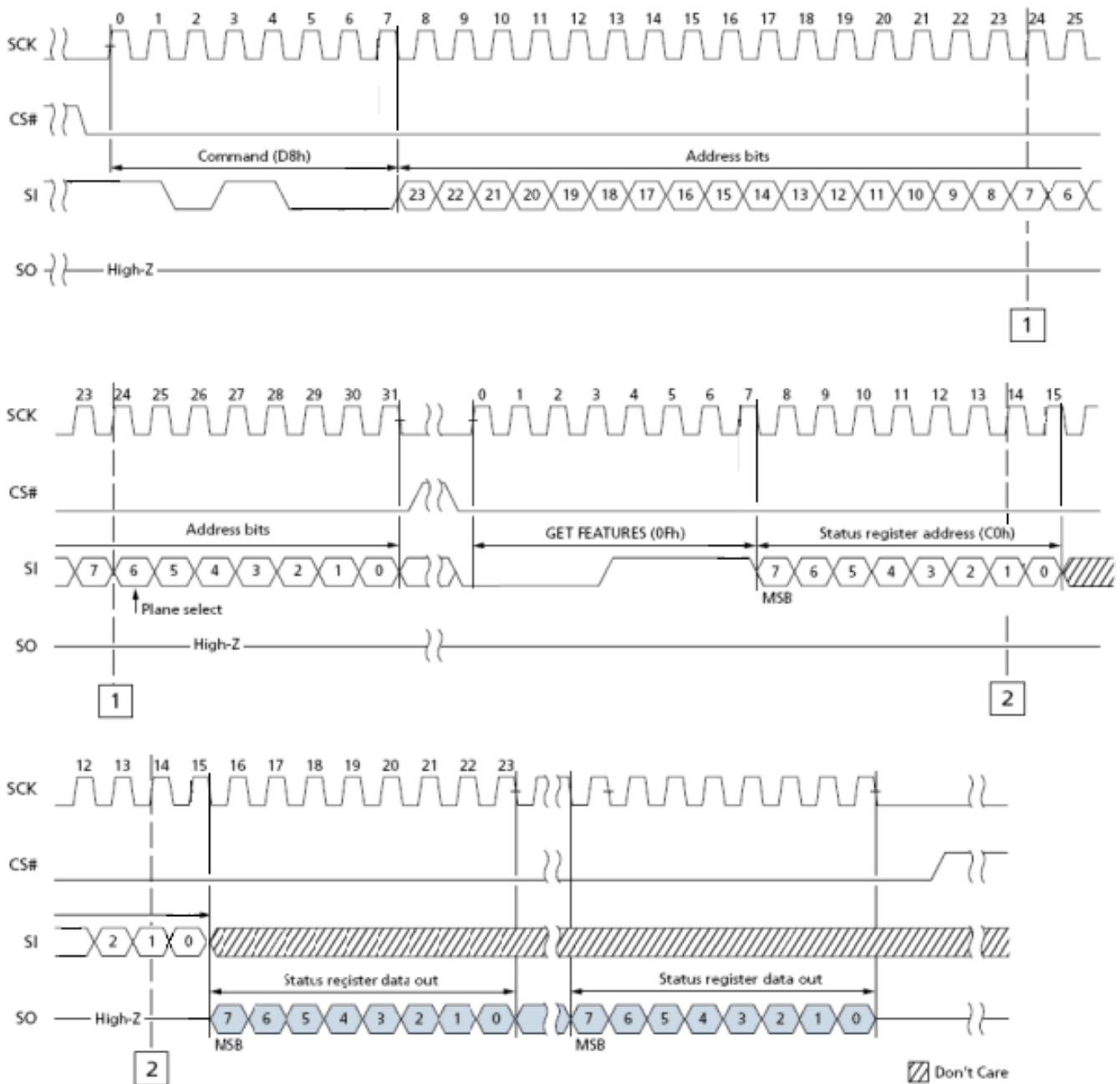
Erase Operation

The command sequence is follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

BLOCK ERASE command requires 24-bit address with 8 dummy bits and a 16-bit row address. If WRITE ENABLE command is not issued (WEL bit is not set), then the rest of the erase sequence is ignored. After the row address is registered, the control logic automatically controls the timing and the erase-verify operations, and the device is busy for t_{BERS} time. BLOCK ERASE command operates on one block at a time.

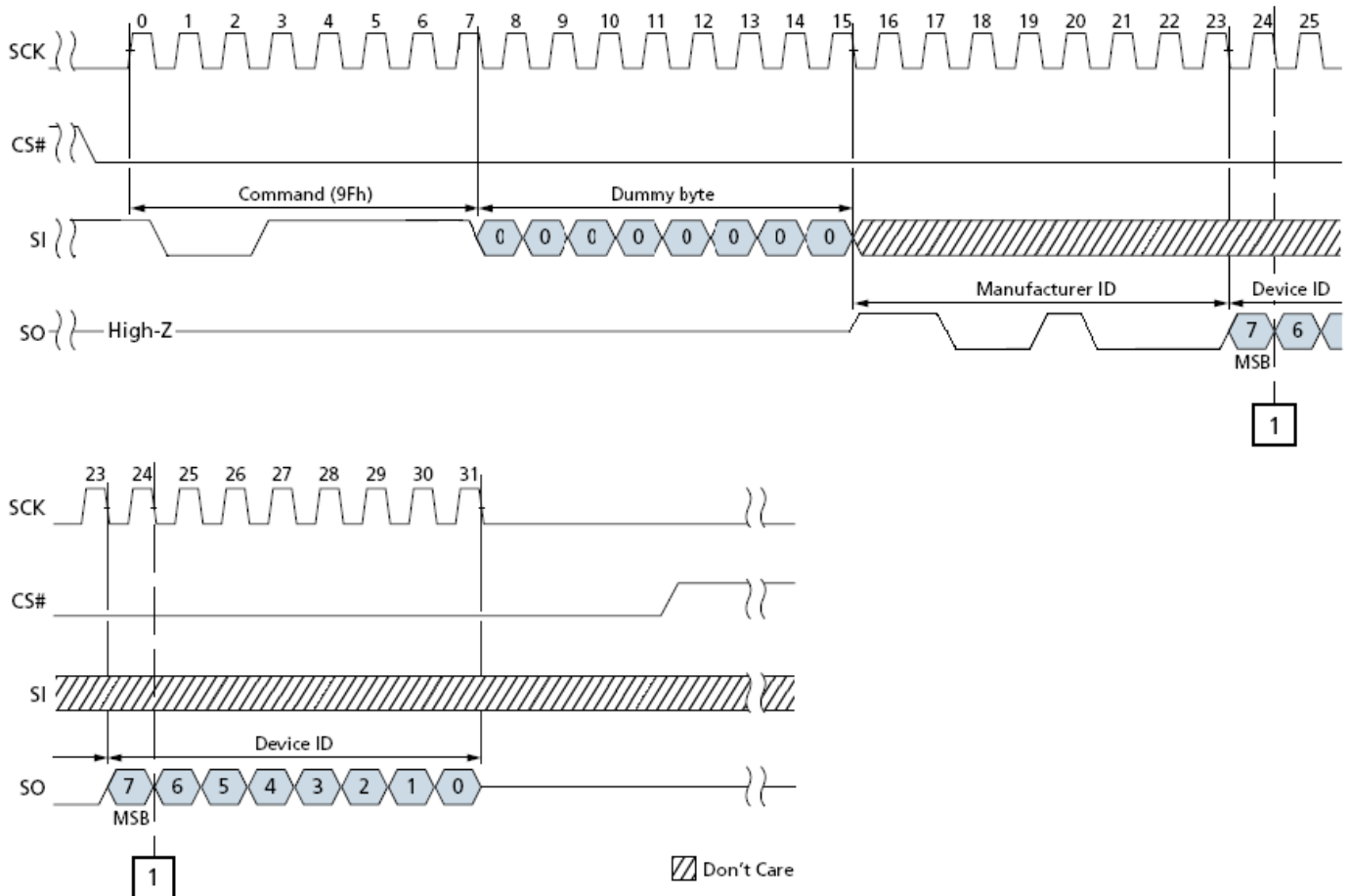
BLOCK ERASE (D8h) Timing



Read ID

The device contains a product identification mode, initiated by writing 9Fh to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

READ ID Timing

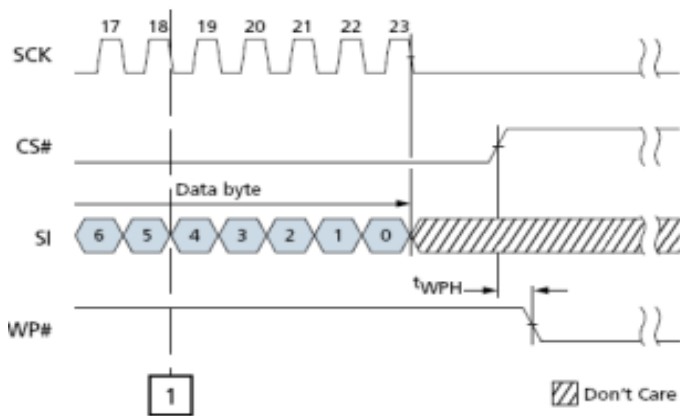
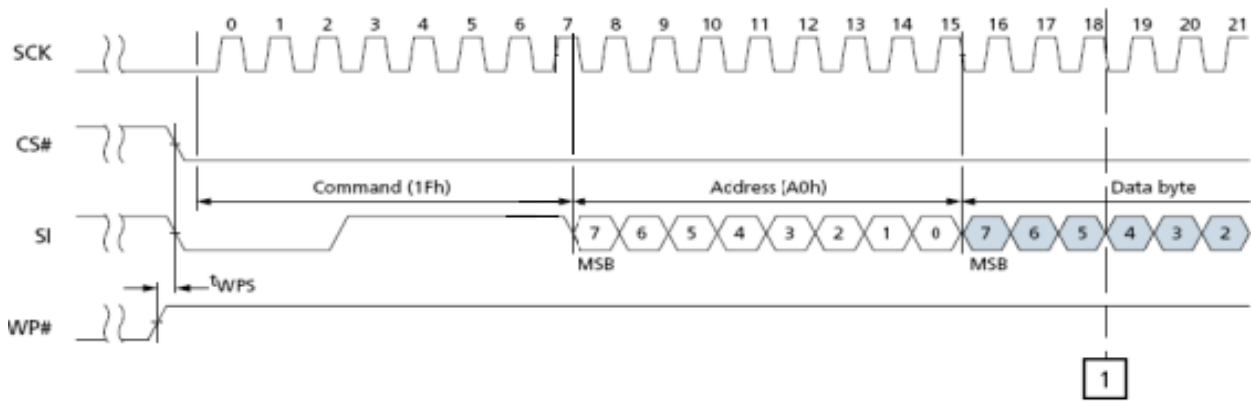


ID Definition Table

| Product ID | 1 st Cycle (Maker Code) | 2 nd Cycle (Device Code) | 3 rd Cycle | 4 th Cycle | 5 th Cycle |
|----------------|---------------------------------------|--|-----------------------|-----------------------|-----------------------|
| F50L1G41LB(2M) | C8h | 01h | 7Fh | 7Fh | 7Fh |

| | Description |
|----------------------|---|
| 1 st Byte | Maker Code |
| 2 nd Byte | Device Code |
| 3 rd Byte | JEDEC Maker Code Continuation Code, 7Fh |
| 4 th Byte | JEDEC Maker Code Continuation Code, 7Fh |
| 5 th Byte | JEDEC Maker Code Continuation Code, 7Fh |

WP# Timing

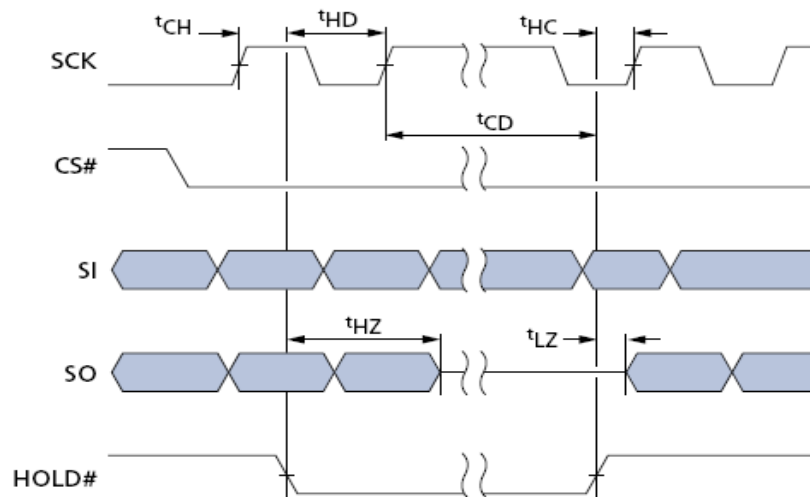


HOLD# Timing

HOLD# input provides a method to pause serial communication with the device but doesn't terminate any READ, PROGRAM, or ERASE operation currently in progress.

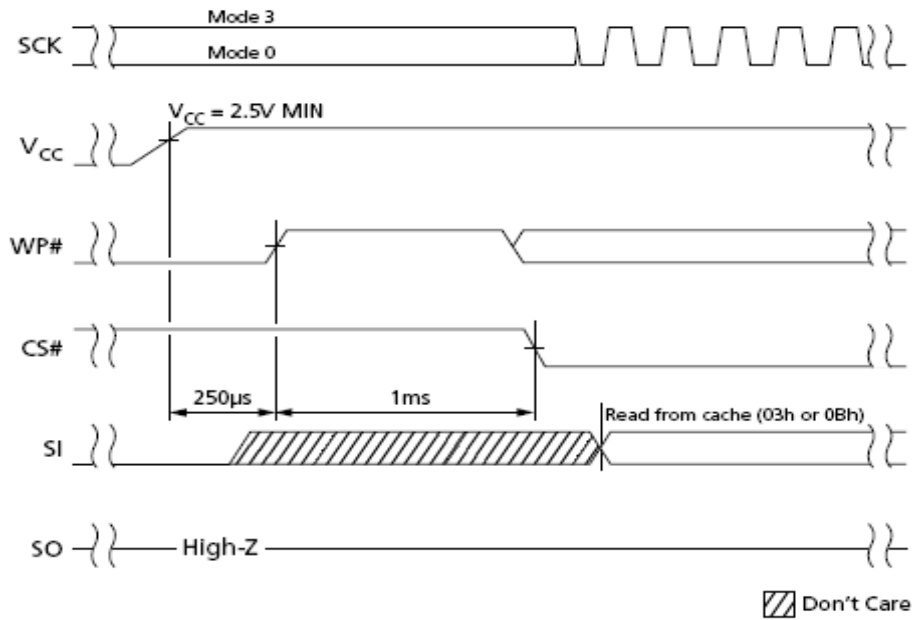
Hold mode starts at the falling edge of HOLD# provided SCK is also Low. If SCK is High when HOLD# goes Low, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also Low. If SCK is High, hold mode ends after the next falling edge of SCK.

During hold mode, SO is Hi-Z, and SI and SCK inputs are ignored.



Power-Up

During power transitions, V_{CC} is internally monitored. 250 μ s after V_{CC} has reached 2.5V, WP# is taken High, the device automatically performs the RESET command. The first access to the SPI NAND device can occur 1ms after WP# goes High, and then CS# can be driven Low, SCK can start, and the required command can be issued to the device.

Power-Up and RESET Timing

Read Unique ID Page / Read Parameter Page / OTP Operations

In addition to the main memory array, F50L1G41LB (2M) is also equipped with one Unique ID Page, and twenty-eight One-Time-Programmable Pages. The Unique ID Page contains 16 identical copies of the 32-Byte data. The Parameter Page contains 3 identical copies of the 256-Byte data. Both pages are Read only.

This flash device also offers one-time programmable memory area. 28 full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Regarding OTP Read, Read Unique ID Page, and Read Parameter Page, please refer to the specific Page addresses defined in OTP Area Details Table.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area. It means the OTP area becomes read-only after being locked.

The OTP area is only accessible while the OTP enable bit is set to 1. To set the device to OTP operation mode, issue the Set Feature (1Fh) command. When the device is in OTP operation mode, subsequent Read and/or Page Program (both X1 and X4) are applied to the OTP area. Please refer to relative command sequences defined in datasheet. When you want to come back to normal operation, you need to set OTP enable bit to 0. Otherwise, device will stay in OTP mode.

OTP/ Read / Read Unique ID / Read Parameter Page:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (B0h).
- Set the OTP enable bit to 1.
- Issue the Page Read (13h) command with a specific Page address.

OTP Program:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (A0h).
- Set Protection bit to 0.
- Issue the feature address (B0h).
- Set the OTP enable bit to 1.
- Issue the Write Enable (06h) command.
- Issue the Program Load (02h) and Program Execute (10h) commands.

OTP Lock:

- Issue the Set Feature (1Fh) command.
- Issue the feature address (A0h).
- Set Protection bit to 0.
- Issue the feature address (B0h).
- Set both the OTP enable and OTP protect bits to 1.
- Issue the Write Enable (06h) command.
- Issue the Program Execute (10h) command.

OTP Modes and Commands Table

| | | Set Feature |
|---------------------|-----------------|--|
| OTP Operation mode | Read | 1Fh - B0h ⁽¹⁾ - 40h or 50h ⁽²⁾ |
| | Page Program | 1Fh - B0h - 40h or 50h |
| OTP Protection mode | Program Protect | 1Fh - B0h - C0h or D0h |
| OTP Release mode | Leave OTP mode | 1Fh - B0h - 00h or 10h |

NOTE:

1. B0h is Configuration Register address.
2. 50h, D0h, and 10h are Configuration Register data values as ECC enabled.

OTP Area Details Table

| Item | Value | Description | Data Length |
|---|-----------|-----------------------------------|--------------|
| Unique ID Page address | 00h | Factory programmed, Read only | 32-Byte x 16 |
| Parameter Page address | 01h | Factory programmed, Read only | 256-Byte x 3 |
| Number of OTP pages | 28 | One Time Program and OTP lockable | 2112-Byte |
| OTP page address | 02h – 1Dh | One Time Program and OTP lockable | 2112-Byte |
| Number of partial page programs for each page in the OTP area | 1 | One Time Program and OTP lockable | 2112-Byte |

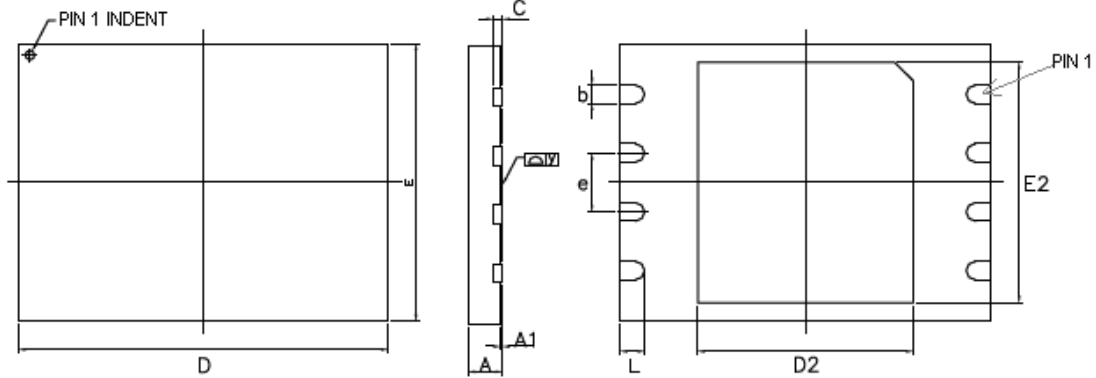
Parameter Page Data Table

| Byte | Description | Value |
|---------|--|---|
| 0-3 | Parameter page signature ("O", "N", "F", "I") | 4Fh, 4Eh, 46h, 49h |
| 4-5 | Revision number | 00h, 00h |
| 6-7 | Features supported | 00h, 00h |
| 8-9 | Optional commands supported | 2Ch, 00h |
| 10-31 | Reserved | All 00h |
| 32-43 | Device manufacturer | 50h, 4Fh, 57h, 45h, 52h, 43h, 48h, 49h, 50h, 20h, 20h, 20h |
| 44-63 | Device model | 50h, 53h, 55h, 31h, 47h, 53h, 32h, 30h, 44h, 58h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h |
| 64 | Manufacturer ID | C8h |
| 65-66 | Date code | 00h, 00h |
| 67-79 | Reserved | All 00h |
| 80-83 | Number of data bytes per page | 00h, 08h, 00h, 00h |
| 84-85 | Number of spare bytes per page | 40h, 00h |
| 86-91 | Reserved | All 00h |
| 92-95 | Number of pages per block | 40h, 00h, 00h, 00h |
| 96-99 | Number of blocks per unit | 00h, 04h, 00h, 00h |
| 100 | Number of logical units | 01h |
| 101 | Number of address cycles | 00h |
| 102 | Number of bits per cell | 01h |
| 103-104 | Number of maximum bad blocks per unit | 14h, 00h |
| 105-106 | Block endurance | 01h, 05h |
| 107 | Guaranteed valid blocks at beginning of target | 01h |
| 108-109 | Block endurance of guaranteed valid blocks | 00h, 00h |
| 110 | Number of partial programs per page | 04h |
| 111 | Reserved | 00h |
| 112 | Number of bits ECC | 00h |
| 113 | Number of Interleaved address bits | 00h |
| 114 | Interleaved operation attributes | 00h |
| 115-127 | Reserved | All 00h |
| 128 | I/O pin capacitance | 08h |

| | | |
|---------|--------------------------------------|-----------------------|
| 129-132 | Reserved | All 00h |
| 133-134 | tPROG (max) | 84h, 03h |
| 135-136 | tBERS (max) | 10h, 27h |
| 137-138 | tR (max) | 64h, 00h |
| 139-163 | Reserved | All 00h |
| 164-165 | Vendor-specific revision number | 00h, 00h |
| 166-253 | Reserved | All 00h |
| 254-255 | Integrity CRC | Set at test |
| 256-511 | Values of bytes 0-255 | Values of bytes 0-255 |
| 512-767 | Values of bytes 0-255 | Values of bytes 0-255 |
| 768+ | Additional redundant parameter pages | |

PACKING DIMENSIONS

8-Contact WSON (8x6 mm)

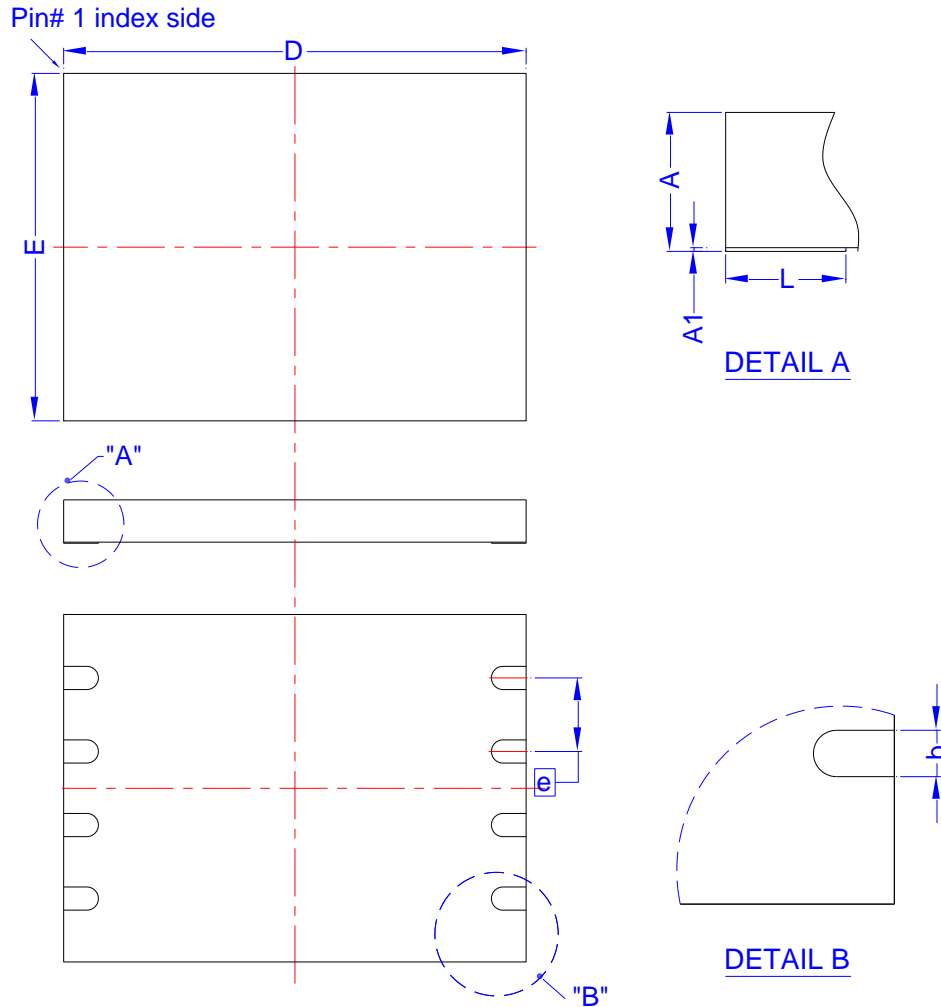


| SYMBOL | MILLIMETERS | | | INCHES | | |
|--------|-------------|--------|------|---------|--------|-------|
| | Min | Normal | Max | Min | Normal | Max |
| A | 0.70 | 0.75 | 0.8 | 0.028 | 0.03 | 0.031 |
| A1 | 0.00 | 0.035 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| C | 0.19 | 0.20 | 0.25 | 0.007 | 0.008 | 0.010 |
| D | 7.90 | 8.0 | 8.10 | 0.311 | 0.315 | 0.319 |
| D2 | 3.35 | 3.40 | 3.45 | 0.132 | 0.134 | 0.136 |
| E | 5.90 | 6.0 | 6.10 | 0.232 | 0.236 | 0.240 |
| E2 | 4.25 | 4.30 | 4.35 | 0.167 | 0.168 | 0.171 |
| e | 1.27BSC | | | 0.05BSC | | |
| L | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| y | 0.00 | ... | 0.08 | 0.000 | ... | 0.003 |

NOTE: BSC, Basic lead spacing between centers.

PACKING DIMENSIONS

8-Contact WSON (8x6 mm) without expose metal pad



| Symbol | Dimension in mm | | | Dimension in inch | | |
|--------|-----------------|------|------|-------------------|-------|-------|
| | Min | Min | Min | Min | Norm | Max |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |

Controlling dimension : millimeter
(Revision date : Apr 25 2018)

Revision History

| Revision | Date | Description |
|-----------------|-------------|--|
| 0.1 | 2016.11.21 | Original |
| 0.2 | 2017.01.03 | Modify title and product ID |
| 0.3 | 2017.08.29 | Add Read Unique ID Page / Read Parameter Page / OTP Operations |
| 0.4 | 2018.01.02 | Modify 8-Contact WSON (8x6 mm) PACKING DIMENSIONS |
| 1.0 | 2018.08.06 | Delete Preliminary |
| 1.1 | 2018.12.03 | Modify the packing dimension of WSON package |
| 1.2 | 2019.01.31 | 1. Restore the packing dimension of WSON package 2. Add the product ID and packing dimension of WSON package without expose metal pad |

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