FA3675F

CMOS IC
For Switching Power Supply Control

■ Description

FA3675F is a control IC for 6-channel DC-DC converter.
This IC can directly drive a Nch/Pch-MOSFET.
This IC is suitable to reduce converter size because it has many functions in a small package LQFP-48.

■ Features

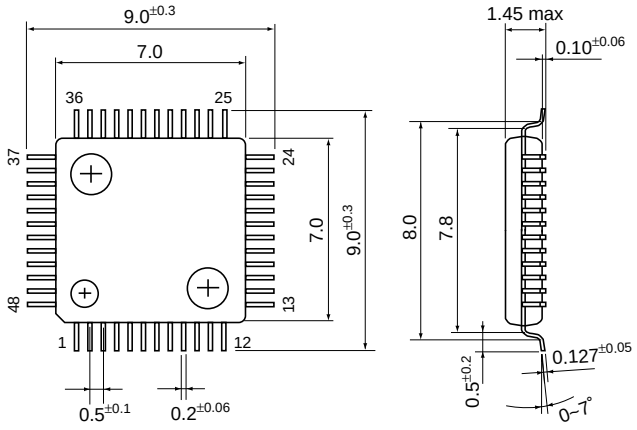
- 6-channel PWM control with MOSFET direct driving :
  5-channel for Pch-MOSFET, 1channel for Nch-MOSFET
- Low input voltage: 2.5V to 20V
- ±1.0% high accuracy bandgap reference
- Low power consumption by means of CDMOS
  Standby mode: 20μA(max.)
  Operating mode: 10mA(max.)
- Soft start function for each channel
- ON/OFF function for each channel
- Timer latch for short protection
- Undervoltage lockout
- Wide range of operation frequency: 50kHz to 1MHz
- Package: LQFP-48(Thin and small)

■ Application

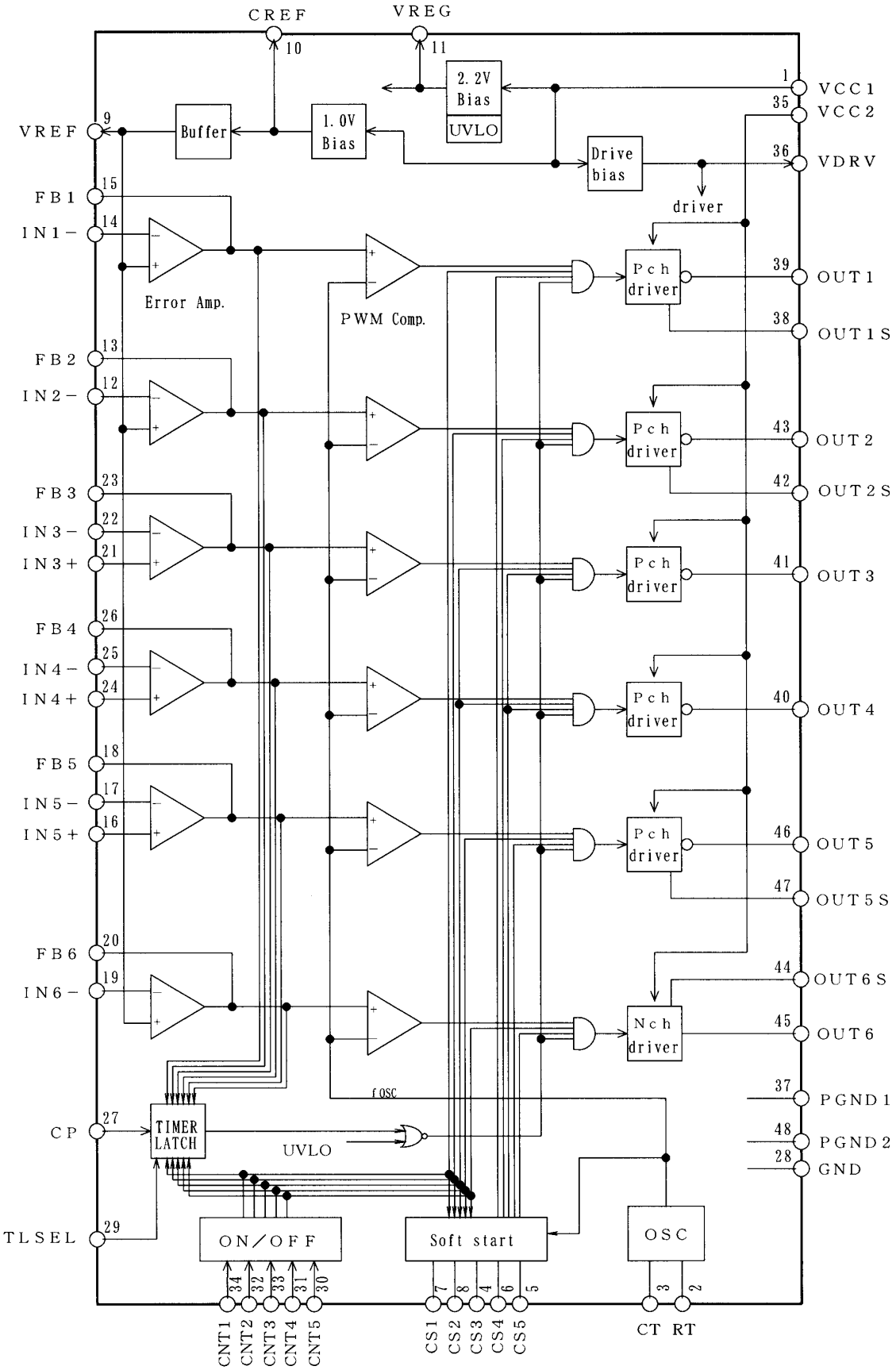
- VTR-camera, digital-steel-camera and portable equipment

■ Dimensions, mm

● LQFP-48



■ Block diagram



Pin No.	Pin symbol	Description
1	VCC1	Power supply for control circuit
2	RT	Oscillator timing resistor
3	CT	Oscillator timing capacitor
4	CS3	Soft start for Ch. 3 & Ch. 4
5	CS5	Soft start for Ch. 6
6	CS4	Soft start for Ch. 5
7	CS1	Soft start for Ch. 1
8	CS2	Soft start for Ch. 2
9	VREF	Reference voltage output
10	CREF	Capacitor for reference voltage output
11	VREG	Regulated voltage output
12	IN2-	Ch. 2 inverting input to error amplifier
13	FB2	Ch. 2 output of error amplifier
14	IN1-	Ch. 1 inverting input to error amplifier
15	FB1	Ch. 1 output of error amplifier
16	IN5+	Ch. 5 non-inverting input to error amplifier
17	IN5-	Ch. 5 inverting input to error amplifier
18	FB5	Ch. 5 output of error amplifier
19	IN6-	Ch. 6 inverting input to error amplifier
20	FB6	Ch. 6 output of error amplifier
21	IN3+	Ch. 3 non-inverting input to error amplifier
22	IN3-	Ch. 3 inverting input to error amplifier
23	FB3	Ch. 3 output of error amplifier
24	IN4+	Ch. 4 non-inverting input to error amplifier

Pin No.	Pin symbol	Description
25	IN4-	Ch. 4 inverting input to error amplifier
26	FB4	Ch. 4 output of error amplifier
27	CP	Timing capacitor for timer latch delay
28	GND	Ground
29	TLSEL	Ch. 3 & Ch. 4 timer latch selection (Low: disable)
30	CNT5	Ch. 6 ON/OFF function
31	CNT4	Ch. 5 ON/OFF function
32	CNT2	Ch. 2 ON/OFF function
33	CNT3	Ch. 3 & Ch. 4 ON/OFF function
34	CNT1	Ch. 1 ON/OFF function
35	VCC2	Power supply for output stage
36	VDRV	Bias for logic circuit of outputs
37	PGND1	Power ground
38	OUT1S	Ch. 1 source electrode of output stage
39	OUT1	Ch. 1 output (for Pch-MOSFET)
40	OUT4	Ch. 4 output (for Pch-MOSFET)
41	OUT3	Ch. 3 output (for Pch-MOSFET)
42	OUT2S	Ch. 2 source electrode of output stage
43	OUT2	Ch. 2 output (for Pch-MOSFET)
44	OUT6S	Ch. 6 source electrode of output stage
45	OUT6	Ch. 6 output (for Nch-MOSFET)
46	OUT5	Ch. 5 output (for Pch-MOSFET)
47	OUT5S	Ch. 5 source electrode of output stage
48	PGND2	Power ground

■ Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	20.0	V
Source peak current	I_{OUT}	–200	mA
Sink peak current	I_{OUT}	200	mA
Input voltage for analog input	V_{ANA}	–0.3 to +2.5	V
Input voltage for logic input	V_{LOG}	–0.3 to Vcc +0.5 (Vcc ≤ 5.0V) –0.3 to +5.5 (Vcc > 5.0V)	V
Total power dissipation *	Pd	550	mW
Junction temperature	T_J	125	°C
Ambient temperature	T_{OP}	–20 to +85	°C
Storage temperature	Tstg	–40 to +150	°C

* Ta < 25°C

■ Recommended operating conditions

Item		Symbol	Min.	Max.	Unit
Power supply voltage		V_{CC}	2.5	18.0	V
Input voltage for logic input	Vcc ≤ 5.0 Vcc > 5.0	V_{LOG}	0.0 0.0	Vcc +0.25 5.25	V
Oscillation frequency		f_{OSC}	50	1000	kHz
Oscillator timing resistor		R_T	6.8	100	kΩ
Oscillator timing capacitor		C_T	22	1000	pF
CREF terminal by-pass capacitor		C_{REF}	0.01		µF

■ **Electrical characteristics** (Ta=25°C, V_{CC1}=V_{CC2}=6V, C_T=100pF, R_T=10kΩ)

Reference voltage section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REF}	No load	0.99	1.00	1.01	V
Load regulation	V_{RFLOD}	No load to R_L=15kΩ		7	15	mV
Line regulation	V_{RFLIN}	V_{CC}=2.5 to 18V		3	10	mV
Output voltage variation due to temperature change	V_{RTa}	Ta=–20 to +85°C		±0.5	±1.0	%

Regulated voltage section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REG}	No load	2.134	2.20	2.266	V
Load regulation	$V_{RG\ LOD}$	No load to R_L=3.9kΩ		2	10	mV
Line regulation	$V_{RG\ LIN}$	V_{CC}=2.5 to 18V		6	20	mV
Output voltage variation due to temperature change	V_{RGTa}	Ta=–20 to +85°C		±0.5	±1.0	%

Oscillator section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	R_T=10kΩ, C_T=100pF	432	480	528	kHz
Frequency variation due to supply voltage change	f_{dV}	V_{CC}=2.5 to 18V		±1	±3	%
Frequency variation due to temperature change	f_{dT}	Ta=–20 to +25°C		±3	±6	%
		Ta=+25 to +85°C		±7	±14	

Error amplifier section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOF}			2	10	mV
Input common mode voltage range	V_{ICOM}		0.2		1.5	V
Open-loop gain	A_{VOL}		70	75		dB
Unity-gain bandwidth	f_T			1.0		MHz
Output sink current	I_{FBL}	V_{FB}=V_{REF} +0.05V	2.5	3.5		mA
Output source current	I_{FBH}	V_{FB}=V_{REF} -0.05V		–0.18	–0.14	mA

Soft-start circuit section 1 (CS1, CS2, CS3)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	V_{CSO}	Duty cycle=0%	0.36	0.46	0.56	V
	V_{CS100}	Duty cycle=100%	1.11	1.31	1.51	V
Charge current	I_{CS}	V_{CS}=0V	–7.5	–5.0	–2.5	μA

Soft-start circuit section 2 (CS4, CS5)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	V_{CSO}	Duty cycle=0%	0.36	0.46	0.56	V
	V_{CS100}	Duty cycle=100%	1.11	1.31	1.51	V
Charge current	I_{CS}			0		μA

Short-circuit protection section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage at CP	V_{CPTH}		1.39	1.64	1.89	V
Charge current at CP	I_{CP}		–3.0	–1.9	–1.0	µA
Threshold voltage at error amplifier output	V_{FBTL}		1.36	1.56	1.76	V

ON/OFF logic input section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input voltage for ON mode	V_{DH}	V_{cc}≤5.0V	1.0		Vcc +0.25	V
		V_{cc}>5.0V	1.0		5.25	
Input voltage for OFF mode	V_{DL}		0		0.4	V

Undervoltage lockout circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
OFF to ON threshold voltage	V_{UVVCC}		1.52	1.72	1.92	V
Voltage hysteresis	Δ_{UVCC}			0.1		V

Output section 1 (OUT1)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
L-level ON resistance	R_{ONL}	I_O=10mA, OUT1S:GND		6	10	Ω
H-level ON resistance	R_{ONH}	I_O=–10mA, OUT1S:GND		6	10	Ω
Rise time	tr	C_{LOAD}=1000pF, OUT1S:GND		30	50	ns
Fall time	tf	C_{LOAD}=1000pF, OUT1S:GND		60	85	ns
Sink current	I_{OUT}	OUT1S:R_{S1}=68Ω to GND	9	12	15	mA

Output section 2 (OUT2, OUT5)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
L-level ON resistance	R_{ONL}	I_O=10mA OUT2S, OUT5S:GND		10	15	Ω
H-level ON resistance	R_{ONH}	I_O=–10mA OUT2S, OUT5S:GND		10	15	Ω
Rise time	tr	C_{LOAD}=1000pF OUT2S, OUT5S:GND		40	60	ns
Fall time	tf	C_{LOAD}=1000pF OUT2S, OUT5S:GND		70	95	ns
Sink current	I_{OUT}	OUT2S, OUT5S: R_{S2}, R_{S5}=68Ω to GND	8	11	14	mA

Output section 3 (OUT3, OUT4)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
L-level ON resistance	R_{ONL}	I_O=10mA		10	15	Ω
H-level ON resistance	R_{ONH}	I_O=–10mA		10	15	Ω
Rise time	tr	C_{LOAD}=1000pF		40	60	ns
Fall time	tf	C_{LOAD}=1000pF		70	95	ns

Output section 4 (OUT6)

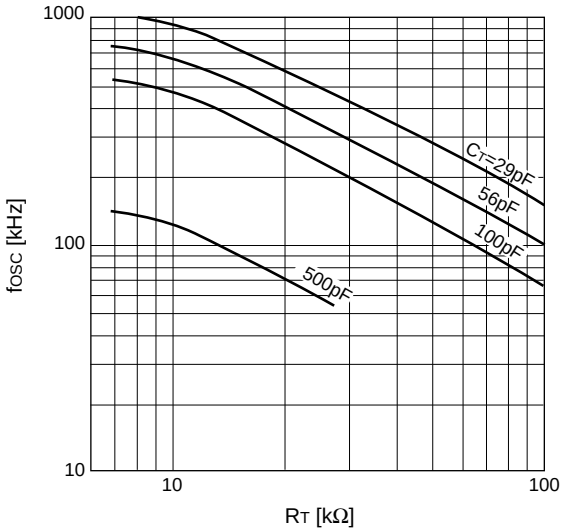
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
L-level ON resistance	R_{ONL}	I_O=10mA, OUT6S:VCC2		10	15	Ω
H-level ON resistance	R_{ONH}	I_O=–10mA, OUT6S:VCC2		10	15	Ω
Rise time	tr	C_{LOAD}=1000pF, OUT6S:VCC2		40	60	ns
Fall time	tf	C_{LOAD}=1000pF, OUT6S:VCC2		70	95	ns
Source current	I_{OUT}	OUT6S:R_{S6}=330Ω to VCC2 V_{CC}=7V	-14	-11	-8	mA

Overall device

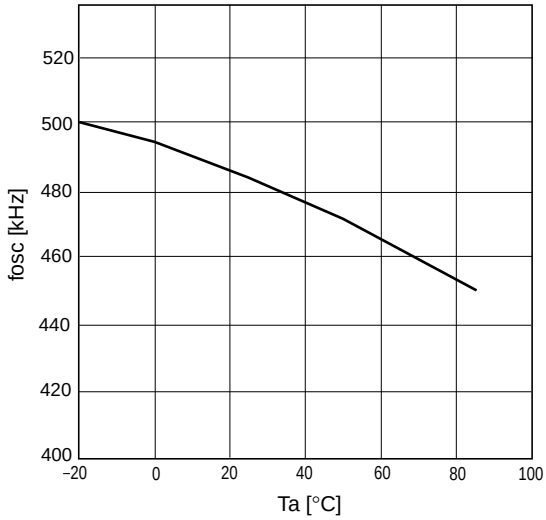
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Standby current	I_{CCO}			12	20	µA
Operating-state supply current	I_{CC}	Duty cycle=0%, R_L= ∞		4	6	mA

■ Characteristic curves (Ta = 25°C)

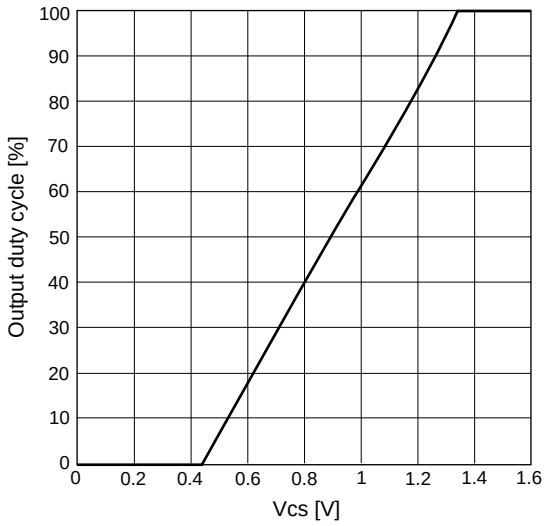
Oscillation frequency (fosc) vs. timing resistor resistance (R_T)



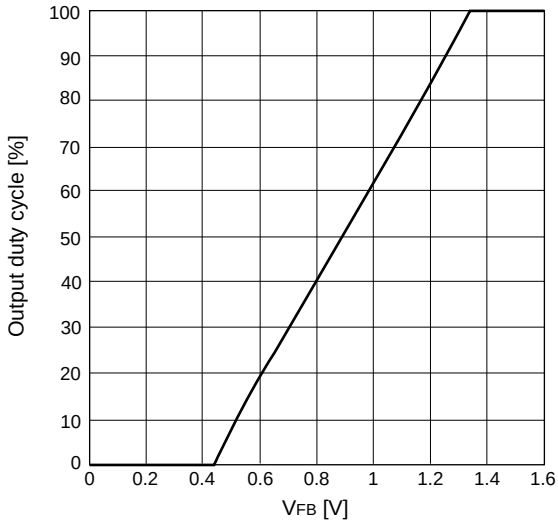
Oscillation frequency (fosc) vs. ambient temperature (Ta)



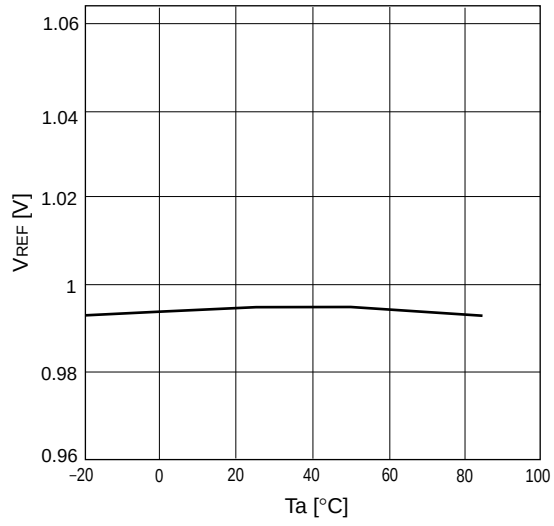
Output duty cycle vs. CS terminal voltage (V_{CS})



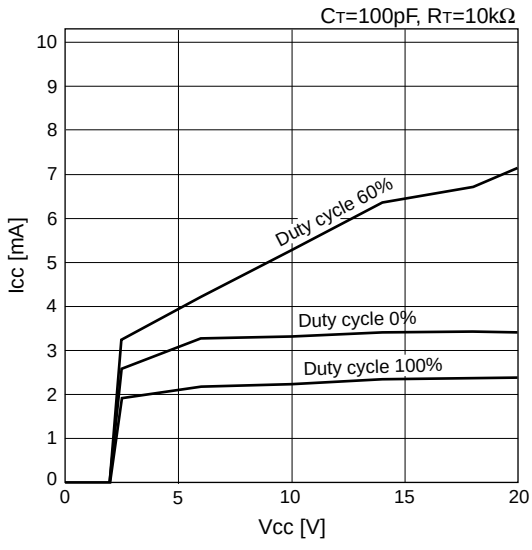
Output duty cycle vs. FB terminal voltage (V_{FB})



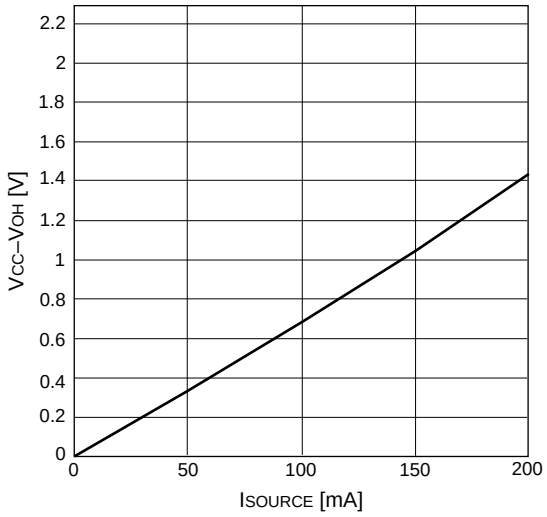
Reference voltage (V_{REF}) vs ambient temperatare (T_a)



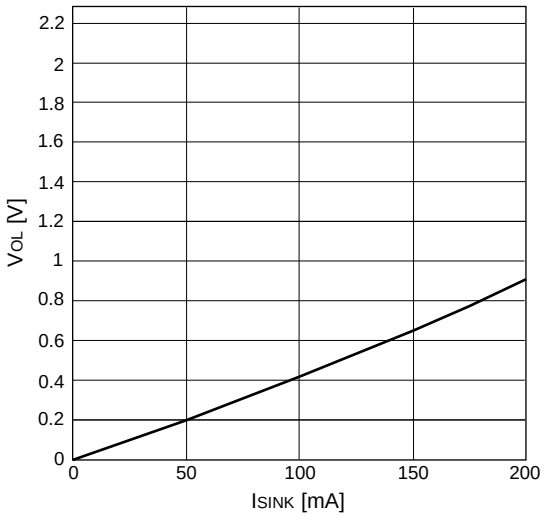
Supply current (I_{CC}) vs supply voltage (V_{CC})



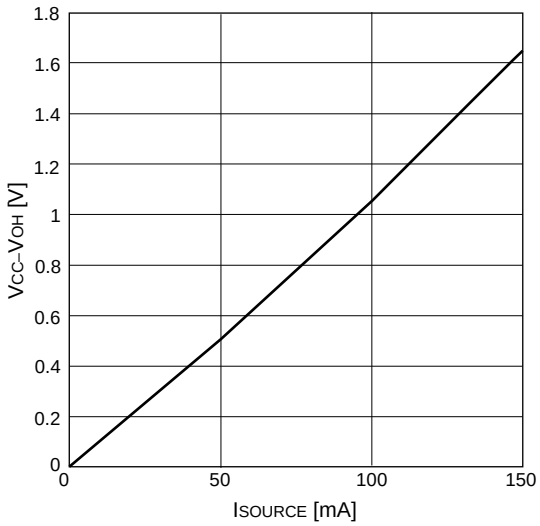
H-level output voltage (V_{CC}-V_{OH}) vs. output source current (I_{SOURCE}) for OUT1



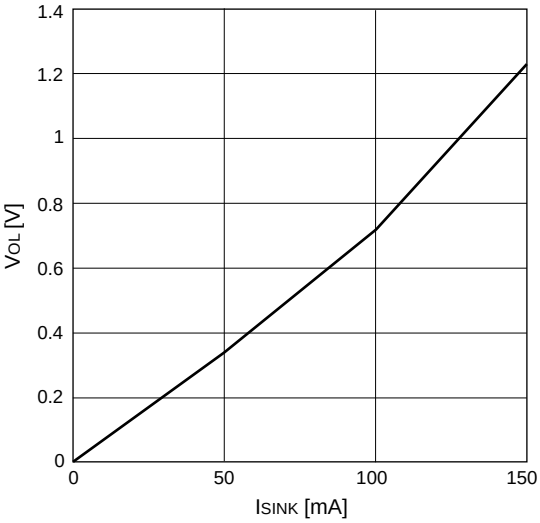
L-level output voltage(V_{OL}) vs. output sink current (I_{SINK}) for OUT1



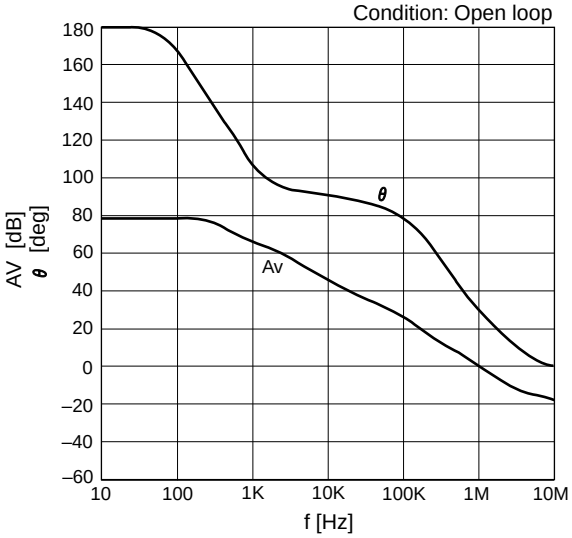
H-level output voltage (V_{CC}-V_{OH}) vs. output source current (I_{SOURCE}) for OUT2, 3, 4, 5, 6



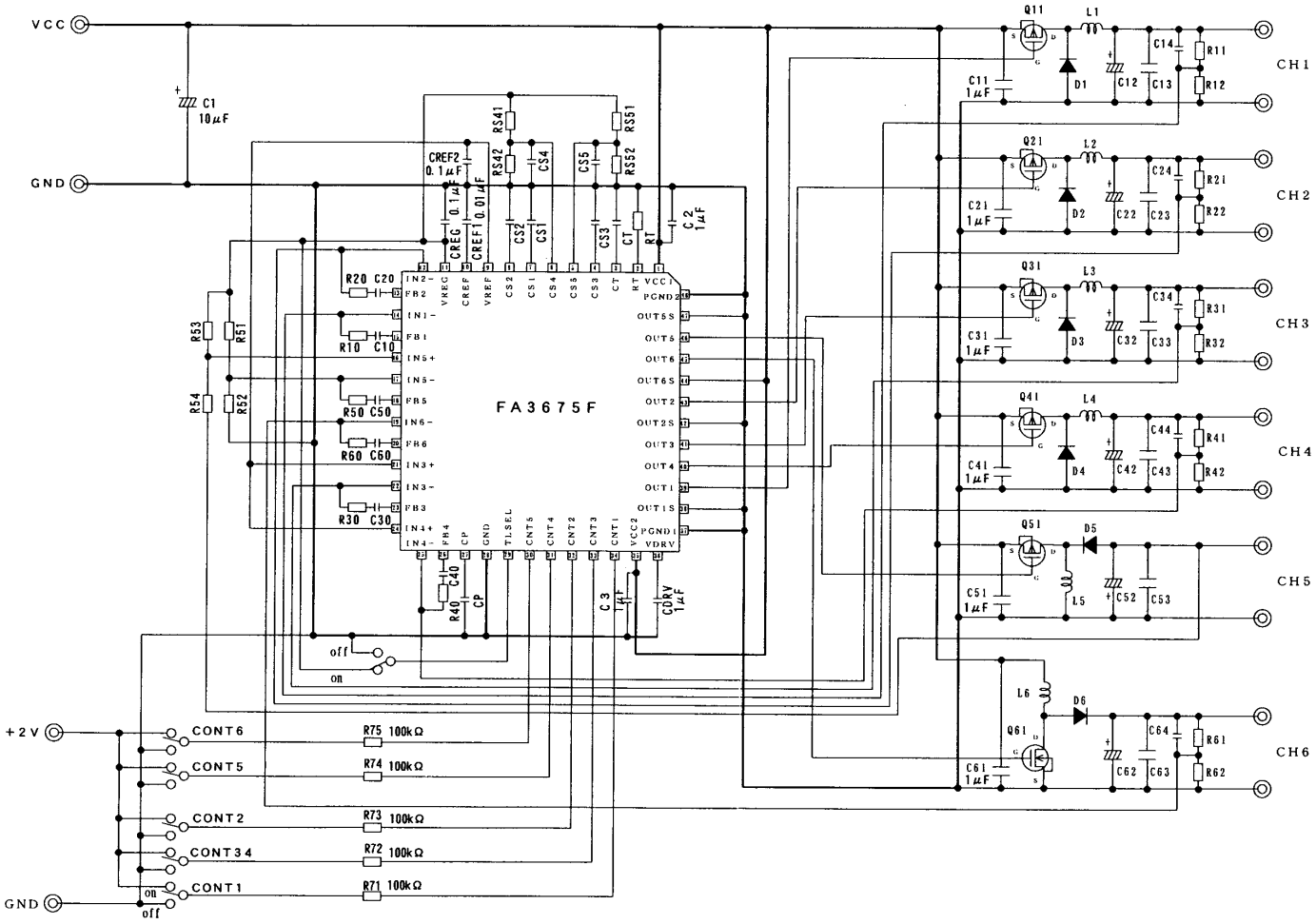
L-level output voltage(V_{OL}) vs. output sink current (I_{SINK}) for OUT2, 3, 4, 5, 6



Error amplifier voltage gain(Av) / phase(θ) vs. frequency(f)



■ Application circuit



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.