FA7700V, FA7701V

CMOS IC
For Switching Power Supply Control

■ Description

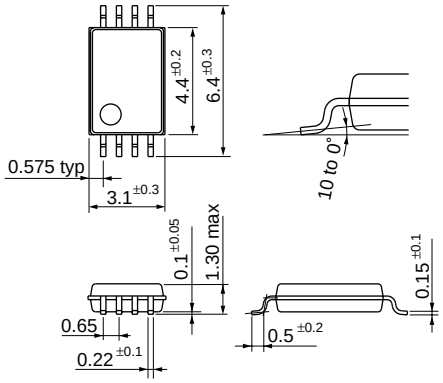
FA7700V/FA7701V are the PWM type DC to DC converter control ICs with 1ch output that can directly drive power MOSFETs. CMOS devices with high breakdown voltage are used in these ICs and low power consumption is achieved. These ICs have not only the functions equivalent to those of FA76XX series but also the functions of directly driving Nch/Pch MOSFETs, lower power consumption, higher frequency operation, and less external components.

■ Features

- Wide range of supply voltage: V_{CC}=2.5 to 20V
- FA7700V: For boost, flyback converter
  (Maximum output duty cycle is 80%)
- FA7701V: For buck converter
  (Maximum output duty cycle is 100%)
- Output stage consist of CMOS push-pull circuit, and achieves a high speed switching of external MOSFETs. (FA7700V: For Nch-MOSFET driving, FA7701V: For Pch-MOSFET driving)
- High accuracy reference voltage (Error amplifier): 0.88V±2%
- Soft start function
- Adjustable built-in timer latch for short-circuit protection
- Output ON/OFF control function
- Less external discrete components needed (2 components less than conventional version of the equivalent products)
- Low power consumption
  Stand-by current: 40µA typ.
  Operating current: 1.2mA typ. (Including error amplifier output current and oscillator current)
- High frequency operation: 50kHz to 1MHz
- Package: TSSOP-8, thin and small

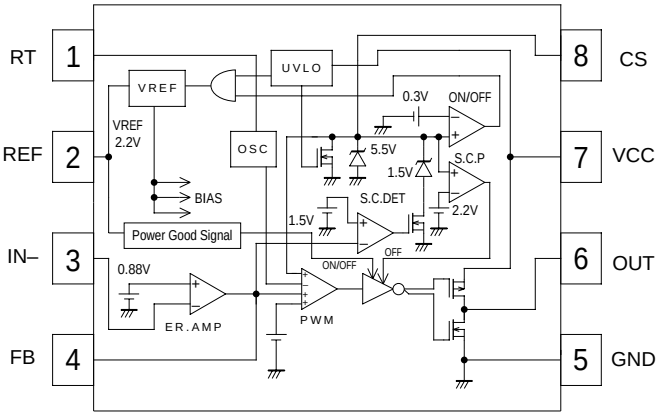
■ Dimensions, mm

● TSSOP-8

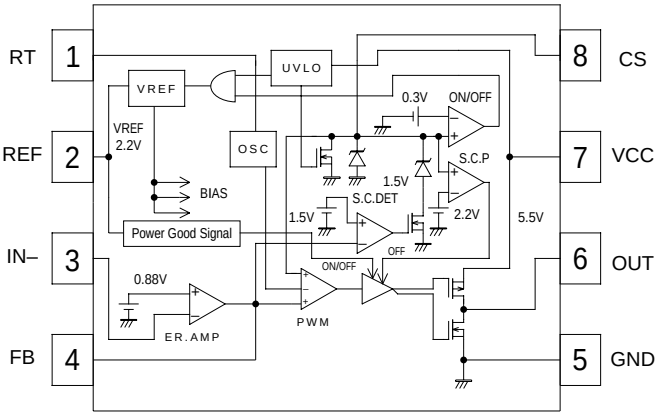


■ Block diagram

● FA7700V



● FA7701V

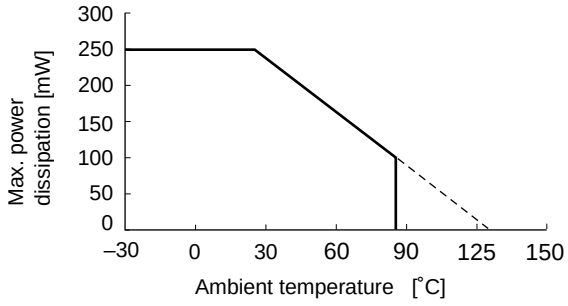


Pin No.	Pin symbol	Description
1	RT	Oscillator timing resistor
2	REF	Internal bias voltage
3	IN (–)	Error amplifier inverting input
4	FB	Error amplifier output
5	GND	Ground
6	OUT	Output for driving switching device
7	VCC	Power supply
8	CS	ON/OFF, soft start, timer latched short circuit protection

■ Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	Vcc	20	V
REF terminal output current	I_{REF}	2	mA
OUT terminal source current	$I_{SO\ peak}$	–400 (peak)	mA
	$I_{SO\ cont}$	–50 (continuos)	
OUT terminal sink current	$I_{SI\ peak}$	+150 (peak)	mA
	$I_{SI\ cont}$	+50 (continuos)	
RT, REF, IN–, FB terminal voltage	V_{RT}, V_{REF}	+2.5 (max.)	V
	V_{IN-}, V_{FB}	–0.3 (min.)	
CS terminal voltage	V_{CS}	Self limiting≒5.5 (max.)	V
		–0.3 (min.)	
CS terminal sink current	I_{CS}	200	µA
Power dissipation	Pd	250 (Ta≦25˚C)	mW
Operating ambient temperature	Ta	–30 to +85	˚C
Operating junction temperature	Tj	+125	˚C
Storage temperature	T_{stg}	–40 to +150	˚C

Maximum power dissipation curve



■ Recommended operating condition

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.5	6	18	V
DC feedback resistor of error amplifier	R_{NF}	100			kΩ
VCC terminal capacitance	C_{VCC}	0.1			µF
REF terminal capacitance	C_{REF}	0.047	0.1	1	µF
CS terminal capacitance	C_S	0.01		10	µF
CS terminal sink current	I_{csin}	1*		50	µA
Oscillation frequency	f_{osc}	50		1000	kHz

* Lower limit of I_{CSIN} does not include leak current "I_L" for capacitor Cs. Set a resistor "R_{CS} [MΩ]" connected between VCC terminal and CS terminal to satisfy the equation.

$$\frac{V_{CC} - 1.5}{50\mu A + I_L} < R_{CS}\ [M\Omega] < \frac{V_{CC} - 1.5}{1\mu A + I_L}$$

■ Electrical characteristics (Ta=25˚C, V_{CC}=6V, R_T=22kΩ)

Internal bias section (REF terminal voltage)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REF}	REF terminal source current I_{REF}=0mA	2.16	2.23	2.30	V
Line regulation	V_{LINE}	Vcc=2.5 to 20V, I_{REF}=0mA		±2	±14	mV
Load regulation	V_{LOAD}	I_{REF}=0 to 2mA		±2	±12	mV
Variation with temperature	V_{TC1}	Ta=–30 to 25°C		±0.3		%
	V_{TC2}	Ta=25 to 85°C		±0.3		%

Oscillator section (Frequency set by R_T terminal)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{osc}	R_T=22kΩ	155	185	215	kHz
Line regulation	f_{LINE}	Vcc=2.5 to 20V		±0.1		%
Variation with temperature	f_{TC1}	Ta=–30 to 25°C, 50k to 1MHz		±2		%
	f_{TC2}	Ta=25 to 85°C, 50k to 1MHz		±3		%

Error amplifier section (IN- terminal, FB terminal)

Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage		V_B	IN- terminal, FB terminal: Shorted (voltage follower)	0.863	0.880	0.897	V
Input current		I_{IN-}		-500		+500	nA
V_B line regulation		V_{BLINE}	Vcc=2.5 to 20V		±1	±5	mV
V_B variation with temperature		V_{BTC1}	Ta=–30 to 25°C		±0.3		%
		V_{BTC2}	Ta=25 to 85°C		±0.3		%
Open loop gain		A_{VO}		70			dB
Unity gain bandwidth		f_T			1.5		MHz
Output current	Source	I_{OHE}	FB terminal=V_{REF}– 0.5V	–220	–160	–100	μA
	Sink	I_{OLE}	FB terminal=0.5V	3	6	12	mA

Pulse width modulation (PWM) section (FB terminal voltage and duty cycle)

Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
FB 0% threshold		V_{FB0}	Duty cycle = 0%	0.560	0.660	0.760	V
FB 50% threshold		V_{FB50}	Duty cycle = 50%		0.880		V
Maximum duty cycle	FA7700	D_{MAX1}	R_T=100kΩ, f=50kHz	85	90	95	%
		D_{MAX2}	R_T=22kΩ, f≒185kHz	83	88	93	%
		D_{MAX3}	R_T=3kΩ, f≒1MHz	80	86	92	%
	FA7701	D_{MAX}		100			%

Undervoltage lock-out section (V_{CC} terminal voltage)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
ON threshold	V_{CCON}			2.07	2.30	V
OFF threshold	V_{CCOF}		1.60	1.93		V
Hysteresis voltage	V_{CCHY}		0.04	0.14	0.24	V
Variation with temperature	V_{CCHY}	Ta= –30 to 25°C		+0.2		mV/°C
		Ta= 25 to 85°C		–0.2		mV/°C

ON/OFF section (CS terminal voltage)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
ON/OFF threshold	V_{ONOF}		0.150	0.300	0.450	V
Threshold variation with temperature	V_{ONTC}	Ta = –30 to 85°C		+0.5		mV/°C

Soft start section (CS terminal voltage)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage 1	V_{CS0}	Duty cycle=0%	0.560	0.660	0.760	V
Threshold voltage 2	V_{CS50}	Duty cycle=50%		0.880		V

Timer latched short circuit protection section (FB terminal, CS terminal)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Short detection threshold voltage	V_{FBTH}	FB terminal voltage	1.350	1.500	1.650	V
Latched mode threshold voltage	V_{CSTH}	CS terminal voltage	2.050	2.200	2.350	V
Latched mode reset voltage	V_{CSRE}	CS terminal voltage	1.700	2.030	2.300	V
Latched mode hysteresis	V_{CSHY}	CS terminal voltage	50	170	350	mV
CS terminal clamped voltage	V_{CSCL1}	FB terminal<1.35V, CS sink current= +1μA	1.400	1.500	1.600	V
	V_{CSCL2}	FB terminal>1.65V, CS sink current= +150μA	4.500	5.500	6.500	V

Output stage section (OUT terminal)

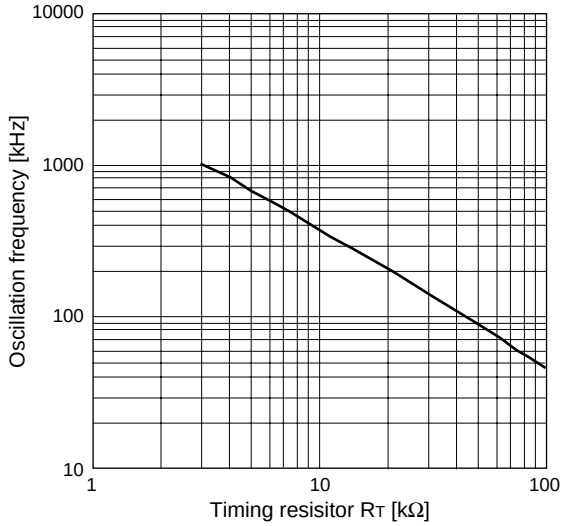
Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
High side on resistance		R_{ONH}	VCC=6V, source current= –50mA		10	20	Ω
		R_{ONH}	VCC=2.5V, source current= –50mA		18	36	Ω
Low side on resistance		R_{ONL}	VCC=6V, sink current= +50mA		5	10	Ω
		R_{ONL}	VCC=2.5V, sink current= +50mA		5	10	Ω
Rise time	FA7700	tr	330pF load to GND terminal		20		ns
	FA7701		330pF load to VCC terminal		25		ns
Fall time	FA7700	tf	330pF load to GND terminal		45		ns
	FA7701		330pF load to VCC terminal		40		ns

Overall section (Supply current to VCC terminal)

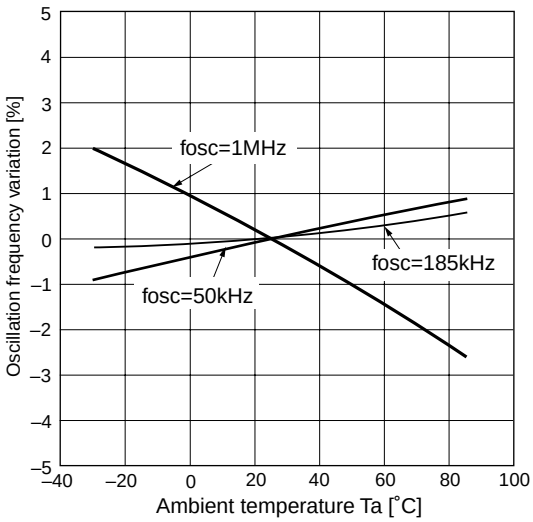
Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
OFF mode supply current	I_{CCST1}	CS terminal=0V		40	100	μA
Operating mode supply current	I_{CC0}	Duty cycle=0%, OUT:Open, IN–=0V, FB:Open		0.9	1.5	mA
	I_{CC1}	Duty cycle=50%, OUT:Open, IN–, FB:Shorted		1.2	2.0	mA
Latched mode supply current	I_{CCLAT}	CS terminal >2.35V, IN–=0V, FB:Open		0.9	1.5	mA

■ Characteristic curves

Oscillation frequency (fosc) vs. timing resistor resistance (R_T)

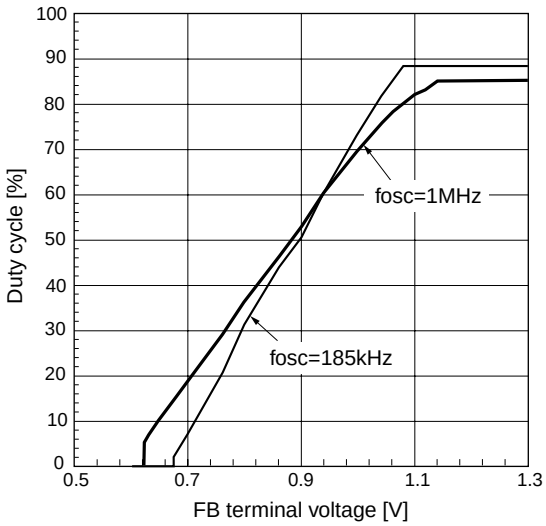


Oscillation frequency (fosc) vs. ambient temperature



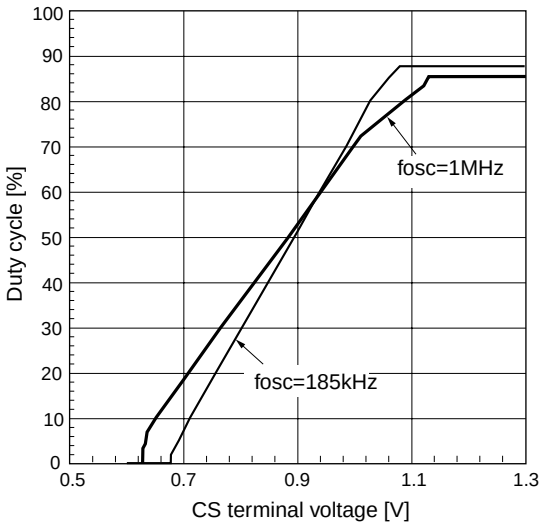
Duty cycle vs. FB terminal voltage

FA7700



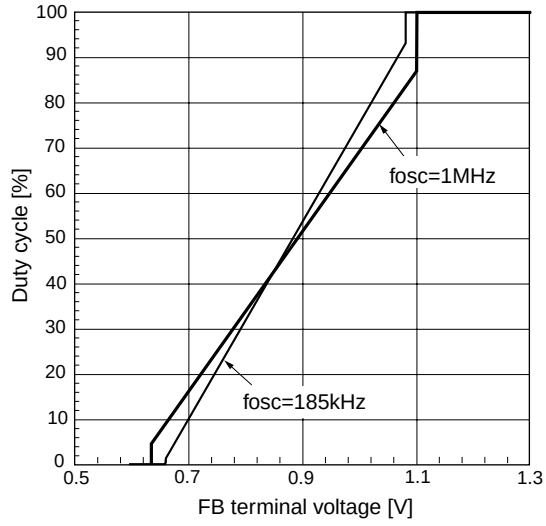
Duty cycle vs. CS terminal voltage

FA7700



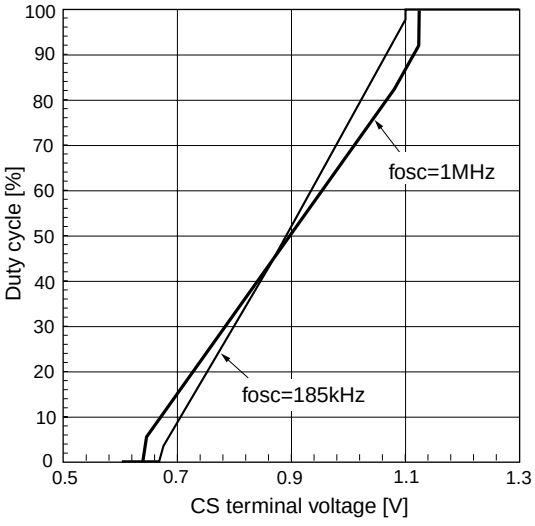
Duty cycle vs. FB terminal voltage

FA7701



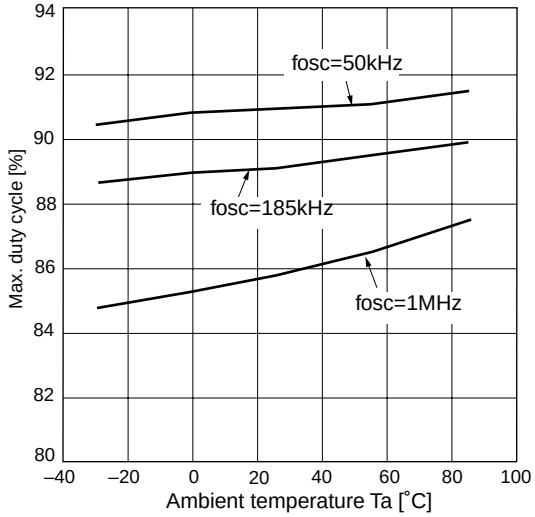
Duty cycle vs. CS terminal voltage

FA7701

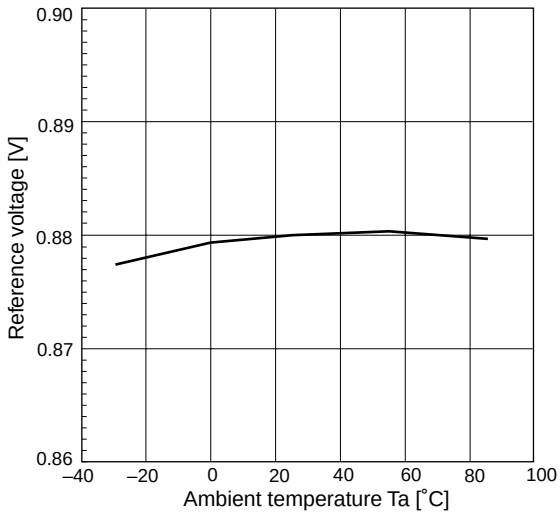


Maximum duty cycle vs. ambient temperature

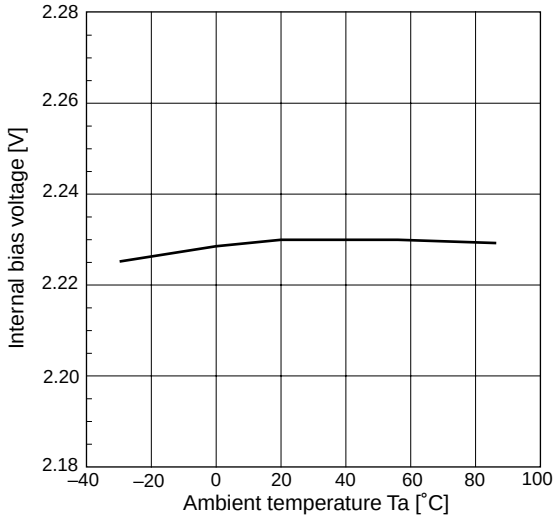
FA7700



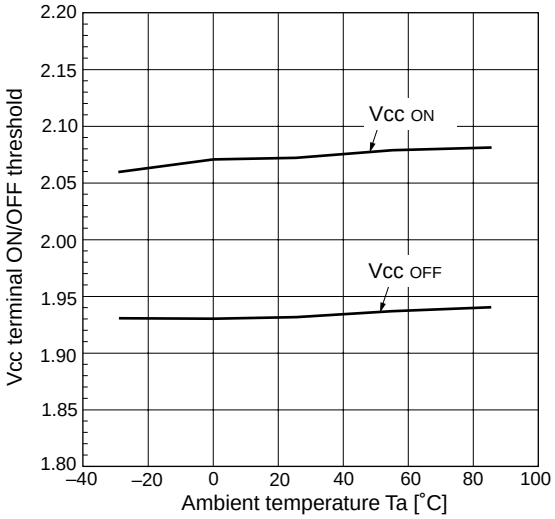
Error amp. reference voltage vs. ambient temperature



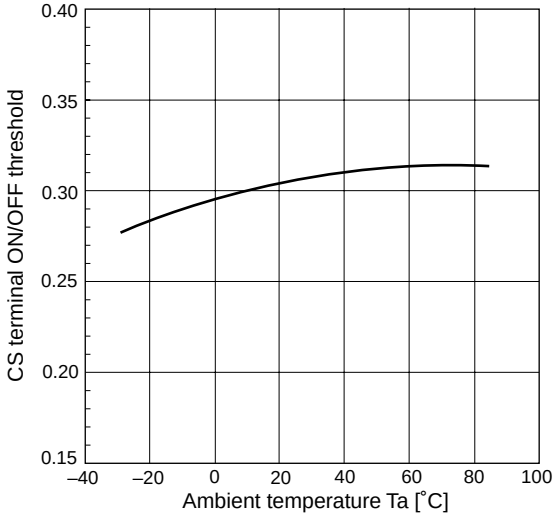
Internal bias voltage vs. ambient temperature



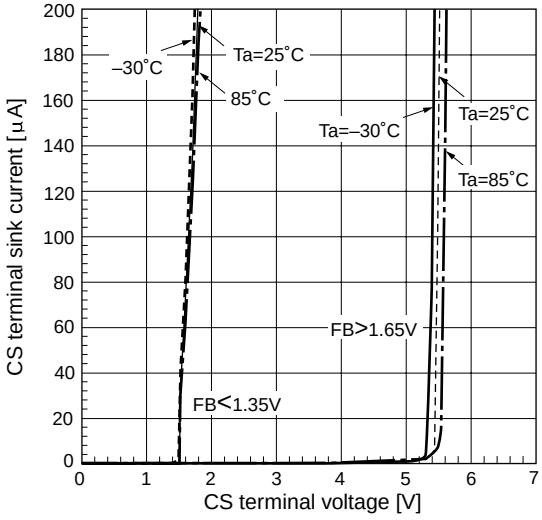
Undervoltage lock-out vs. ambient temperarure



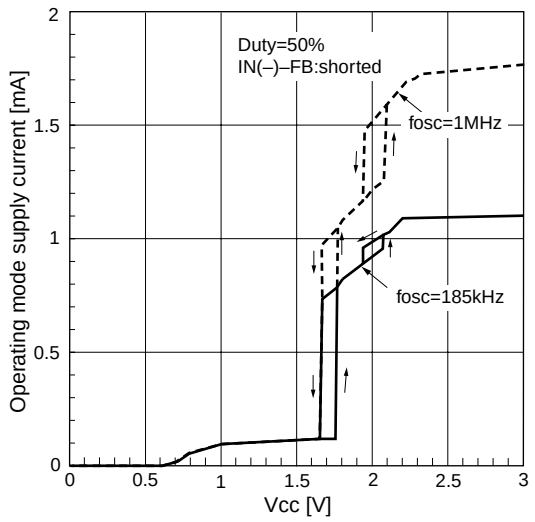
CS terminal ON/OFF threshold vs. ambient temperature



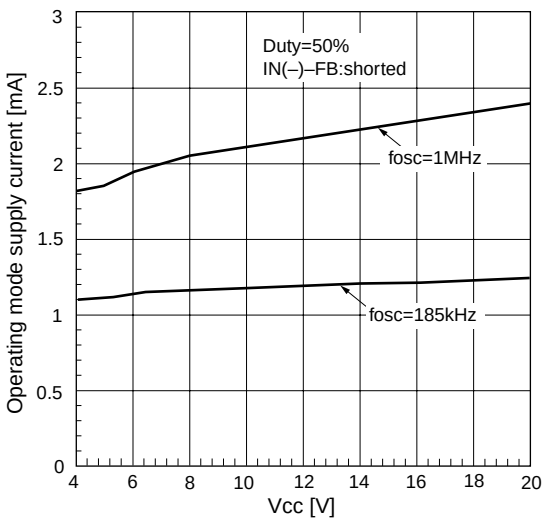
CS terminal voltage vs. CS terminal sink current



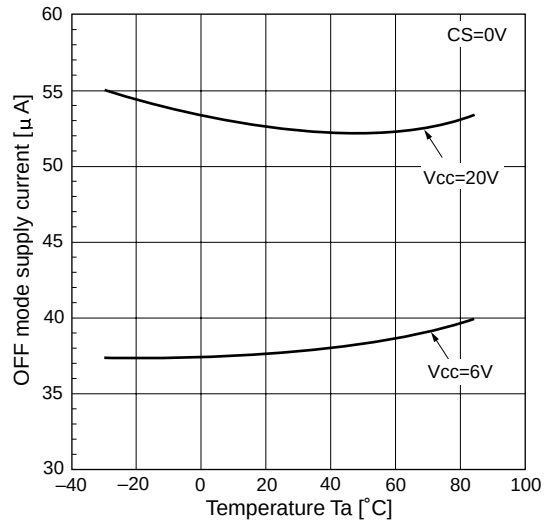
Operating mode supply current vs. Vcc



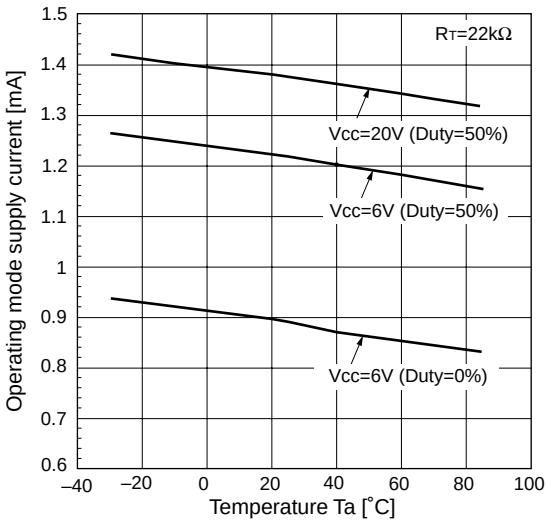
Operating mode supply current vs. Vcc



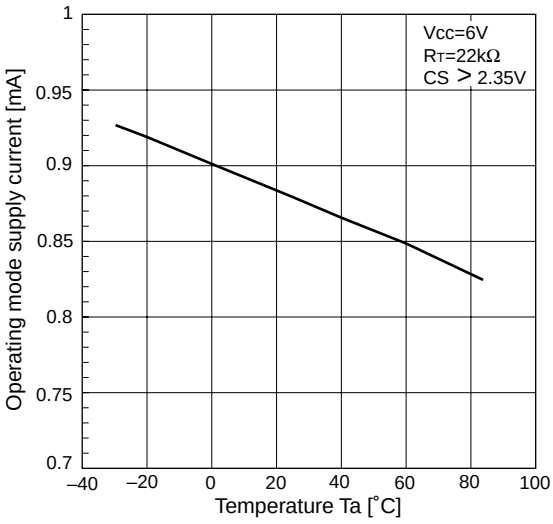
OFF mode supply current vs. temperature



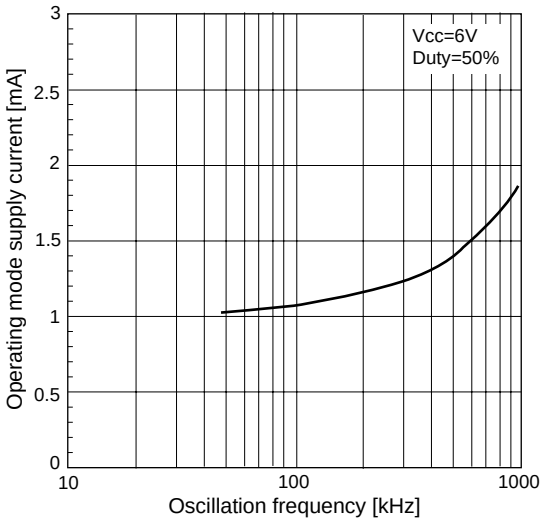
Operating mode supply current vs. temperature



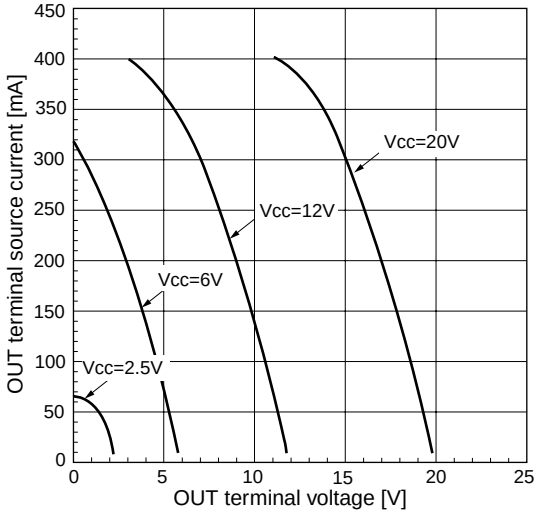
Latched mode supply current vs. temperature



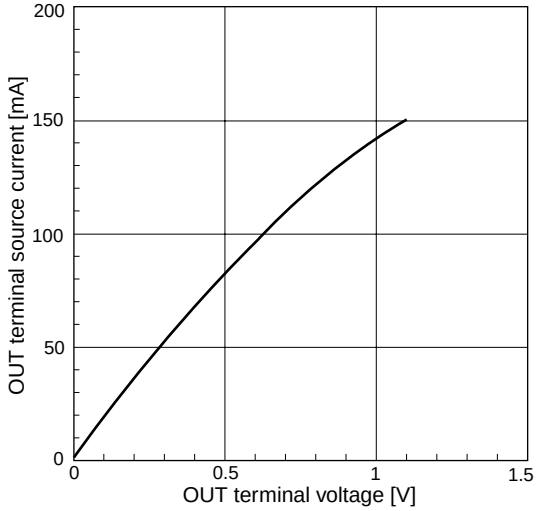
Oscillation frequency vs. operating mode supply current



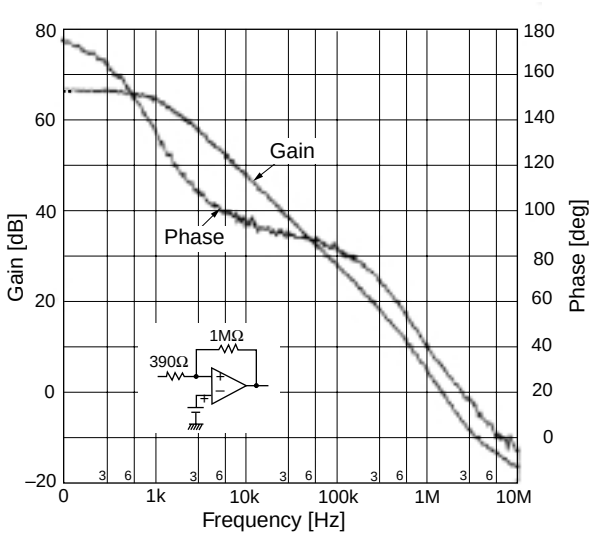
OUT terminal source current vs. OUT terminal voltage



OUT terminal sink current vs. OUT terminal voltage



Error amplifier gain and phase vs. frequency



■ Description of each circuit

1. Reference voltage circuit

This circuit consists of the reference voltage circuit using band gap reference, and also serves as the power supply of the internal circuit. The precision of output is 2.23V±3%.
It is stabilized under the supply voltage of 2.5V or over.
The precision of reference voltage of error amplifier circuit is 0.88V±2%, and the reference voltage circuit is connected to the non-inverting input of the error amplifier circuit.

2. Oscillator

The oscillator generates a triangular waveform by charging and discharging the built-in capacitor. A desired oscillation frequency can be determined by the value of the resistor "R_T" connected to the RT terminal (Fig. 1).
The built-in capacitor voltage oscillates between approximately 0.66V and 1.1V with almost the same charging and discharging gradients. You can set the desired oscillation frequency by changing the gradients using the resistor connected to the RT terminal. (Large R_T: Low frequency, small R_T: High frequency)
The oscillator waveform cannot be observed from the outside because a terminal for this purpose is not provided. The oscillator output is connected to the PWM comparator.

3. Error amplifier circuit

The IN(–) terminal (Pin 3) is an inverting input terminal.
The non-inverting input is internally connected to the reference voltage (0.88V±2%; 25˚C). The FB terminal (Pin 4) is the output of the error amplifier. Gain setting and phase compensation setting is done by connecting a capacitance and a resistor between the FB terminal and the IN(–) terminal. Vout which is the output voltage of DC to DC converter can be calculated by:

$$Vout = V_B \times \frac{R1 + R2}{R2}$$

Gain A_V between the Vout and the FB terminal can be calculated by:

$$AV = -\frac{R_{NF}}{R1}$$

4. PWM comparator

The PWM comparator has 4 input terminals. (Fig. 4)
The oscillator output ① is compared with the CS terminal voltage ②, and the error amplifier voltage ③, then, the lower voltage between ② and ③ is preferred.
While the preferred voltage is lower than the oscillator output, the PWM comparator output is Low. While the preferred voltage is higher than the oscillator output, the PWM comparator output is High (Fig. 5). When the IC starts, the capacitor connected to the CS terminal is charged through the resistor connected to the power supply, and then the output pulses begin to widen gradually as the operation of soft start.
In steady operation, the pulse width is determined based on the voltage of the error amplifier ③, and then the output voltage is stabilized. The Dead Time control voltage (④ DT voltage) of FA7700 and FA7701 has different characteristics to adjust the ICs to various types of power supply circuits being controlled and also to reduce external discrete components as many as possible. FA7700 is developed for fly-back circuits, and boost circuits, and the DT voltage is set in the IC so that the maximum output duty cycle is fixed to 80% min.. (Maximum output duty cycle changes according to operation frequencies. —See page 6 "Maximum output duty vs. temperature".)
It prevents magnetic saturation of the transformer or the like when a short-circuit in the output circuit occurs. FA7701 is developed for buck circuits, and it is designed for the maximum output duty cycle of 100%. The timing chart of PWM comparator is described in Fig. 5.

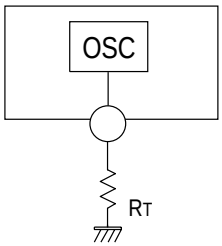


Fig. 1

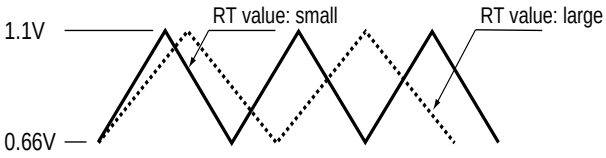


Fig. 2

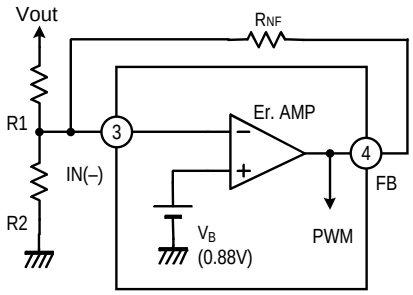


Fig. 3

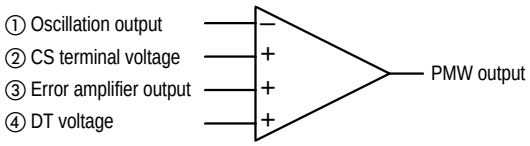


Fig. 4

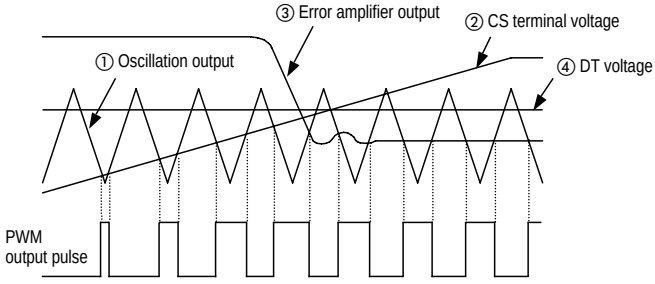


Fig. 5

5. Soft start function

As described in Fig. 6, RCS is connected between CS terminal and VCC terminal, and Cs is connected between CS terminal and GND. The voltage of CS terminal rises when starting the power supply, because Cs is charged by Vcc through Rcs. The soft start function starts by charging a capacitor Cs connected to PWM comparator. To estimate the soft start period, the time (ts) between the start and the moment when the width of output pulse reaches 50% is calculated by:

$$ts\ [ms] \fallingdotseq Cs \times Rcs \times 1n\left(\frac{Vcc}{Vcc - 0.88}\right)$$

Cs : Capacity of Cs [μF]
Rcs : Resistance of Rcs [kΩ]
Vcc : Supply voltage [V]

The maximum current flowing in Rcs should be within the recommended value (50μA max.).

$$\frac{Vcc - 1.5}{50\mu A + I_L} < Rcs\ [M\Omega] < \frac{Vcc - 1.5}{1\mu A + I_L}$$

(I_L: leak current of capacitor Cs)

Note: This IC operates ON/OFF function by the CS terminal (CS < 0.3V typ. : OFF), then it turns off the internal bias voltage VREF (off mode). Therefore, you can not connect the resistor "Rcs" between CS terminal and REF terminal, and can connect the resistor only to VCC terminal.

6. ON/OFF circuit

The ON/OFF function can be controlled by external signal to the CS terminal, the IC becomes off mode. When the CS terminal voltage is below 0.30V(typ.), the output of ON/OFF comparator C3 is set to LOW, and the internal power source VREF is shut off, then the IC is switched to the off mode. The power consumption in the off mode is 40μA(typ.). A sample circuit is given in Fig. 7.

7. Timer latch short-circuit protection circuit

The short-circuit protection circuit consists of two comparators C1, C2 (Fig. 6). In steady operation, the output of S.C.DET comparator C2 is set to High, and the CS terminal is clamped by the 1.5V Zener diode, because the output of error amplifier is about 1V. If the converter output voltage drops due to a short-circuit, when the output voltage of error amplifier rises excesses 1.5V, the output of S.C.DET comparator C2 is set to low, and then the clamp of Zener diode is turned off.
As a result, the voltage of CS terminal rises up to the lower value of either 5.5 V or the voltage of VCC terminal.
If the voltage of CS terminal excesses 2.2V, the output of S.C.P comparator C1 is set to high, and the circuit shuts down the output circuit of the IC. When it occurs, the current consumption of the IC is 0.9mA (typ.) because the IC is set to OFF latch mode. The period (tp) between the occurrence of a short-circuit in the converter output and the triggering of the short-circuit protection function can be calculated by the following expression:

$$tp\ [ms] \fallingdotseq Cs \times Rcs \times 1n\left(\frac{Vcc - 1.5}{Vcc - 2.2}\right)$$

Cs : Capacitance of Cs [μF]
Rcs : Resistance of Rcs [kΩ]
Vcc : Supply voltage [V]

Note: When the IC is used in a product with low VCC voltage, the period (tp) of the triggering of the short-circuit protection described above fluctuates significantly. Therefore, sufficient care should be taken in such cases.

Example When Rcs=750kΩ, Cs=0.1μF: Vcc=2.5V: tp ≒ 90ms
Vcc=3.6V: tp ≒ 30ms

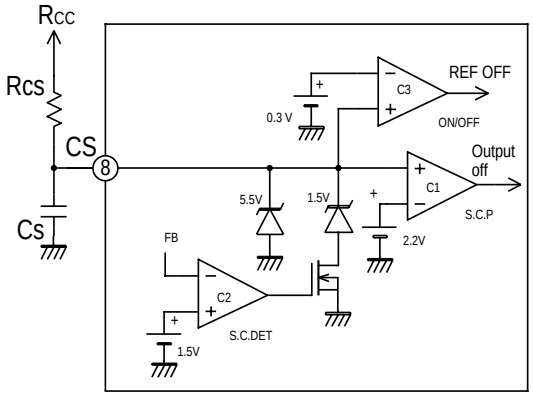


Fig. 6

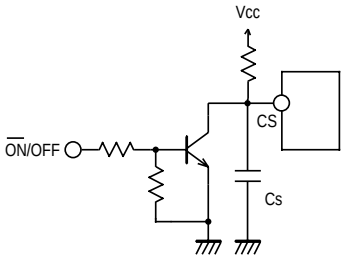


Fig. 7

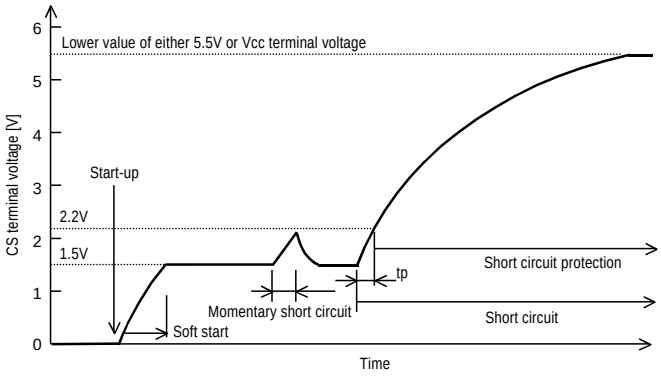


Fig. 8

You can reset the off latch mode operation of the short-circuit protection by either of the following ways: lowering the CS voltage below 2.03V (typ.); lowering the Vcc voltage below the Off threshold voltage of undervoltage lock out; 1.93V (typ.); lowering the voltage of FB terminal below 1.5V (typ.)
The off latch mode action cannot be triggered by externally applying voltage of over 2.2V forcibly to the CS terminal (1.5V, ZD clamped). Characteristics of the current and the voltage of CS terminal is shown in the characteristic curve (CS terminal voltage vs. CS terminal sink current) on page 6. Be sure to use the IC up to the recommended CS terminal current of 50µA.

8. Output circuit
The IC contains a push-pull output stage and can directly drive MOSFETs (FA7700: N ch, FA7701: P ch). The maximum peak current of the output stage is a sink current of +150mA, and a source current of –400mA. The IC can also drive NPN, and PNP transistors. The maximum peak current in such cases is ±50mA. Be sure to design the output current considering the rating of power dissipation.

9. Power good signal circuit/ Undervoltage lockout circuit
The IC contains a protection circuit against undervoltage malfunctions to protect the circuit from the damage caused by malfunctions when the supply voltage drops. When the supply voltage rises from 0V, the circuit starts to operate at VCC of 2.07V (typ.) and outputs generate pulses. If a drop of the supply voltage occurs, it stops output at VCC of 1.93V (typ.). when it occurs, the CS terminal is turned to Low level and then it is reset. The power good signal circuit monitors the voltage of REF terminal, and stops output until the voltage of REF terminal excesses approximately 2V to prevent malfunctions.

■ Design advice

1. Setting the oscillation frequency
As described in item 2 “Oscillator” of “Description of each circuit”, a desired oscillation frequency can be determined by the value of the resistor connected to the RT terminal. When designing an oscillation frequency, you can set any frequency between 50kHz and 1MHz. You can roughly obtain the oscillation frequency from the characteristic curve “Oscillation frequency (fosc) vs. timing resistor resistance(R_T)” or the value can be calculated by the following expression.

$$f_{OSC} = 3000 \times R_T^{-0.9}$$

$$R_T = \left(\frac{3000}{f_{OSC}}\right)^{1.11}$$

f_{OSC}: Oscillation frequency [kHz]
R_T: Timing resistor [kΩ]

This expression, however, can be used for rough calculation, the value obtained is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, be sure to verify the effectiveness of the values of the components in an actual circuit.

2. Operation around the maximum or the minimum output duties
As described in characteristic curves on page 5, “output duty cycle vs. FB terminal voltage (V_{FB})” and “output duty cycle vs. CS terminal voltage (Vcs)”, the linearity of the output duty of this IC drops around the minimum output duty and the maximum output duty (FA7701 only). This phenomena are conspicuous when operating in a high frequency (when the pulse width is narrow). Therefore be careful when using high frequency.

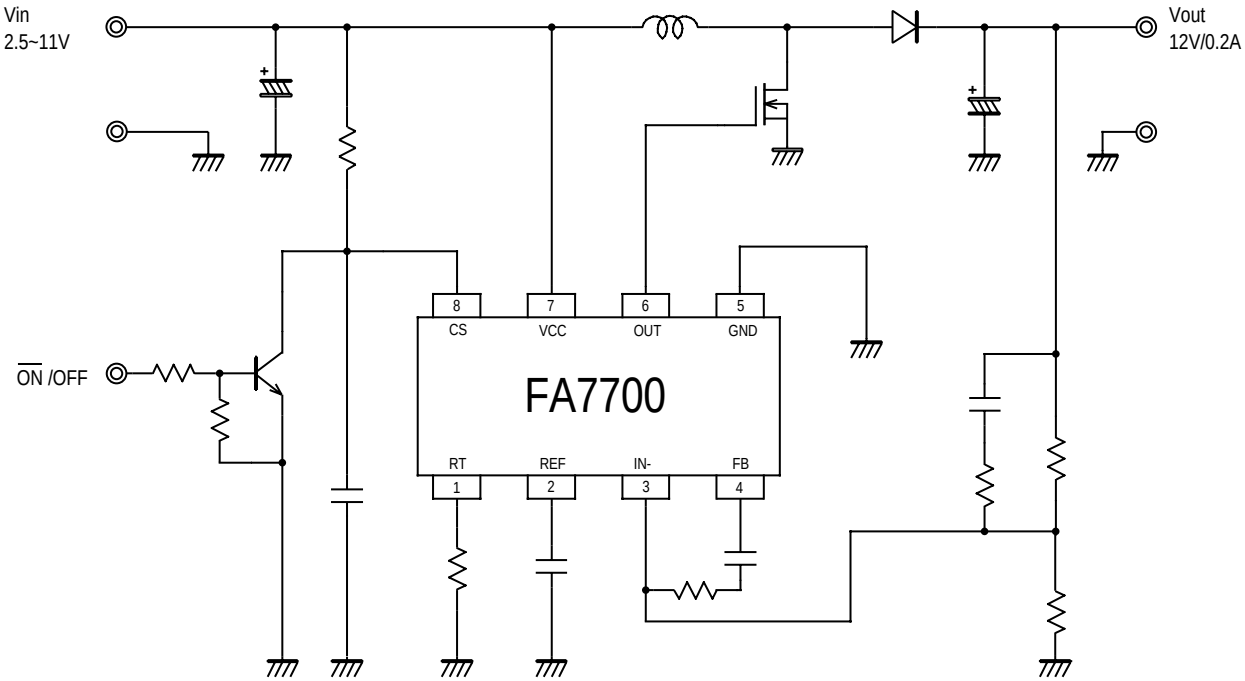
3. Restriction of external discrete components
To achieve a stable operation of the ICs, the value of external discrete components connected to Vcc, R_{EF}, CS, FB terminals should be within the recommended operational conditions.

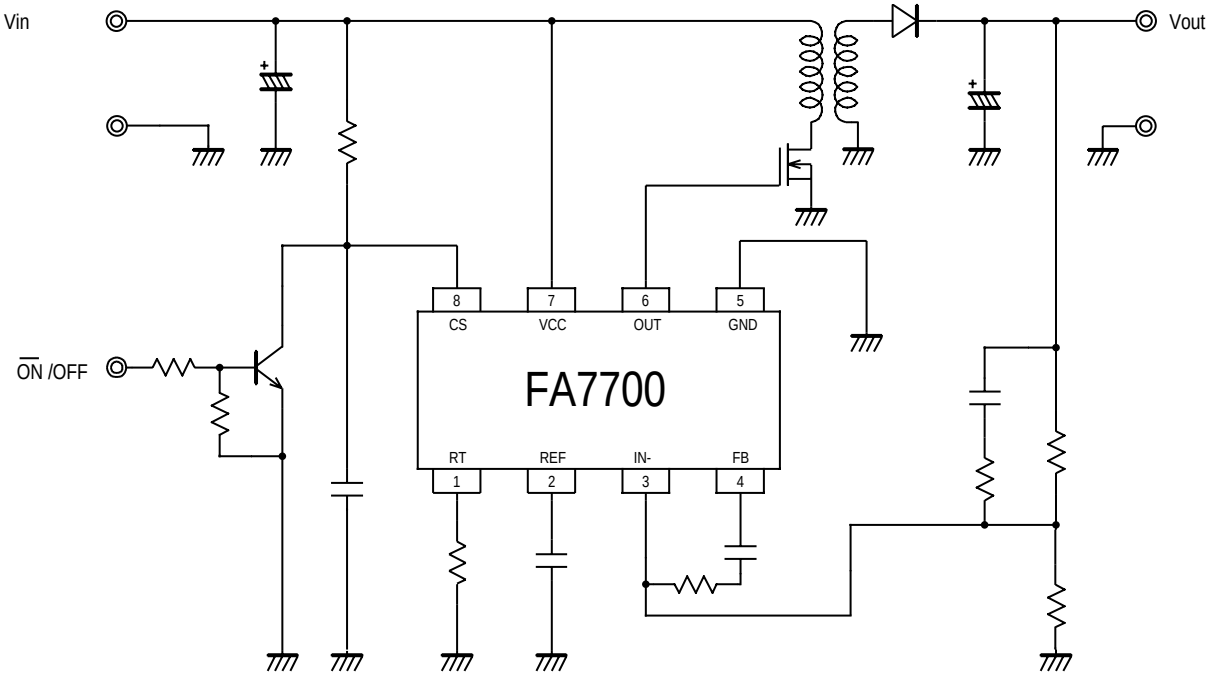
4. Loss calculation
Since it is difficult to measure IC loss directly, the calculation to obtain the approximate loss of the IC connected directly to a MOSFET is described below.
When the supply voltage is Vcc, the current consumption of the IC is Icc, the total input gate charge of the driven MOSFET is Qg, the switching frequency is fsw, the total loss Pd of the IC can be calculated by:
$Pd \fallingdotseq Vcc \times (Icc + Qg \times fsw)$.
The values in this expression is influenced by the effects of the dependency of supply voltage, the characteristics of temperature, or tolerance. Therefore, be sure to verify appropriateness of the value considering the factors above under all applicable conditions.

Example:
When V_{CC} = 6V, in the case of a typical IC, from the characteristic curve, Icc=1.2mA. When operating in Qg = 6nC, fsw = 500kHz, Pd should be:
$Pd \fallingdotseq 6 \times (1.2mA + 6nC \times 500kHz) \fallingdotseq 25.2mW$

■ Application circuit

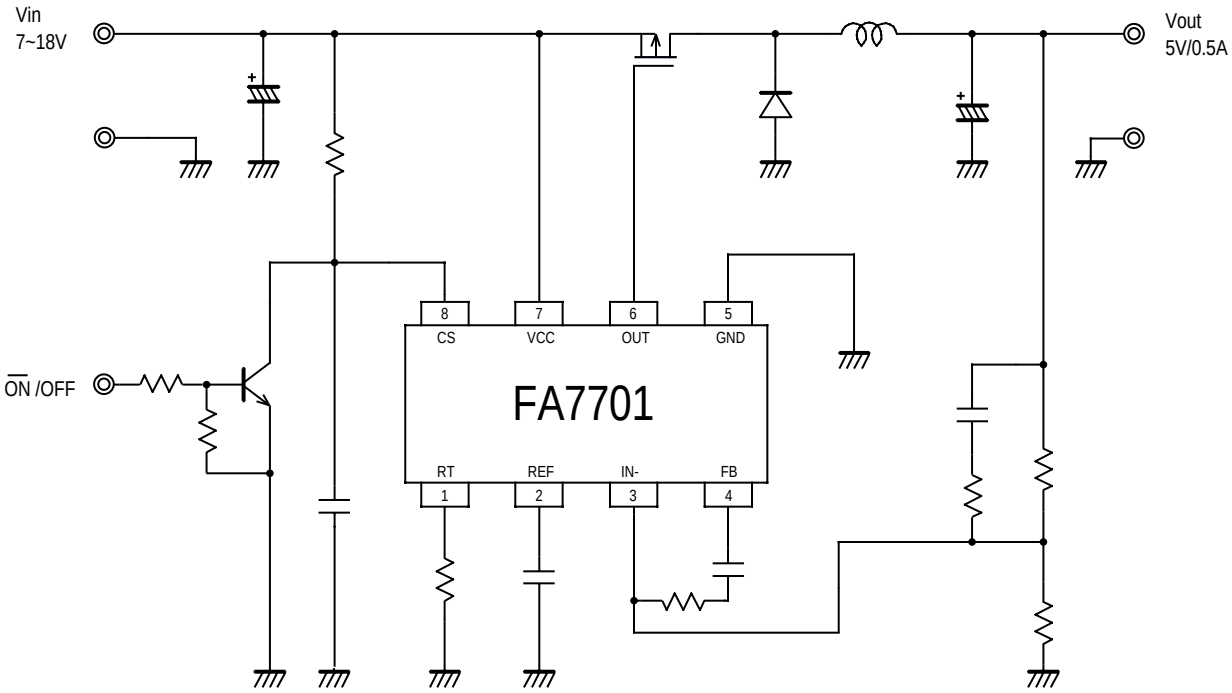
● FA7700





■ Application circuit

● FA7701



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.