

FAN3506

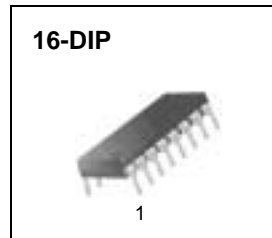
PC SMPS Secondary Side Control IC

Features

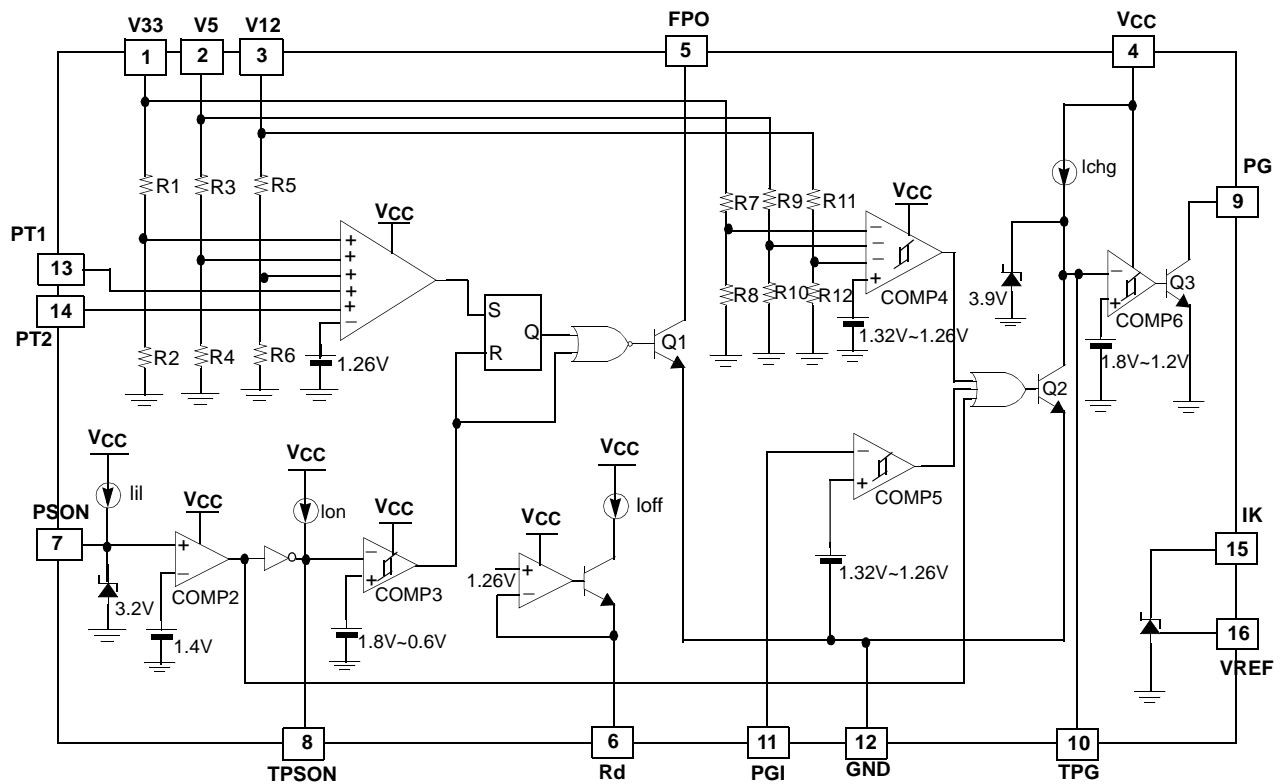
- Few External Components
- Low Voltage Operation ($V_{cc_min}=4.5V$)
- Over Voltage Protection for 3.3V/5V/12V Output
- Two Protection Inputs (PT1, PT2)
- Fault Protection Output with Open Collector
- Power Supply on/off Delay Time Control (PSON)
- Latch Function Controlled by PSON and Protection
- Power Good Signal Generator with Hysteresis
- 300ms(Typ) Power Good Delay
- Programmable Shunt Regulator Trimmed to $\pm 2\%$
- 16-Pin Dual In-line Package (16-DIP-300)

Description

The FAN3506 is complete housekeeping circuitry for use in the secondary side of PC SMPS (Switched Mode Power Supply). It contains various functions, which are over voltage protection including two extra protection inputs, power supply on/off delay control and power good signal generator. Especially, it contains a programmable shunt regulator for output feedback and the reference voltage is trimmed to $\pm 2\%$. The FAN3506 is available in 16-DIP.



Block Diagram



Pin Description

No	Name	I/O	Function
1	V33	I	+3.3V Output Voltage of SMPS Secondary Side
2	V5	I	+5V Output Voltage of SMPS Secondary Side
3	V12	I	+12V Output Voltage of SMPS Secondary Side
4	VCC	I	Supply Voltage. +5Vsb(+5V Standby Supply) is Recommended for Vcc. The Operating Range is 4.5V~15V. Vcc=5V, Ta=25°C at test.
5	FPO	O	Fault Protection Output(FPO) With Open Collector Structure. This Signal Controls the Primary Switch(PWM IC) Through an Opto-coupler. Maximum Current Rating is 20mA. When FPO = "Low", the Main SMPS is Operational and if FPO = "High", the Main SMPS is Turned-off.
6	Rd	-	OFF Delay Resistor. This Block is Made up of a Buffer With Vout = 1.258V. A Resistor Should be Connected to the Pin6 for Determination of Off Delay Current. The Recommended Value of Rd Resistor is 28kΩ at Ctpson=0.22uF. The off Delay Time is Gotten by Following Equation. $T_{off} = [Ctpson * (V8max - VthL)] / (1.258V/Rrd)$
7	PSON	I	Power Supply On/Off (Remote On/Off) Input. It is TTL Operation and its Threshold Voltage is 1.4V. The Maximum Voltage of Pin7 is About 3.9V(Typ), With Absolutely Maximum Voltage, 5.25v. If Pson Is Low, Fpo Is Low, Too. That Means The main SMPS is Operation(Active). When PSON is High, then FPO is High and the Main SMPS is off.
8	TPSON	-	Power Supply On/Off Delay. Ton/Toff = 24ms/8ms(Typ) with Ctpson=0.22uF & Rd=28kΩ. Its High/Low Threshold Voltages 1.8V/0.6V and the Maximum Voltage After Full Charging is About 2.2V. So Vcharge = VthH = 1.8V and Vdischg = V8max - VthL = 1.6V. Each Delay Time is Decided by the Following Equations, $T_{on} = (Ctpson * VthH) / I_{on}$, $T_{off} = [Ctpson * (V8max - VthL)] / (Vrd/Rrd)$.
9	PG	O	Power Good Signal Output with Open Collector. The Maximum Current Rating is 20mA. PG High Means that the Power is Good for Operation and PG low Means Power Fail.
10	TPG	-	PG Delay. $T_d = 300ms(Typ)$ with Ctpg=2.2uF. The Threshold Voltage is 1.8V and the Delay Time is Decided by the Following Equation, $T_d = (Ctpg * Vth) / I_{chg} = 1.8Ctpg / I_{chg}$.
11	PGI	I	Power Good Signal Input. Its Threshold Voltage is 1.26V When the PGI Voltage Drops From High to Low.
12	GND	-	Ground
13	PT1	I	Protection Input 1. This can be Used for an Adjustable OVP or Another Protection Input.
14	PT2	I	Protection Input 2. This can be Used for an Adjustable OVP or Another Protection Input.
15	IK	I	Cathode of the Programmable Shunt Regulator. Absolute Min/Max Current Rating is 1mA/30mA.
16	VREF	I	Reference of Programmable Shunt Regulator. This Circuit is Prepared for Feedback of Output Voltage as it Equals to KA431(LM431). It is Trimmed to ±2%.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	4.5 ~ 15	V
FPO (Fault Protection Output) Voltage	V _{FPO}	20	V
FPO Maximum Current	I _{FPO}	20	mA
PGI Maximum Voltage	V _{pgi}	20	V
PG Output Maximum Current	I _o (PG)	20	mA
Cathode Voltage	V _{ka}	20	V
Cathode Current for IK	I _K	1 ~ 30	mA
Power Dissipation	P _D	1	W
Operating Temperature Range	T _{OPR}	-25 ~ +80	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Electrical Characteristics

(V_{CC} = 5V, T_a = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION SECTION						
OVP Detecting Voltage for 3.3V	V _{OVP33}	PSON=0V	3.9	4.1	4.3	V
OVP Detecting Voltage for 5V	V _{OVP5}	PSON=0V	5.7	6.1	6.5	V
OVP Detecting Voltage for 12V	V _{OVP12}	PSON=0V	13.6	14.3	15.0	V
Protection Input Voltage 1	V _{pt1}	PSON=0V	1.21	1.26	1.31	V
Protection Input Voltage 2	V _{pt2}	PSON=0V	1.21	1.26	1.31	V
POWER SUPPLY ON/OFF SECTION (PSON)						
PSON Input Threshold Voltage	V _{th}	PSON=0V : 0V to 2V	1	1.4	1.8	V
PSON Input Open Voltage	V _{ih}	PSON : Open	2	-	5.25	V
PSON Input Low Current	I _{il}	PSON=0V	0	-	-1	mA
PSON Delay Charging Current	I _{on}	PSON=TPSON=0V	-10	-16	-24	uA
Buffer Output Voltage	V _{Rd}	I _{sink} =45uA, 200uA	1.21	1.26	1.31	V
Pin8 Clamping Voltage	V _{8max}	PSON=0V	2.0	2.2	2.4	V
High Threshold for On/Off Delay (Note1)	V _{thH}	TPSON : 0V to 2.2V	1.6	1.8	2.0	V
Low Threshold for On/Off Delay (Note2)	V _{thL}	TPSON : 2.2V to 0V	0.4	0.6	0.8	V
Power Supply ON Delay Time (Note3)	T _{on}	C _{pin8} =0.22μF, R _d =28kΩ	16	26	36	msec
Power Supply OFF Delay Time (Note4)	T _{off}	C _{pin8} =0.22μF, R _d =28kΩ	4	8	14	msec
FPO Saturation Voltage	V _{sat} (FPO)	I _o =10mA	-	0.2	0.4	V
FPO Leakage Current	I _{leak} (FPO)	FPO=20V	0	0.01	1	uA

Electrical Characteristics (Continued)

(VCC= 5V, Ta = 25°C, unless otherwise specified)

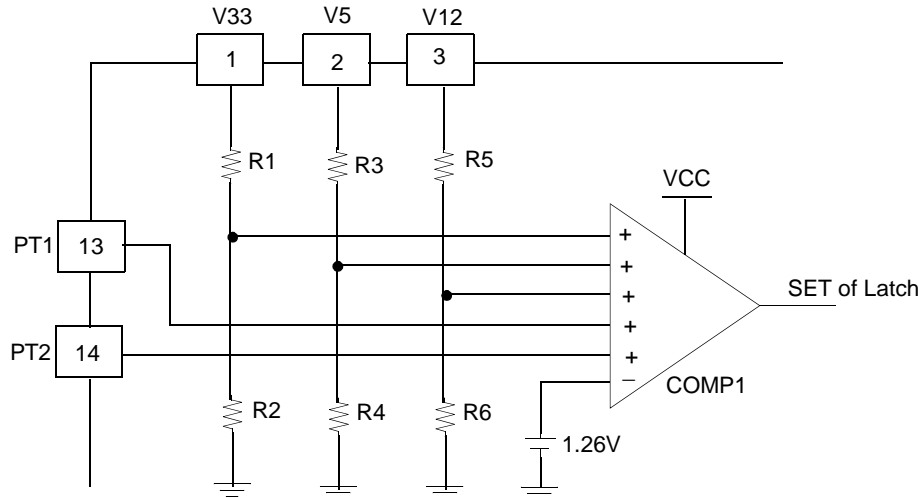
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER GOOD SECTION						
PGI Threshold Voltage	V _{pgi}	PGI : 1.5V to 1V	1.21	1.26	1.31	V
V33 Under Voltage Level	V _{uv33}	V33 : 3.3V to 2V	2.66	2.8	2.94	V
V5 Under Voltage Level	V _{uv5}	V5 : 5V to 3.5V	4.1	4.3	4.5	V
V12 Under Voltage Level	V _{uv12}	V12 : 12V to 9V	9.8	10.3	10.8	V
Pin10 Clamping Voltage	V10 _{max}	TPG : Open	3.4	3.9	4.4	V
PG Delay Comparator Threshold Voltage	V _{th} (TPG)	TPG : 0V to 2.5V	1.5	1.8	2.1	V
PG Delay Comparator Hysteresis Voltage	HY	TPG : 2.5V to 0V	0.3	0.6	0.9	V
Charging Current for PG Delay	I _{chg}	TPG = 0V	-9	-15	-23	uA
PG Delay Time	T _d (PG)	C _{pin10} = 2.2uF	100	300	500	msec
PG Output Rising Time (Note5)	T _r	C _{pin9} = 0.1uF	-	1	-	usec
PG Output Falling Time (Note6)	T _f	C _{pin9} = 0.1uF	-	1	-	usec
PG Output Saturation Voltage	V _{sat} (PG)	I _{sink} = 15mA	-	0.2	0.4	V
PG Output Leakage Current	I _{leak} (PG)	V(PG) = 20V	0	0.01	1	uA
PROGRAMMABLE SHUNT REGULATOR (KA431) SECTION						
Reference Input Voltage	V _{ref}	I _K = V _{REF} , I _K = 1mA	2.45	2.50	2.55	V
Load Regulation	V _{ref}	I _K = 1mA to 10mA	-	5	15	mV
Temperature Stability (Note7)	ΔV _{ref} /ΔT	T _a = -25 ~ +85°C	-	4.5	17	mV
Output Sinking Current Capability	I _{sink}	-	10	25	-	mA
Gain Bandwidth (Note8)	GBW	GV = 1	-	1	-	MHz
TOTAL DEVICE						
Supply Current	I _{cc}	PSON = 2V	-	3	8	mA

Note :

1. Power Supply ON Delay (PSON :High → Low). Power Supply is Active when PSON is Low.
2. Power Supply OFF Delay (PSON :Low → High). Power Supply is Off when PSON is High.
3. T_{on} = (C_{pin8} * V_{on}) / I_{on} = (C_{pin8} * V_{thH}) / I_{on}
4. T_{off} = (C_{pin8} * V_{off}) / I_{off} = [C_{pin8} * (V_{8max} - V_{thL})] / (V_{Rd} / R_d)
- 5,6,7,8 : These parameters, although guaranteed, are but not 100% tested in production.

Block Description & Application Hints

1. OVP Block



OVP function is simply realized by connecting Pin1, Pin2, Pin3 to each secondary output. R1,2,3,4,5,6 are internal resistors of the IC. Each OVP level is determined by resistor ratio and the typical values are 4V/6.1V/14.2V.

- OVP Detecting voltage for +3.3V

$$\cdot V_{ovp33} = (R1+R2)/R2 * 1.26V = 4.1V(Typ)$$

- OVP Detecting voltage for +5V

$$\cdot V_{ovp5} = (R3+R4)/R4 * 1.26V = 6.1V(Typ)$$

- OVP Detecting voltage for +12V

$$\cdot V_{ovp12} = (R5+R6)/R6 * 1.26V = 14.3V(Typ)$$

Especially, Pin13 & Pin14 are prepared for extra OVP inputs or another protection signal, respectively. That is, if you want over voltage protection of extra output voltage, then you can make a function with two external resistors.

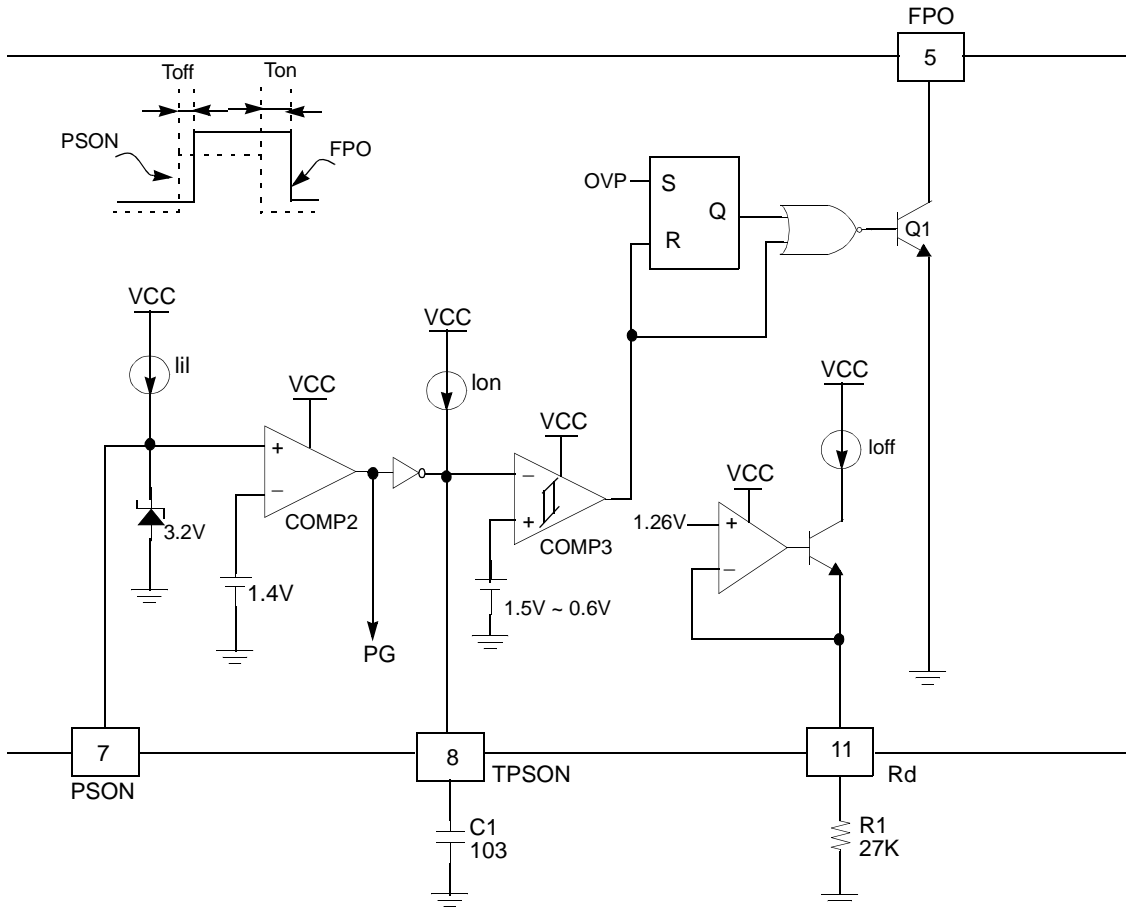
- Threshold Voltage of Protection Input 1 : $V_{pt1} = 1.26V$

- Threshold Voltage of Protection Input 2 : $V_{pt1} = 1.26V$

OVP function operates without delay time. In the case of OVP, system designer should know a fact that the main power can be dropped after a little time because of system delay, even if FPO is triggered by OVP.

So when the OVP level is tested with a set, you should check the secondary outputs(+3.3V/+5V/+12V) and FPO(Pin5) simultaneously. you can know the each OVP level as checking each output voltage in just time that FPO is triggered from low to high.

2. PSON & ON /OFF Delay Block



PSON & On/Off Delay Block is controlled by a Microprocessor.

If a high signal is supplied to the PSON(Pin7), the output of COMP2 becomes high status. The output signal is transferred to On/Off delay block and PG block.

If no signal is supplied to Pin7, Pin7 maintains high status(=3.2V) for the internal pull-up resistor.

When PSON is high, it produces FPO(Pin5) "High" signal after OFF delay time (about 8ms) for stabilizing system.

Then, all outputs (+3.3V, +5V, +12V) are grounded.

When PSON is changed to "Low", it produces FPO "Low" signal after ON delay time (about 26ms) for stabilizing the system.

If PSON is low, then FPO is low. That means the main SMPS is Active(operational). When PSON is high, FPO is high and the main SMPS is turned-off.

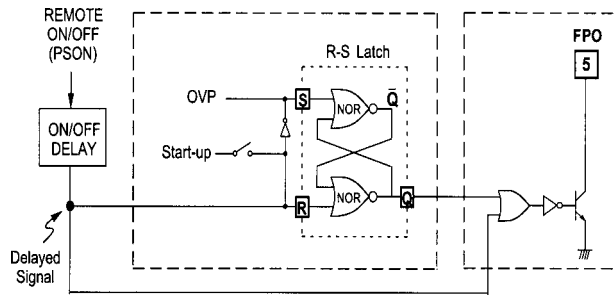
On/Off Delay Time can be calculated by following equation. 0.22uF Capacitor is recommended for following equations.

$$- \text{Ton} = (\text{Ctpson} * \text{VthH}) / \text{Ion} = (0.22\mu\text{F} * 1.8\text{V}) / 16\mu\text{A} = 26\text{ms}$$

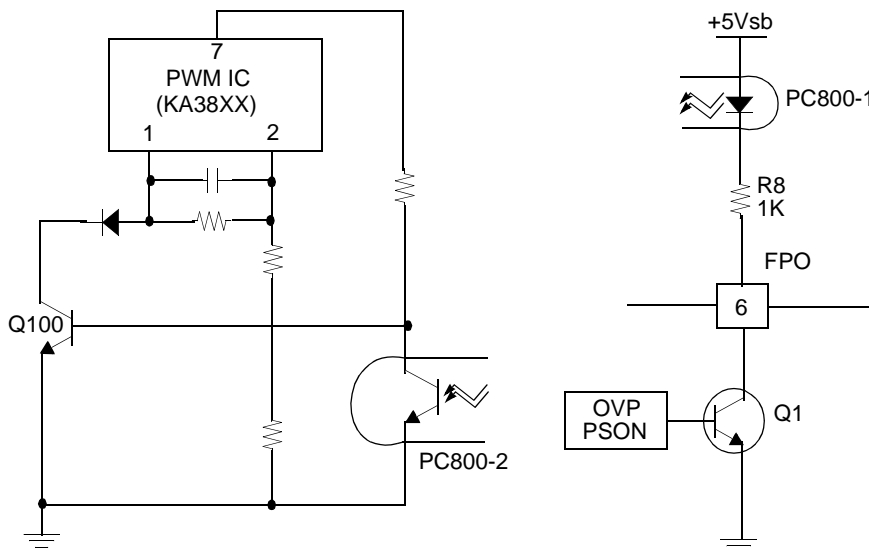
$$- \text{Toff} = [\text{Ctpson} * (\text{V8max} - \text{VthL})] / \text{Ioff} = [\text{Ctpson} * (\text{V8max} - \text{VthL})] / (\text{VRd} / \text{Rd})$$

Because Ion current for charging is fixed by internal current source, On delay time is varied by the capacitor value. On the contrary, Off Delay time is decided by the Rd value. If the Rd is 27K(Recommended) and the Delay capacitor value is 0.22uF, Toff is 8ms(Typ).

3. Latch & FPO Output



OVP	SET	RESET	Qn+1	Qn
L	L	L	Qn	Qn
L	L	H	L	H
H	H	L	H	L
H	H	H	L	H



Power Good Signal Generator circuits generate "On & Off" signal depending on the status of output voltage to prevent the malfunctions of following systems like microprocessor and etc. from unstable outputs at power on & off .

At Power On, it produces PG "High" signal after some delay (300ms_Typ) for stabilizing outputs.

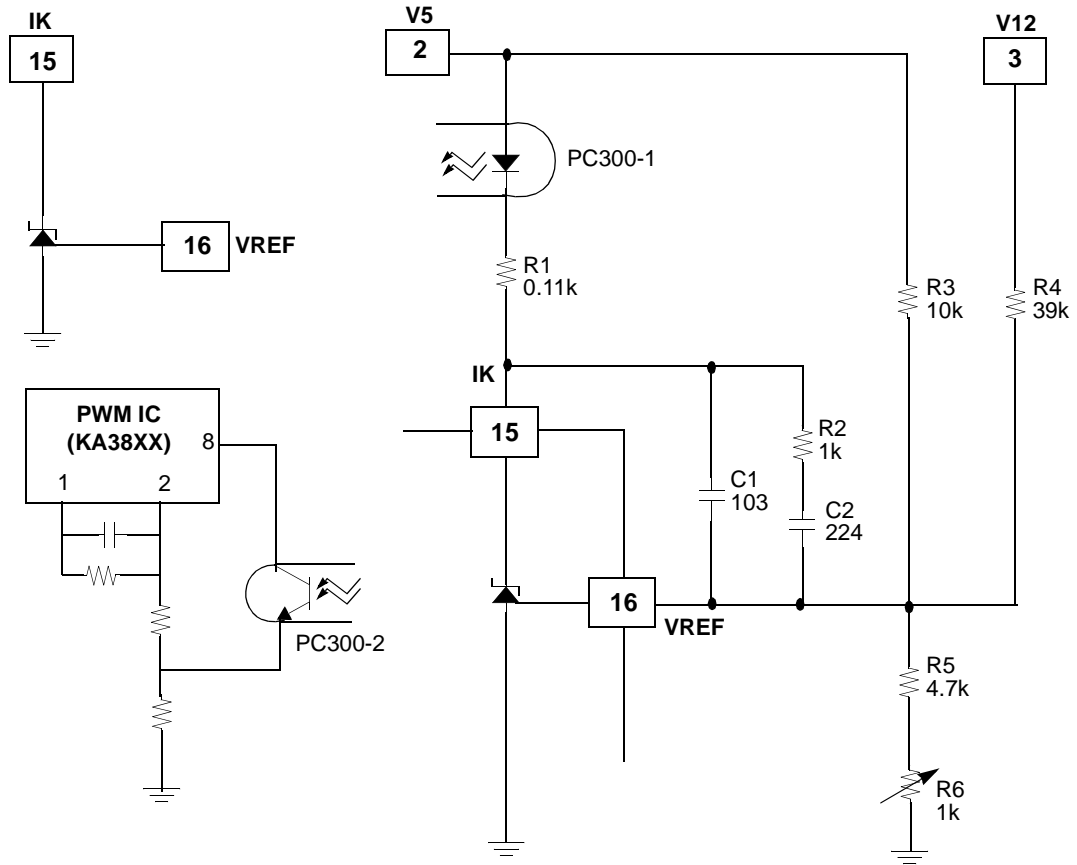
At power Off, it produces PG "Low" signal without delay by sensing the status of power source for protecting following systems. COMP6 creates PG "Low" without delay when +5V output falls to less than 4.3V to prevent some malfunction at transient status, thus it improves system stability. FAN3506 detects the Under Voltage level of three outputs(+3.3V/+5V/+12V) and PGI, respectively.

- UV Deducing Level of +3.3V : $V_{uv33} = 2.8V(Typ)$
- UV Deducing Level of +5V : $V_{uv5} = 4.3V(Typ)$
- UV Deducing Level of +12V : $V_{uv12} = 10.3V(Typ)$
- UV Deducing Level of PGI : $V_{pgi} = 1.26V(Typ)$

When PSON signal is high, it generates PG "Low" signal without delay. It means that PG becomes "Low" before main power is grounded. PG delay time($T_d(PG)$) is determined by capacitor value, threshold voltage of COMP6 and the charging current and its equation is as following.

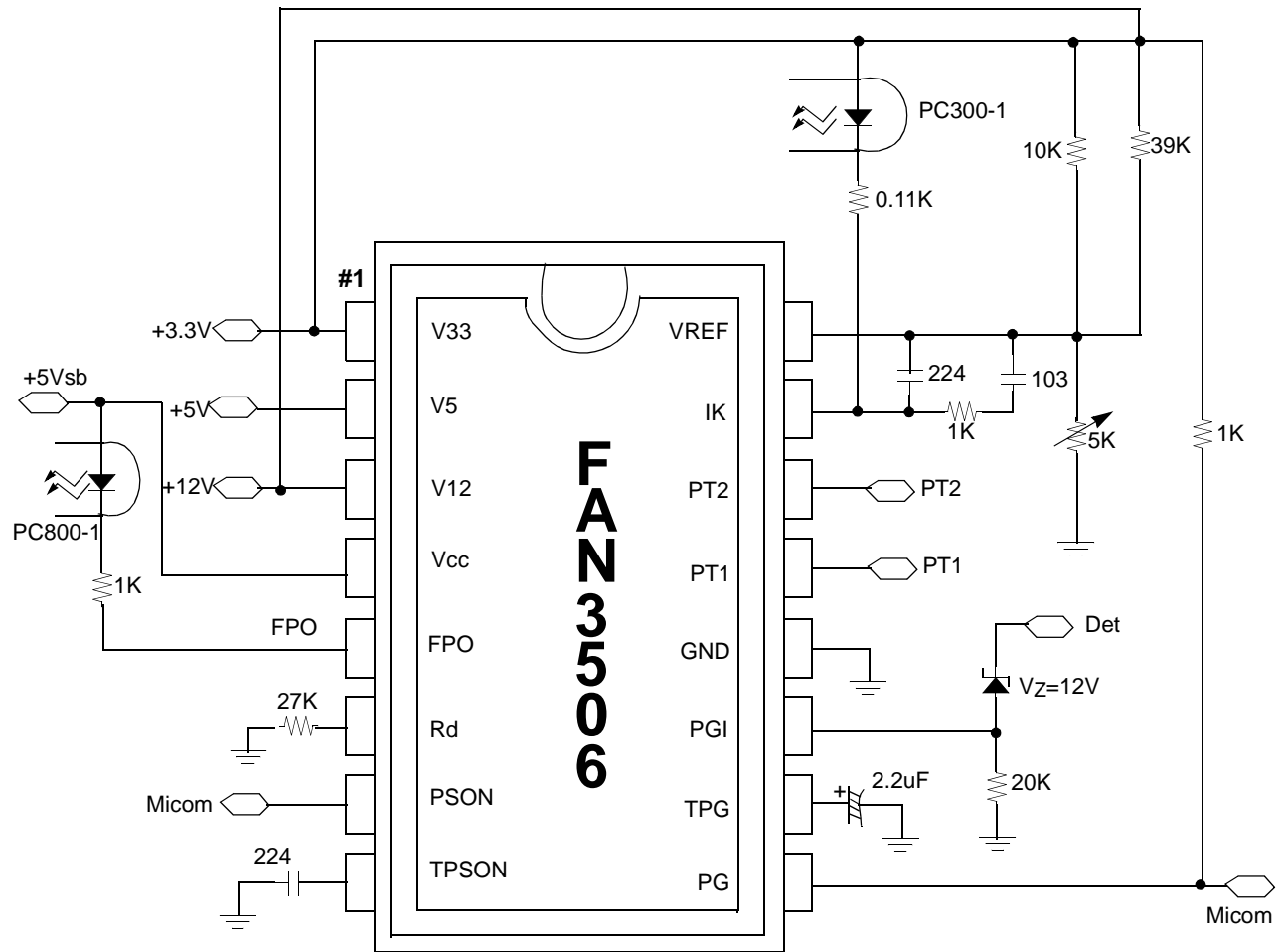
$$T_d(PG) = (C_{tpg} * V_{thH}) / I_{chg} = 300ms(Typ)$$

4. Programmable Shunt Regulator

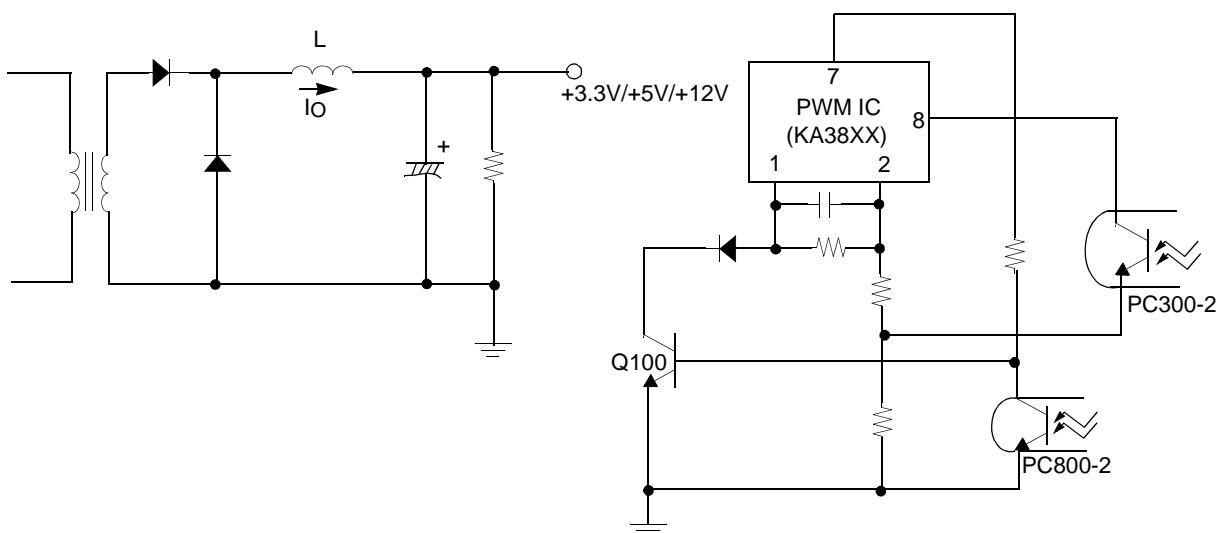


The core of the circuit equals to KA431(LM431) and Vref1 is trimmed to $\pm 2\%$ (2.45V ~ 2.55V) and it is for corrective output voltages (+5V/+12V). +5V/ +12V output voltages are determined by the resistor ratio of R3, R4, R5, R6. A photo coupler is used in order to control PWM IC in the primary side. R1 determines the bias current of the shunt regulator and 110 Ω is appropriate value. The resistor value can be changed by set condition and requirements. C1 and R2, C2 are the compensation circuit for stability.

Typical Application Circuit



[Complete Housekeeping Circuit using the FAN3506]



Typical Performance Characteristics

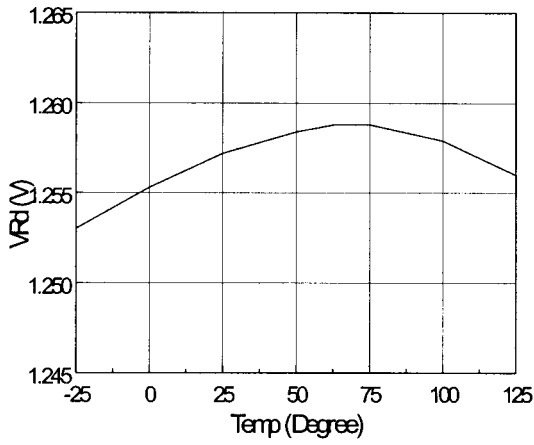


Figure 1. Temperature Stability for VRd

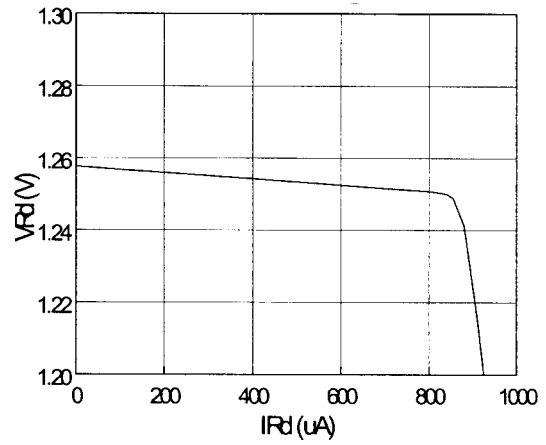


Figure 2. Buffer Output Voltage vs. IRd

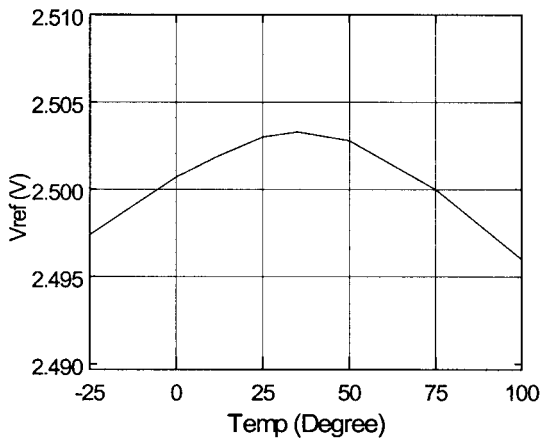


Figure 3. Temperature Stability for Vref

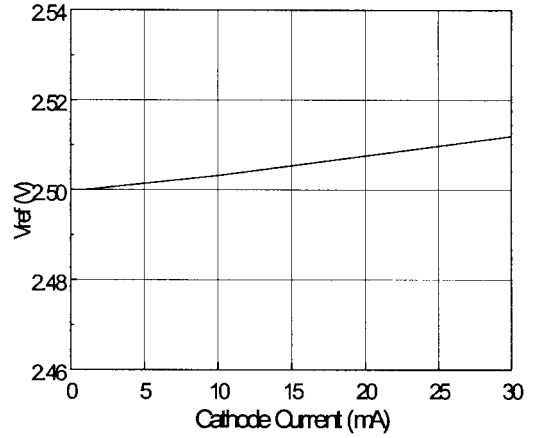


Figure 4. Current Stability of Vref

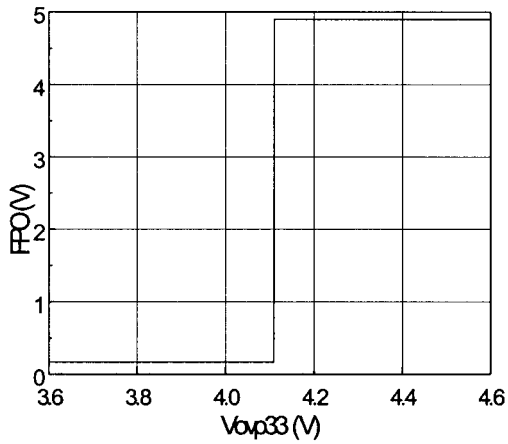


Figure 5. OVP Detecting Voltage for 3.3V

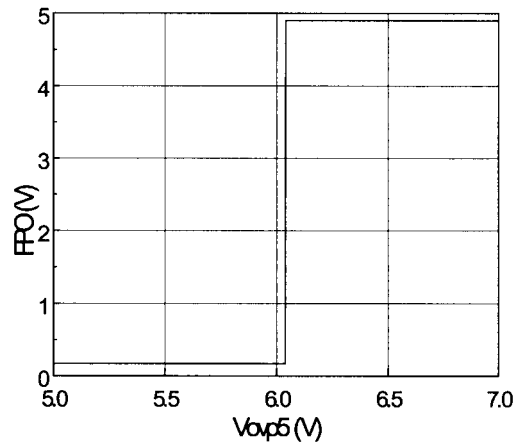


Figure 6. OVP Detecting Voltage for 5V

Typical Performance Characteristics (Continued)

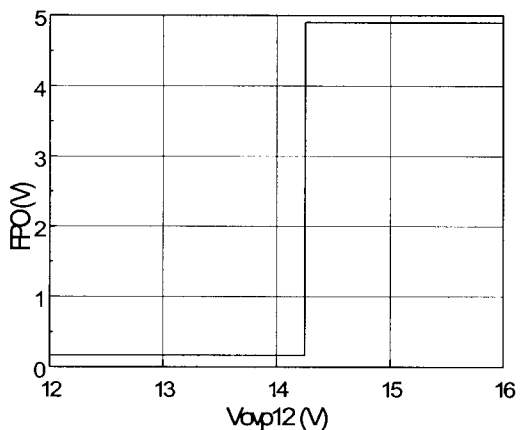


Figure 7. OVP Detecting Voltage for 12V

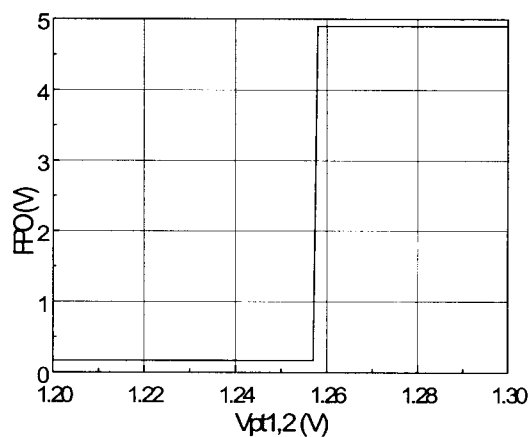


Figure 8. Protection Input Voltage 1,2

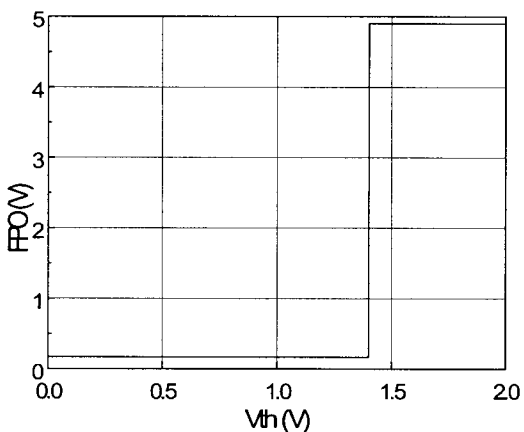


Figure 9. PSON Input Threshold Voltage

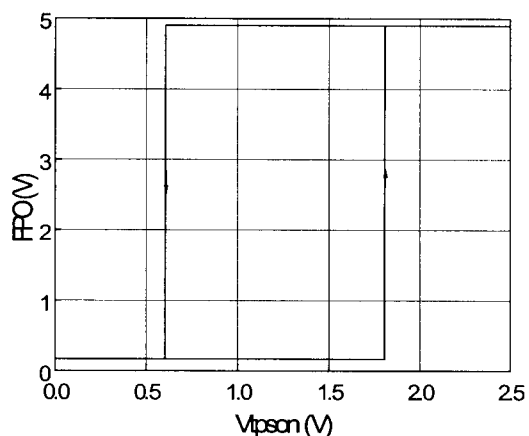


Figure 10. High/Low Threshold of On/Off Delay

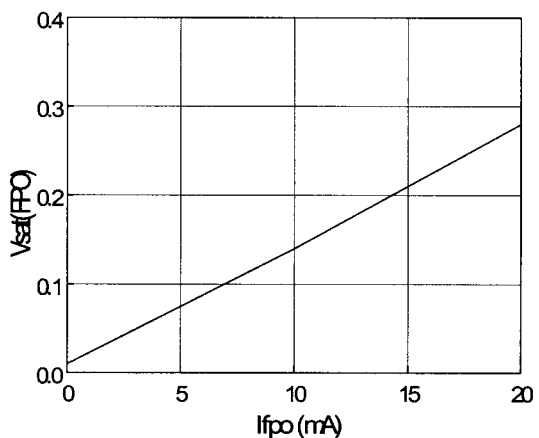


Figure 11. FPO Saturation Voltage

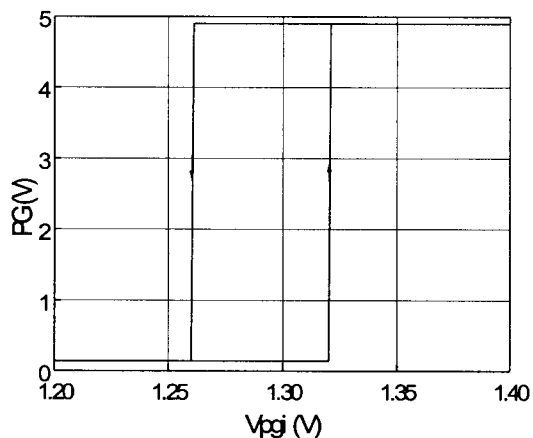


Figure 12. PGI Threshold Voltage

Typical Performance Characteristics (Continued)

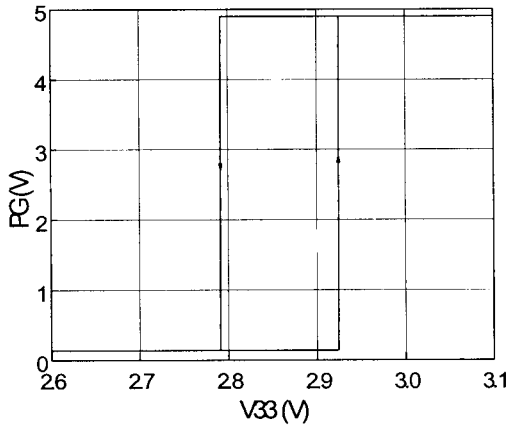


Figure 13. V33 Under Voltage Level

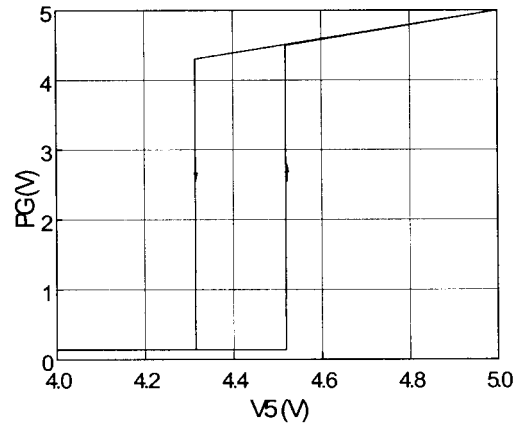


Figure 14. V5 Under Voltage Level

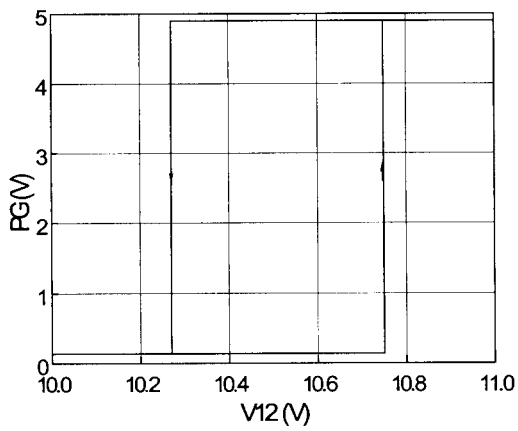


Figure 15. V12 Under Voltage Level

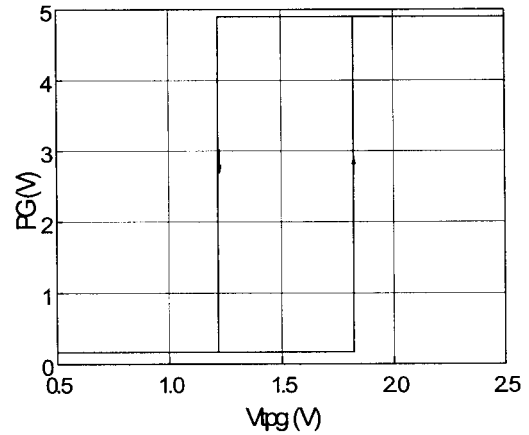


Figure 16. High/Low Threshold of PG Delay COMP

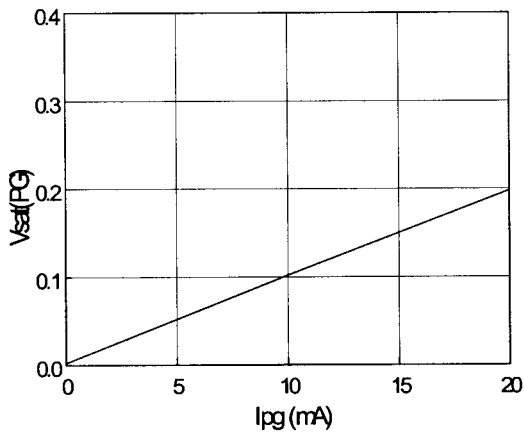


Figure 17. PG Saturation Voltage

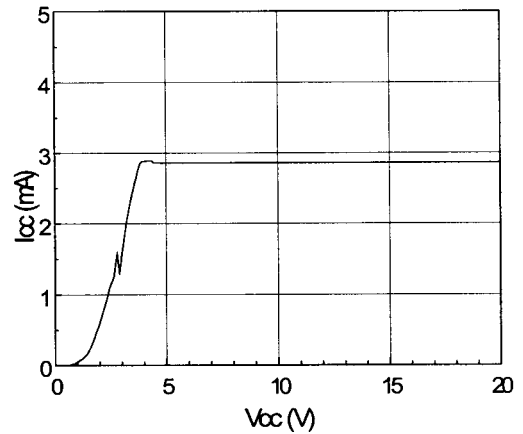


Figure 18. Supply Current of Vcc

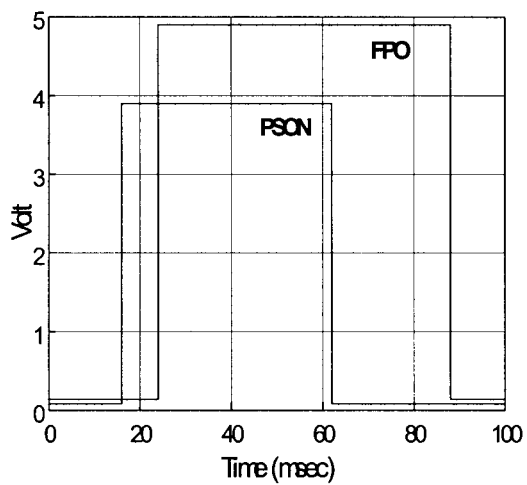
Typical Performance Characteristics (Continued)

Figure 19. Power Supply On/Off Delay Time

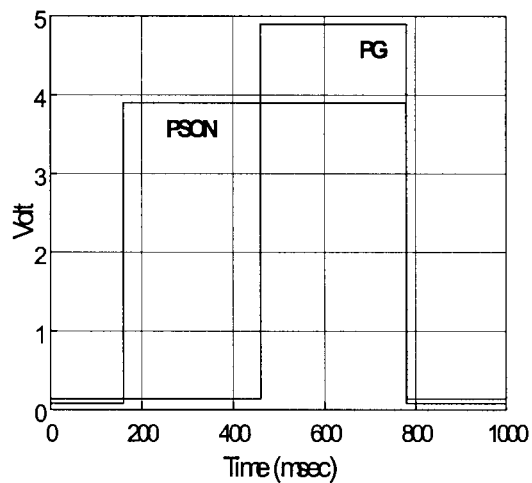


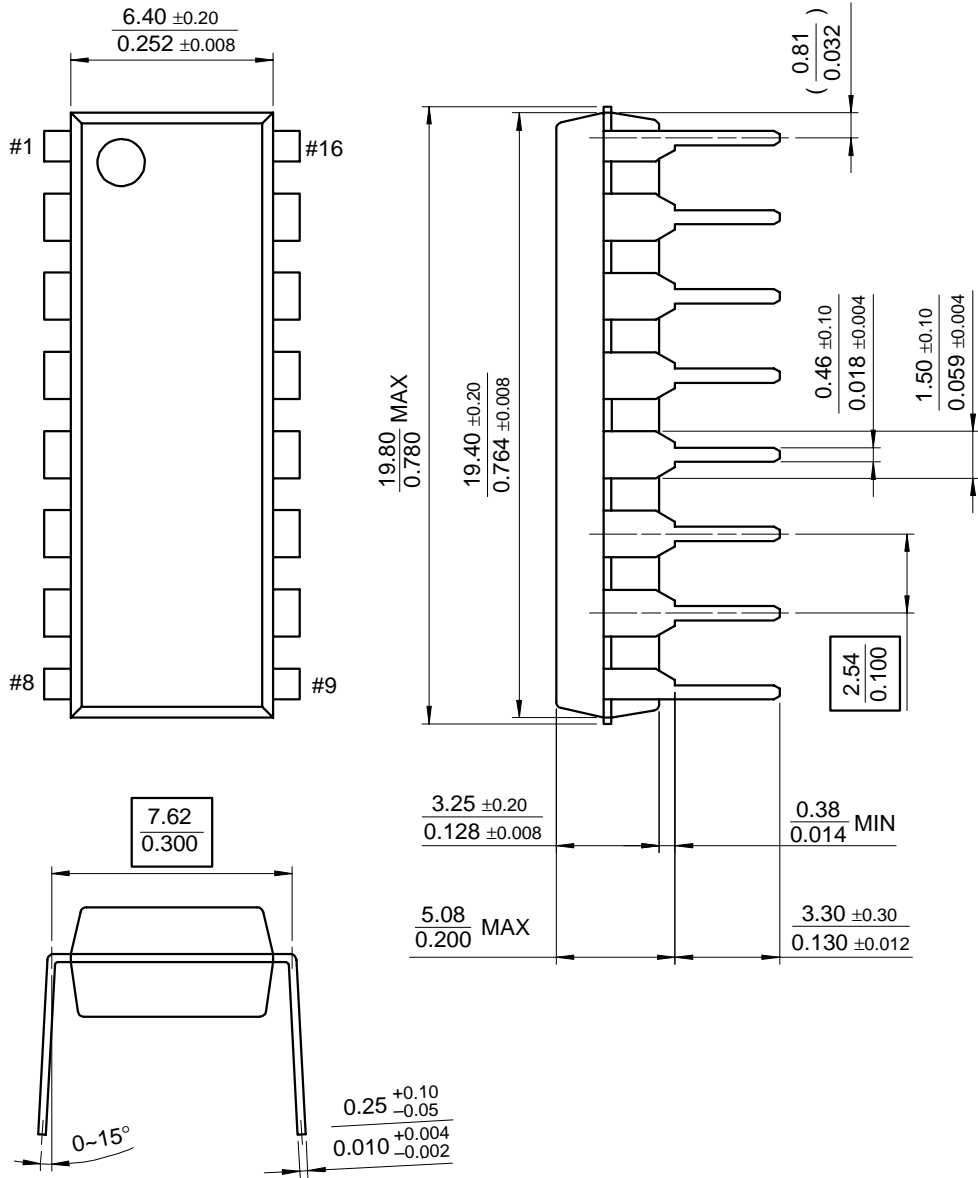
Figure 20. PG Delay Time

Mechanical Dimensions

Package

Dimensions in millimeters

16-DIP



Ordering Information

Product Number	Package	Operating Temperature
FAN3506	16-DIP	-25°C ~ +85°C

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.