FAIRCHILD SEMICONDUCTOR®

April 2010

FAN4860
3MHz, 5V Output Synchronous TinyBoost™ Regulator

Features

- Operates with Very Small External Components: 1µH Inductor and 0402 Case Size Input and Output Capacitors
- Input Voltage Range from 2.3V to 4.5V
- Fixed 5.0V Output Voltage
- Maximum Load Current 200mA at V_{IN}=2.3V
- Maximum Load Current 300mA at V_{IN}=3.3V
- Up to 92% Efficient
- Low Operating Quiescent Current
- True Load Disconnect During Shutdown
- Variable On-time Pulse Frequency Modulation (PFM) with Light-Load Power-Saving Mode
- Internal Synchronous Rectifier (No External Diode Needed)
- Thermal Shutdown and Overload Protection
- 6-Pin 2 x 2mm UMLP
- 6-Bump WLCSP, 0.4mm Pitch

Applications

- USB "On the Go" 5V Supply
- HDMI 5V Supply
- 5V Supply for H-Bridge Motor Drivers
- Powering 5V Peripherals
- Supply Source for WLED Torch and Flash Lighting
- PDAs, Portable Media Players
- Cell Phones, Smart Phones, Portable Instruments

Description

The FAN4860 is a low-power boost regulator designed to provide a regulated 5V output from a single cell Li-Ion battery. The output voltage is fixed at 5.0V with a guaranteed maximum load current of 200mA at V_{IN}=2.3V and 300mA at V_{IN}=3.3V. Input current in shut-down mode is less than 1µA, which maximizes battery life.

Light-load PFM operation is automatic and "glitch-free". The regulator maintains output regulation at no-load with 37µA quiescent current.

The combination of built-in power transistors, synchronous rectification, and low supply current make the FAN4860 ideal for battery powered applications.

The FAN4860 is available in 6-bump 0.4mm pitch Wafer-Level Chip Scale Package (WLCSP) and a 6-lead 2x2mm ultra-thin MLP package.

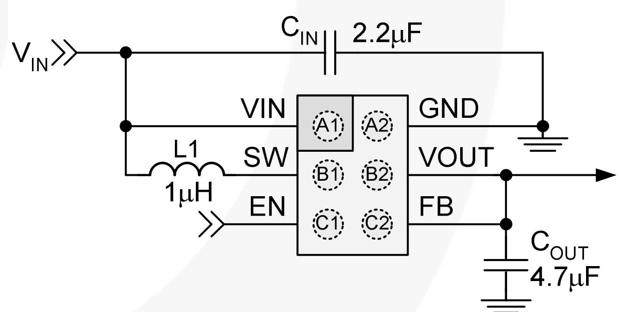


Figure 1. Typical Application

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN4860UC5X	-40°C to 85°C	WLCSP, 0.4mm Pitch	Tape and Reel
FAN4860UMP5X	-40°C to 85°C	UMLP-6, 2 x 2mm	Tape and Reel

Please refer to tape and reel specifications at http://www.fairchildsemi.com/packaging.

Block Diagrams

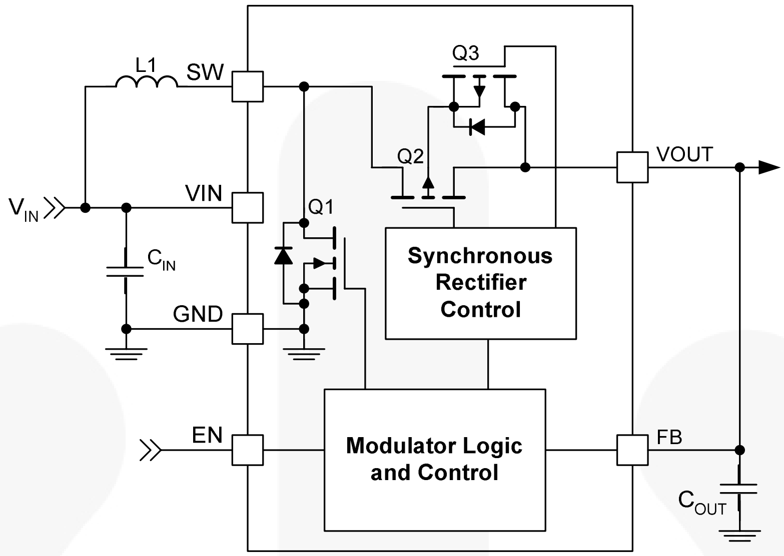


Figure 2. IC Block Diagram

Pin Configuration

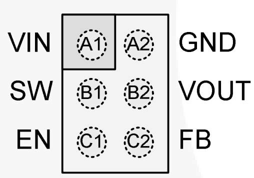


Figure 3. WLCSP (Top View)

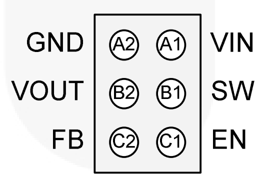


Figure 4. WLCSP (Bottom View)

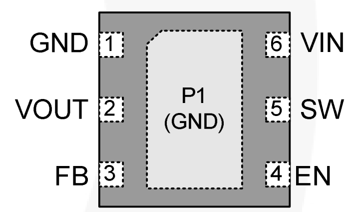


Figure 5. 2X2mm UMLP (Top View)

Pin Definitions

Pin #		Name	Description
WLCSP	UMLP		
A1	6	VIN	**Input Voltage**. Connect to Li-Ion battery input power source and input capacitor (C_{IN}).
B1	5	SW	**Switching Node**. Connect to inductor.
C1	4	EN	**Enable**. When this pin is HIGH, the circuit is enabled. This pin should not be left floating.
C2	3	FB	**Feedback**. Output voltage sense point for V_{OUT}. Connect to output capacitor (C_{OUT}).
B2	2	VOUT	**Output Voltage**. This pin is both the output voltage terminal as well as an IC bias supply.
A2	1, P1	GND	**Ground**. Power and signal ground reference for the IC. All voltages are measured with respect to this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{IN}	VIN Pin		-0.3	5.5	V
V_{OUT}	VOUT Pin		–2	6	V
V_{FB}	FB Pin		–2	14	V
V_{SW}	SW Node	DC	-0.3	5.5	V
		Transient: 10ns, 3MHz	-1.0	6.5	
V_{EN}	EN Pin		-0.3	5.5	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2.0		kV
		Charged Device Model per JESD22-C101	1.0		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{IN}	Supply Voltage	2.3	4.5	V
I_{OUT}	Output Current		200	mA
T_A	Ambient Temperature	–40	+85	°C
T_J	Junction Temperature	–40	+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Symbol	Parameter		Typical	Units
θ_{JA}	Junction-to-Ambient Thermal Resistance	WLCSP	130	°C/W
		UMLP	57	°C/W

Electrical Specifications

Minimum and maximum values are at V_{IN}=V_{EN}=2.3V to 4.5V, T_A=-40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A=25°C, V_{IN}=V_{EN}=3.6V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IN}	V_{IN} Input Current	Quiescent: V_{IN}=3.6V, I_{OUT}=0, EN=V_{IN}		37	45	μA
		Shutdown: EN=0, V_{IN}=3.6V		0.5	1.5	
I_{LK_OUT}	V_{OUT} Leakage Current	V_{OUT}=0, EN=0, V_{IN}=4.2V		10		nA
I_{LK_RVSR}	V_{OUT} to V_{IN} Reverse Leakage	V_{OUT}=5V, V_{IN}=3.6V, EN=0			2.5	μA
V_{UVLO}	Under-Voltage Lockout	V_{IN} Rising		2.2	2.3	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			190		mV
V_{ENH}	Enable HIGH Voltage		1.05			V
V_{ENL}	Enable LOW Voltage				0.4	V
I_{LK_EN}	Enable Input Leakage Current			0.01	1	μA
V_{OUT}	V_{OUT} Output Voltage Accuracy(1)	V_{IN} from 2.3V to 4.5V, I_{OUT}≤200mA	4.80	5.05	5.15	V
		V_{IN} from 2.7V to 4.5V, I_{OUT}≤200mA	4.85	5.05	5.15	
		V_{IN} from 3.3V to 4.5V, I_{OUT}≤300mA	4.85	5.05	5.15	
V_{REF}	Reference Accuracy	Referred to V_{OUT}	4.975	5.050	5.125	V
t_{OFF}	Off Time	V_{IN}=3.6V, I_{OUT}=200mA	195	240	265	ns
I_{OUT}	Maximum Output Current(2)	V_{IN}=2.3V, V_{OUT}=5V	200			mA
		V_{IN}=3.3V, V_{OUT}=5V	300			
		V_{IN}=3.6V, V_{OUT}=5V		400		
I_{SW}	SW Peak Current Limit	V_{IN}=3.6V, V_{OUT}>V_{IN}	930	1100	1320	mA
I_{SS}	Soft-Start Input Peak Current Limit(2)	V_{IN}=3.6V, V_{OUT} < V_{IN}		850		mA
t_{SS}	Soft-Start Time	V_{IN}=3.6V, I_{OUT}=200mA Time=Rising EN until Regulated V_{OUT}		100	300	μs
$R_{DS(ON)}$	N-Channel Boost Switch	V_{IN}=3.6V		300		mΩ
	P-Channel Sync Rectifier	V_{IN}=3.6V		400		
T_{TSD}	Thermal Shutdown	I_{LOAD}=10mA		150		°C
T_{TSD_HYS}	Thermal Shutdown Hysteresis			30		°C

Notes:

1. I_{LOAD} from 0 to I_{OUT}; also includes load transient response. V_{OUT} measured from mid-point of output voltage ripple. Effective capacitance of C_{OUT} > 1.5μF.
2. Guaranteed by design and characterization; not tested in production.

Typical Characteristics

Unless otherwise specified, circuit per Figure 1, 3.6V_{IN}, T_A=25°C.

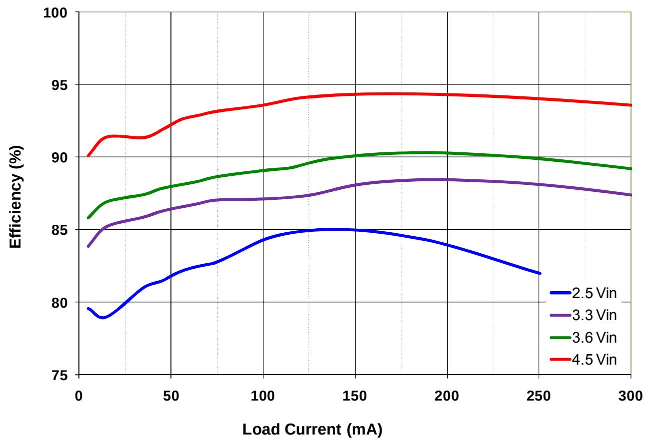


Figure 6 Efficiency vs. V_{IN}

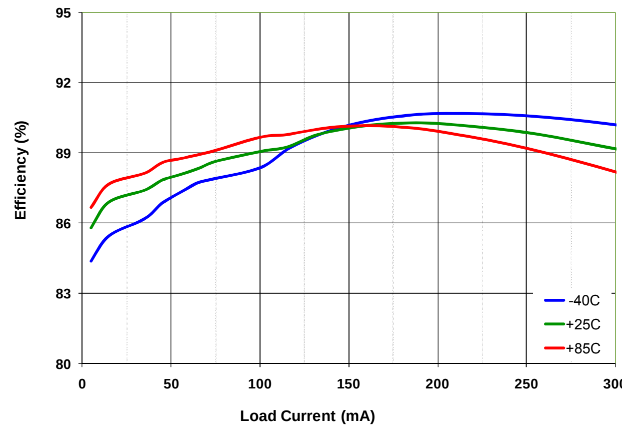


Figure 7 Efficiency vs. Temperature, 3.6V_{IN}

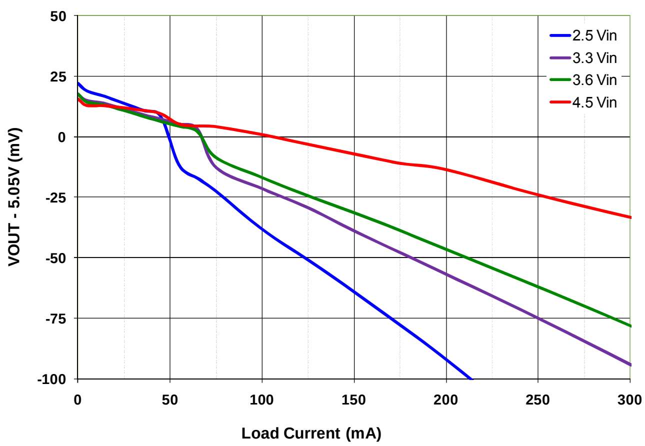


Figure 8 Line and Load Regulation

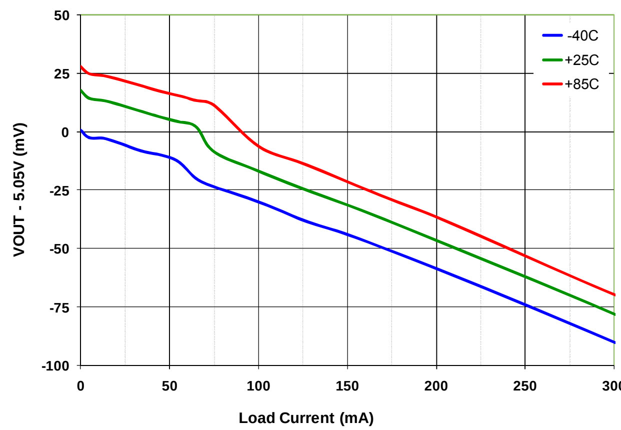


Figure 9 Load Regulation vs. Temperature, 3.6V_{IN}

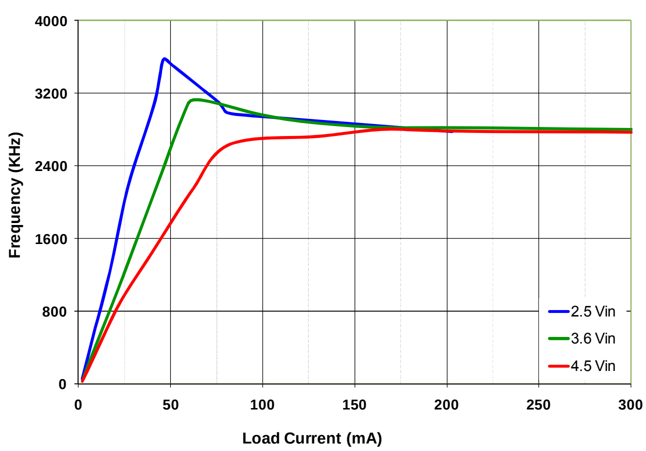


Figure 10 Switching Frequency

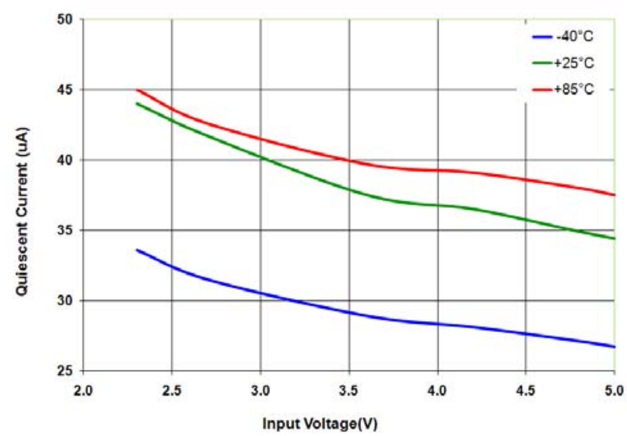


Figure 11 Quiescent Current

Typical Characteristics

Unless otherwise specified, circuit per Figure 1, $3.6V_{IN}$, T_A=25°C.

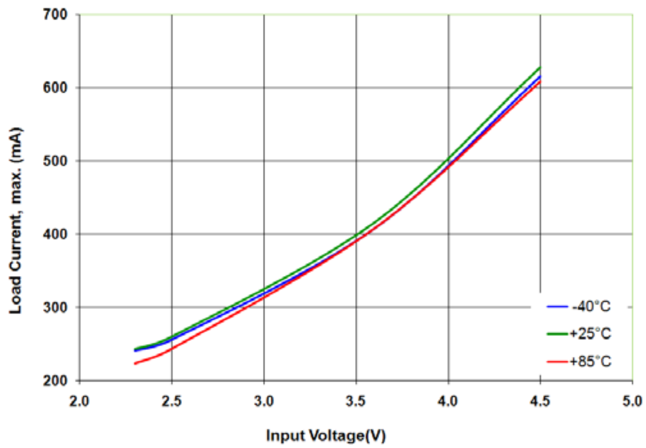


Figure 12 Maximum DC Load Current

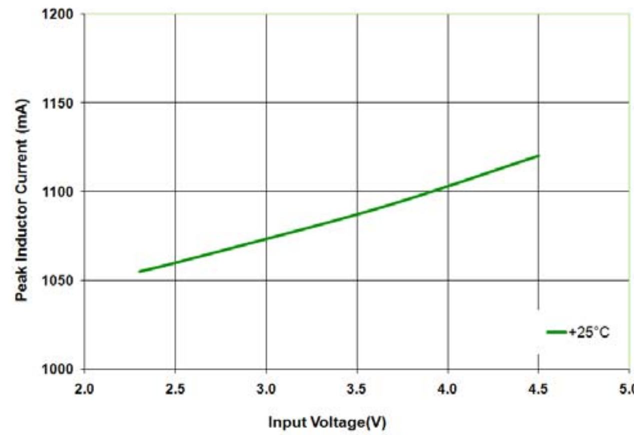


Figure 13 Peak Inductor Current

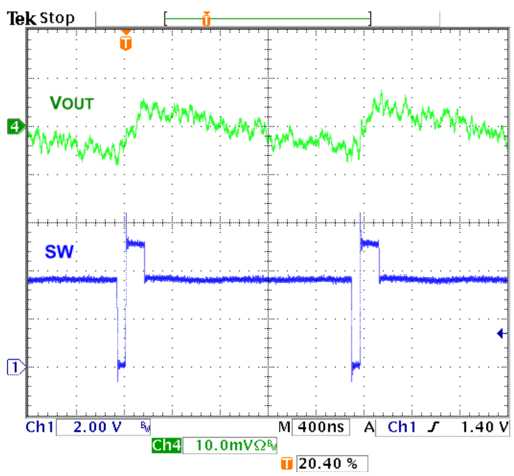


Figure 14 Output Ripple, 10mA PFM Load

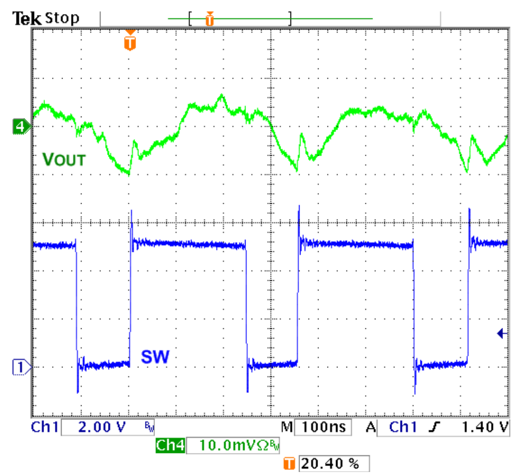


Figure 15 Output Ripple, 200mA PWM Load

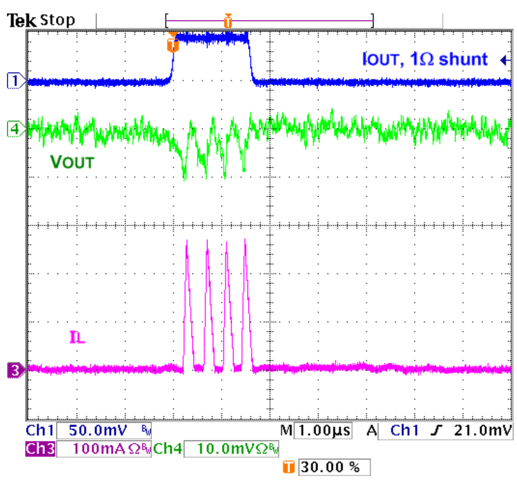


Figure 16 0-50mA Load Transient, 100ns Step

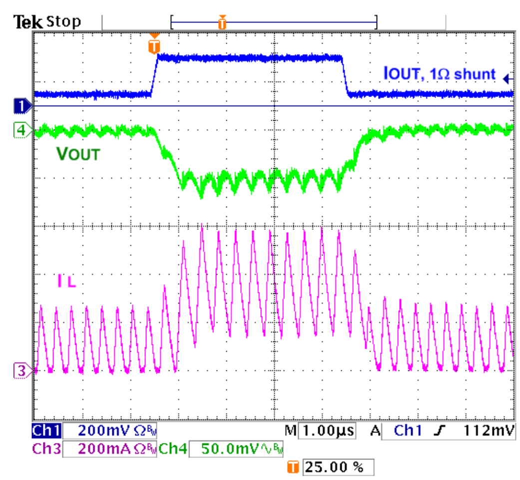


Figure 17 50-200mA Load Transient, 100ns Step

Typical Characteristics

Unless otherwise specified, circuit per Figure 1, 3.6V_{IN}, T_A=25°C.

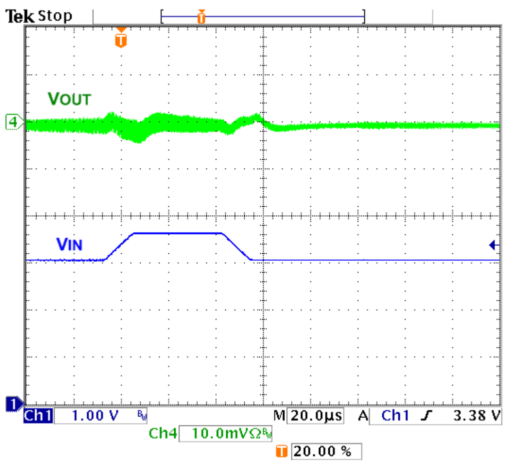


Figure 18 Line Transient, 5mA Load, 10µs Step

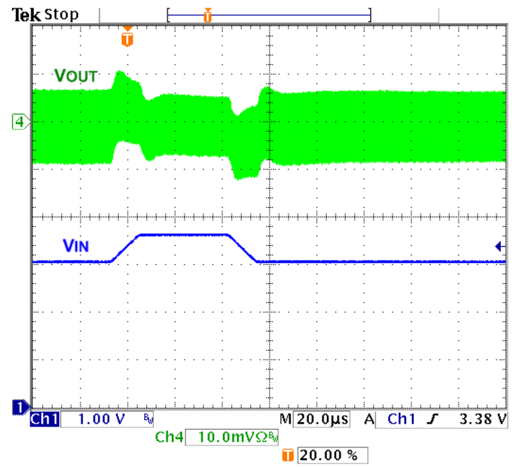


Figure 19 Line Transient, 200mA Load, 10µs Step

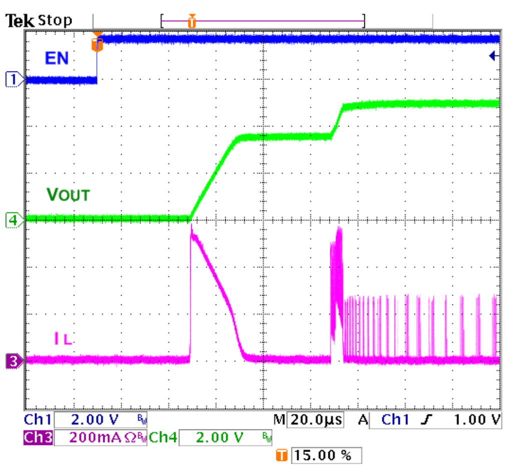


Figure 20 Startup, No Load

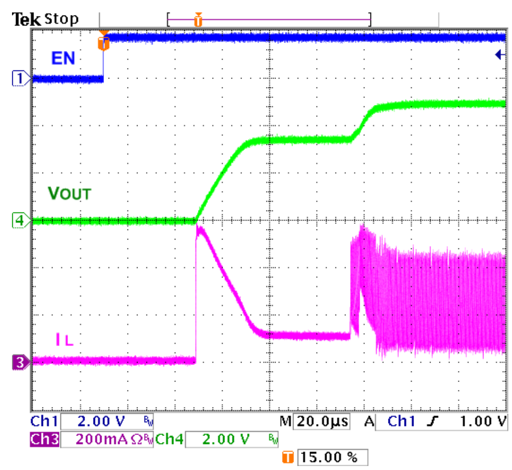


Figure 21 Startup, 33Ω Load

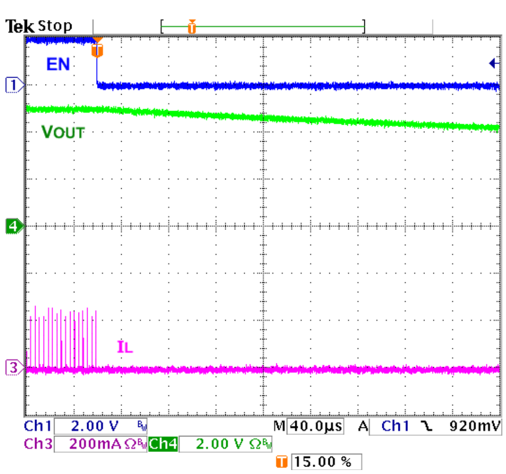


Figure 22 Shutdown, 1KΩ Load

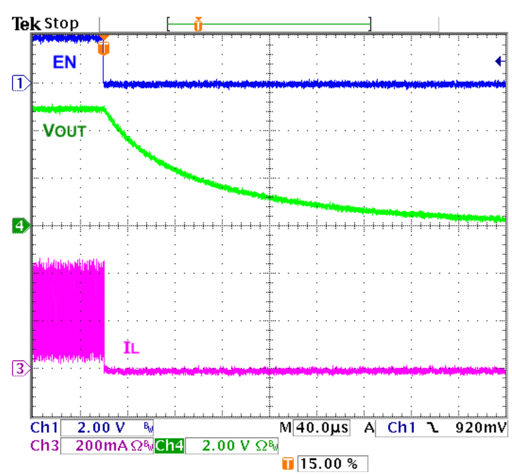


Figure 23 Shutdown, 33Ω Load

Typical Characteristics

Unless otherwise specified, circuit per Figure 1, 3.6V_{IN}, T_A=25°C.

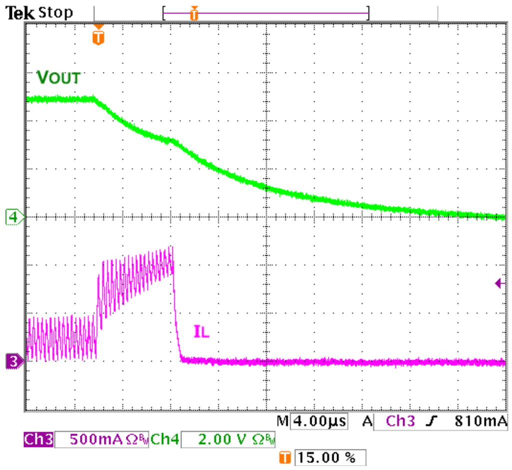


Figure 24 Overload Protection

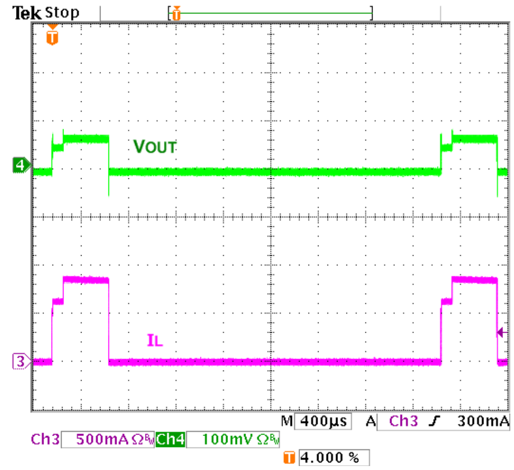


Figure 25 Short-Circuit Response

Functional Description

Circuit Description

FAN4860 is a synchronous boost regulator, typically operating at 3MHz in continuous conduction mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltages.

At light-load currents, the converter switches automatically to power-saving PFM mode. The regulator automatically and smoothly transitions between quasi-fixed-frequency continuous conduction PWM mode and variable-frequency PFM mode to maintain the highest possible efficiency over the full range of load current and input voltage.

PWM Mode Regulation

The FAN4860 uses a minimum on-time and computed minimum off-time to regulate V_{OUT}. The regulator achieves excellent transient response by employing current mode modulation. This technique causes the regulator output to exhibit a load line. During PWM mode, the output voltage drops slightly as the input current rises. With a constant V_{IN}, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with negligible overshoot.

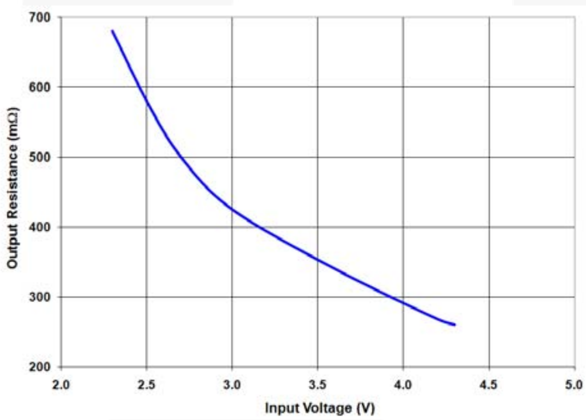


Figure 26 Output Resistance (R_{OUT})

V_{OUT} as a function of I_{LOAD} can be computed when the regulator is in PWM mode (continuous conduction) as:

$$V_{OUT} = 5.05 - R_{OUT} \bullet I_{LOAD} \quad \text{EQ. 1}$$

For example, at V_{IN}=3.3V, and I_{LOAD}=200mA, V_{OUT} would drop to:

$$V_{OUT} = 5.05 - 0.38 \bullet 0.2 = 4.974V \quad \text{EQ. 1A}$$

At V_{IN}=2.3V, and I_{LOAD}=200mA, V_{OUT} would drop to:

$$V_{OUT} = 5.05 - 0.68 \bullet 0.2 = 4.914V \quad \text{EQ. 1B}$$

PFM Mode

If $V_{OUT} > V_{REF}$ when the minimum off-time has ended, the regulator enters PFM mode. Boost pulses are inhibited until $V_{OUT} < V_{REF}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.05V in PFM mode.

Table 1. Operating States

Mode	Description	Invoked When:
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{OUT} < V_{REG}$
BST	Boost Operating Mode	$V_{OUT}=V_{REG}$

Shutdown and Startup

If EN is LOW, all bias circuits are off and the regulator is in shutdown mode. During shutdown, true load disconnect between battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

LIN State

When EN rises, if V_{IN} > UVLO, the regulator first attempts to bring V_{OUT} within about 1V of V_{IN} by using the internal fixed current source from V_{IN} (I_{LIN1}). The current is limited to about 630mA during LIN1 mode.

If V_{OUT} reaches V_{IN}-1V during LIN1 mode, the SS state is initiated. Otherwise, LIN1 times out after 16 CLK counts and the LIN2 mode is entered.

In LIN2 mode, the current source is incremented to 850mA. If V_{OUT} fails to reach V_{IN}-1V after 64 CLK counts, a fault condition is declared.

SS State

Upon the successful completion of the LIN state ($V_{OUT} \geq V_{IN}$-1V), the regulator begins switching with boost pulses current limited to about 50% of nominal level, incrementing to full scale over a period of 32 CLK counts.

If the output fails to achieve 90% of its setpoint within 96 CLK counts at full-scale current limit, a fault condition is declared.

BST State

This is the normal operating mode of the regulator. The regulator uses a minimum t_{OFF}-minimum t_{ON} modulation scheme. Minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$, which keeps the regulator's switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to V_{IN} and is higher if the inductor current reaches 0 before $t_{OFF(MIN)}$ during the prior cycle.

To ensure that V_{OUT} does not pump significantly above the regulation point, the boost switch remains off as long as FB > V_{REF}.

Fault State

The regulator enters the FAULT state under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN state to SS state.
- V_{OUT} fails to achieve the voltage required to advance from SS state to BST state.
- Sustained (32 CLK counts) pulse-by-pulse current limit during the BST state.
- The regulator moves from BST to LIN state due to a short circuit or output overload (V_{OUT} < V_{IN}-1V).

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between V_{IN} and V_{OUT}. After waiting 480 CLK counts, a re-start is attempted.

Soft-Start and Fault Timing

The soft-start timing for each state, and the fault times, are determined by the fault clock, whose period is inversely proportional to V_{IN}. This allows the regulator more time to charge larger values of C_{OUT} when V_{IN} is lower. With higher V_{IN}, this also reduces power delivered to V_{OUT} during each cycle in current limit.

The number of clock counts for each state is illustrated in Figure 27.

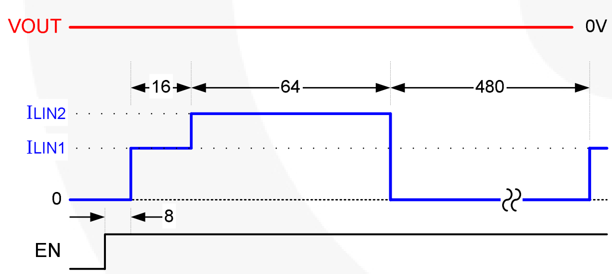


Figure 27. Fault Response into Short Circuit

The fault clock period as a function of V_{IN} is shown in Figure 28.

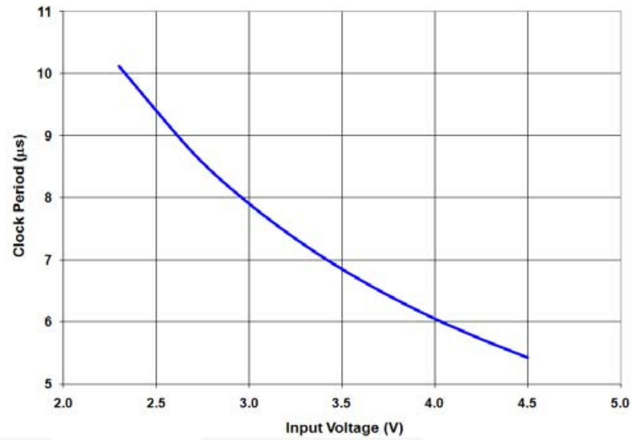


Figure 28. Fault Clock Period vs. V_{IN}

The V_{IN}-dependent LIN mode charging current is illustrated in Figure 29.

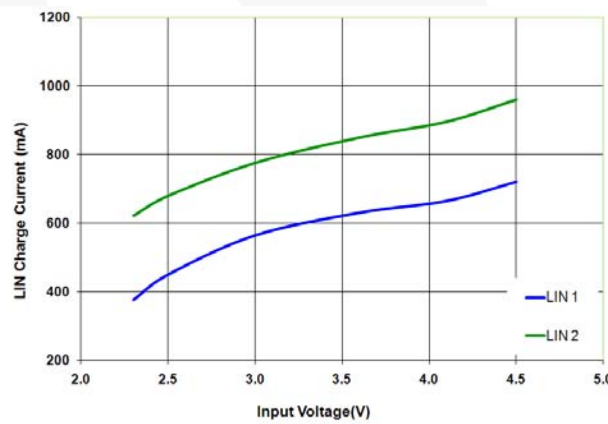


Figure 29. LIN Mode Current vs. V_{IN}

Over-Temperature Protection (OTP)

The regulator shuts down when the thermal shutdown threshold is reached. Restart, with soft-start, occurs when the IC has cooled by about 30°C.

Over-Current Protection (OCP)

During boost-mode operation, the FAN4860 employs a cycle-by-cycle peak current limit to protect switching elements. Sustained current limit, for 32 consecutive fault CLK counts, initiates a fault condition.

During an overload condition, as V_{OUT} collapses to approximately V_{IN}-1V, the synchronous rectifier is immediately switched off and a fault condition is declared.

Automatic restart occurs once the overload/short is removed and the fault timer completes counting.

Application Information

External Component Selection

Table 2 shows the recommended external components for the FAN4860:

Table 2. External Components

REF	Description	Manufacturer
L1	1.0µH, 0.8A, 190mΩ, 0805	Murata LQM21PN1R0MC0, or equivalent
C_{IN}	2.2µF, 6.3V, X5R, 0402	Murata GRM155R60J225M
		TDK C1005X5R0J225M
C_{OUT}	4.7µF, 10V, X5R, 0603(3)	Kemet C0603C475K8PAC
		TDK C1608X5R1A475K

Note:

3. A 6.3V-rated 0603 capacitor may be used for C_{OUT}, such as Murata GRM188R60J225M. All datasheet parameters are valid with the 6.3V-rated capacitor. Due to DC bias effects, the 10V capacitor offers a performance enhancement; particularly output ripple and transient response, without any size increase.

Output Capacitance (C_{OUT})

Stability

The effective capacitance (C_{EFF}) of small, high-value, ceramic capacitors decrease as their bias voltage increases, as shown in Figure 30.

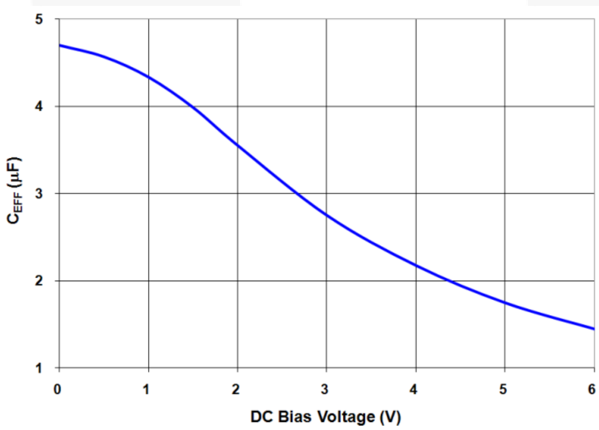


Figure 30. C_{EFF} for 4.7µF, 0603, X5R, 6.3V (Murata GRM188R60J475K)

FAN4860 is guaranteed for stable operation with the minimum value of C_{EFF} ($C_{EFF(MIN)}$) outlined in Table 3.

Table 3. Minimum C_{EFF} Required for Stability

Operating Conditions		$C_{EFF(MIN)}$ (µF)
V_{IN} (V)	I_{LOAD} (mA)	
2.3 to 4.5	0 to 200	1.5
2.7 to 4.5	0 to 200	1.0
2.3 to 4.5	0 to 150	1.0

C_{EFF} varies with manufacturer, dielectric material, case size, and temperature. Some manufacturers may be able to provide an X5R capacitor in 0402 case size that retains C_{EFF} >1.5µF with 5V bias; others may not. If this C_{EFF} cannot be economically obtained and 0402 case size is required, the IC can work with the 0402 capacitor as long as the minimum V_{IN} is restricted to >2.7V.

For best performance, a 10V-rated 0603 output capacitor is recommended (Kemet C0603C475K8PAC, or equivalent). Since it retains greater C_{EFF} under bias and over temperature, ouptut ripple can is reduced and transient capability enhanced.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}.

$$V_{RIPPLE(P-P)} = t_{ON} \bullet \frac{I_{LOAD}}{C_{OUT}} \quad \text{EQ. 2}$$

and

$$t_{ON} = t_{SW} \bullet D = t_{SW} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{EQ. 3}$$

Therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet \frac{I_{LOAD}}{C_{OUT}} \quad \text{EQ. 4}$$

where:

$$t_{SW} = 1/f_{SW} \quad \text{EQ. 5}$$

As can be seen from EQ. 4, the maximum V_{RIPPLE} occurs when V_{IN} is minimum and I_{LOAD} is maximum.

Startup

Input current limiting is in effect during soft-start, which limits the current available to charge C_{OUT}. If the output fails to achieve regulation within the time period described in the soft-start section above; a FAULT occurs, causing the circuit to shut down, then restart after a significant time period. If C_{OUT} is a very high value, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high-current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempt soft-start, only to have C_{OUT} discharged by the load when in the FAULT state.

The circuit can start with higher values of C_{OUT} under full load if V_{IN} is higher, since:

$$I_{OUT} = \left(I_{LIM(PK)} - \frac{I_{RIPPLE}}{2} \right) \bullet \frac{V_{IN}}{V_{OUT}} \qquad \text{EQ. 6}$$

Generally, the limitation occurs in BST mode.

The FAN4860 starts on the first pass (without triggering a FAULT) under the following conditions for $C_{EFF(MAX)}$:

Table 4. Maximum C_{EFF} for First-Pass Startup

Operating Conditions		$C_{EFF(MAX)}$ (µF)
V_{IN} (V)	$R_{LOAD(MIN)}$	
2.3 to 4.5	25Ω	10
2.7 to 4.5	25Ω	15
2.7 to 4.5	33Ω	22

C_{EFF} values shown in Table 4 typically apply to the lowest V_{IN}. The presence of higher V_{IN} enhances ability to start into larger C_{EFF} at full load.

Transient Protection

To protect against external voltage transients caused by ESD discharge events, or improper external connections, some applications employ an external transient voltage suppressor (TVS) and Schottky diode (D1 in Figure 31).

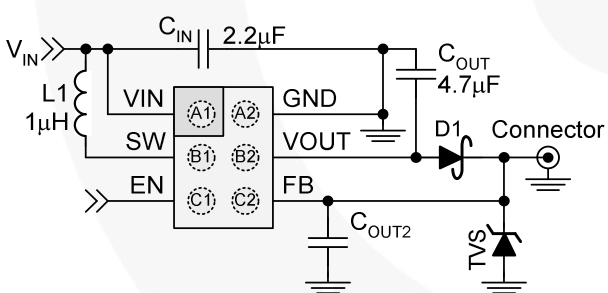


Figure 31 FAN4860 with External Transient Protection

The TVS is designed to clamp the FB line (system V_{OUT}) to +10V or –2V during external transient events. The Schottky diode protects the output devices from the positive excursion. The FB pin can tolerate up to 14V of positive excursion, while both the FB and VOUT pins can tolerate negative voltages.

The FAN4860 includes a circuit to detect a missing or defective D1 by comparing V_{OUT} to FB. If V_{OUT} – FB > about 0.7V, the IC shuts down. The IC remains shut down until V_{OUT} < UVLO and V_{IN} < UVLO+0.7 or EN is toggled.

C_{OUT2} may be necessary to preserve load transient response when the Schottky is used. When a load is applied at the FB pin, the forward voltage of the D1 rapidly increases before the regulator can respond or the inductor current can change. This causes an immediate drop of up to 300mV, depending on D1's characteristics if C_{OUT2} is absent. C_{OUT2} supplies instantaneous current to the load while the regulator adjusts the inductor current. A value of at least half of the minimum value of C_{OUT} should be used for C_{OUT2}. C_{OUT2} needs to withstand the maximum voltage at the FB pin as the TVS is clamping.

The maximum DC output current available is reduced with this circuit, due to the additional dissipation of D1.

Layout Guideline

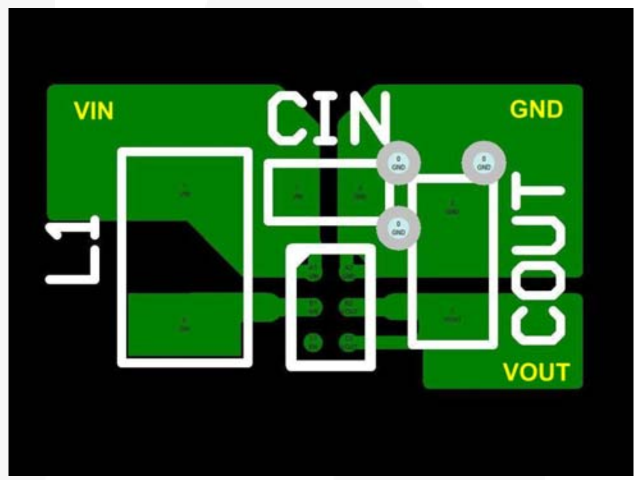


Figure 32 WLCSP Suggested Layout (Top View)

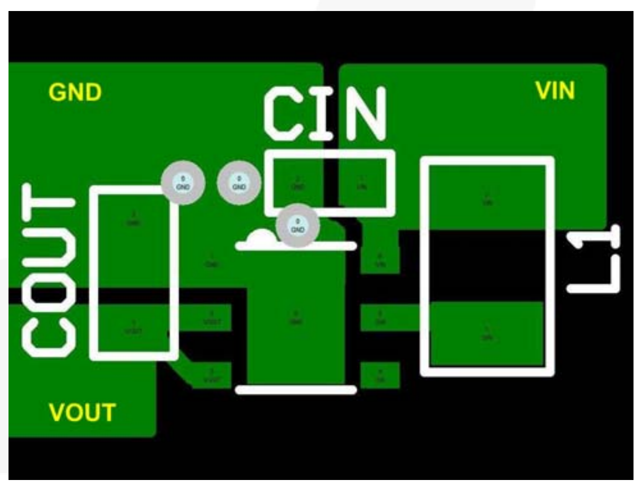
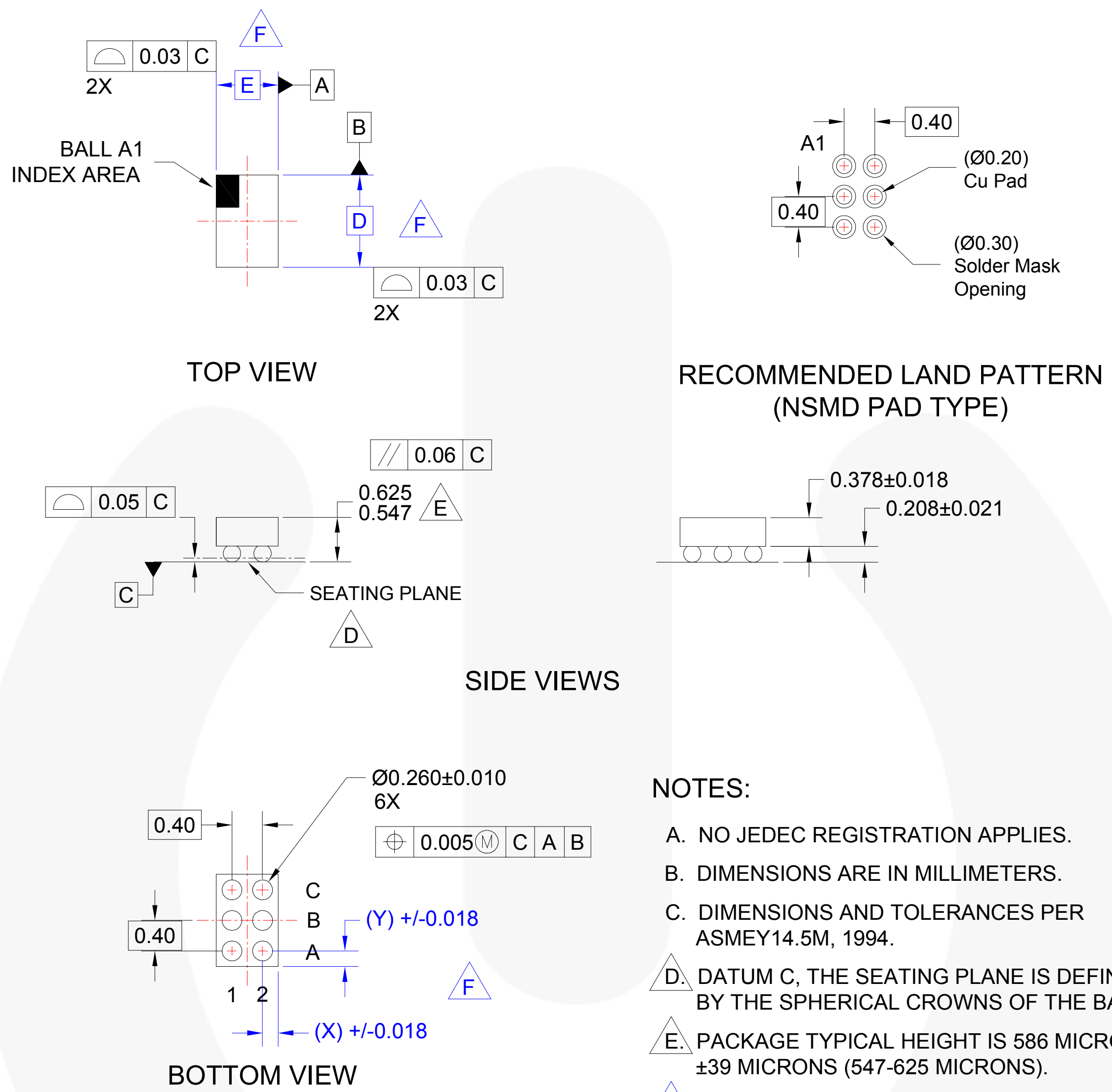


Figure 33 UMLP Suggested Layout (Top View)

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 1994.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006ACrev4.

Figure 33. 6-Lead, 0.4mm Pitch, WLCSP Package

Product-Specific Dimensions

Product	D	E	X	Y
FAN4860UC5X	1.230mm +/-0.030mm	0.880mm +/-0.030mm	0.240mm	0.215mm

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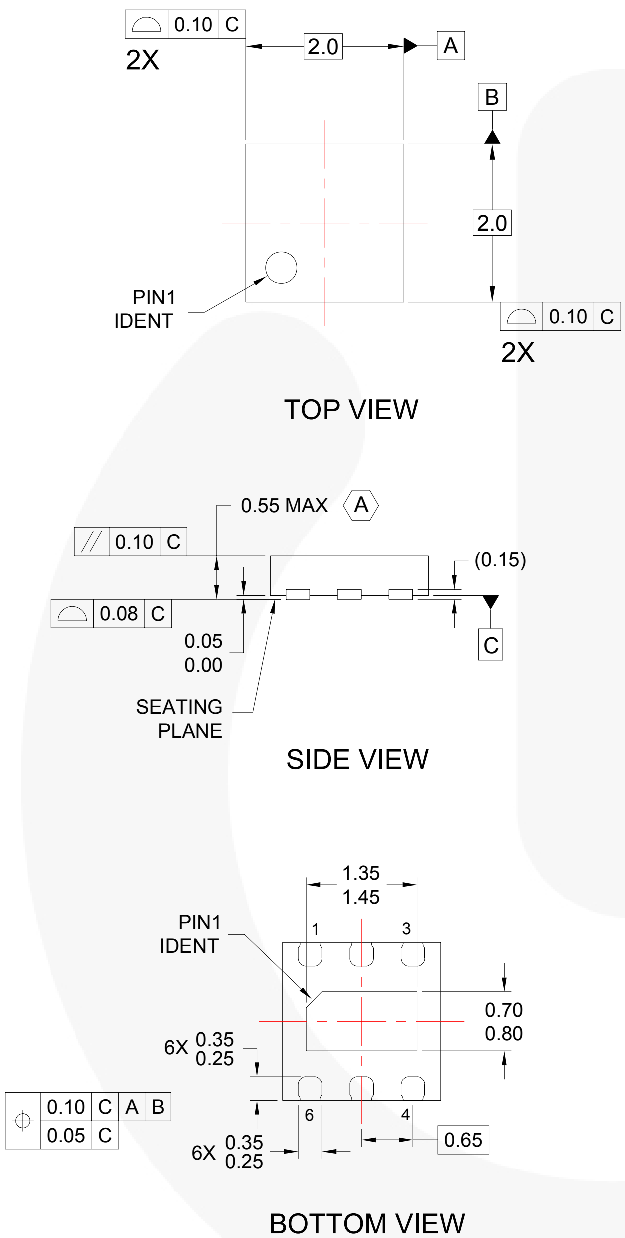
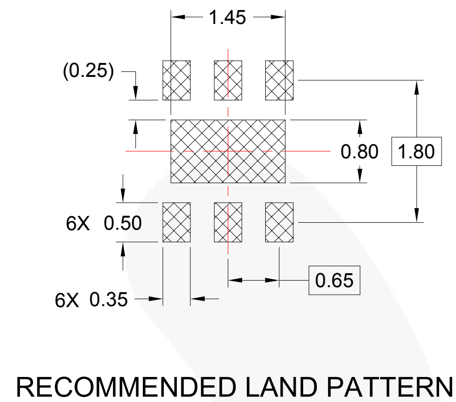
Physical Dimensions





NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.

E. DRAWING FILENAME: MKT-UMLP06Erev2.

Figure 34. 6-Lead UMLP Package

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