

4-BIT SINGLE CHIP MICROCOMPUTERS

GMS34XXXT SERIES

USER`S MANUAL

- GMS34004T
- GMS34112T
- GMS34140T

Revision 1.1

**Published by MCU Application Team in HYNIX Semiconductor Inc.
All Right Reserved.**

Editor's E-Mail : rhja@hynix.com

Additional information of this manual may be served by HYNIX Semiconductor Inc. Offices in Korea or Distributors and Representative listed at address directory.

HYNIX Semiconductor Inc. reserves the right to make changes to any Information here at any time without notice.

The information, diagrams, and other data in this manual are correct and reliable; however, HYNIX Semiconductor Inc. is in no way responsible for any violations of patents or other rights of the third party generated by the use of this manual.

Table of Contents

Chapter 1

| | |
|-------------------------------------|------|
| Introduction | 1-1 |
| Outline of Characteristics | 1-1 |
| Characteristics | 1-1 |
| Block Diagram | 1-2 |
| Pin Assignment and Terminal | 1-3 |
| Pin Dimension | 1-4 |
| Pin Description and Circuit | 1-7 |
| I/O circuit types and options | 1-8 |
| Electrical Characteristics | 1-10 |

Chapter 2

| | |
|---------------------------------------|-----|
| Architecture | 2-1 |
| Block Description | 2-1 |
| Program Memory (ROM) | 2-1 |
| EPROM Address Register | 2-2 |
| Data Memory (RAM) | 2-3 |
| X-Register (X) | 2-3 |
| Y-Register (Y) | 2-4 |
| Accumulator (Acc) | 2-4 |
| Arithmetic and Logic Unit (ALU) | 2-4 |
| State Counter (SC) | 2-5 |
| Clock Generator | 2-6 |
| Pulse Generator | 2-7 |
| Initial Reset Circuit | 2-8 |
| Watch Dog Timer (WDT) | 2-8 |
| Stop Function | 2-9 |
| Port Operation | 2-9 |

Chapter 3

| | |
|-------------------|-----|
| Instruction | 3-1 |
|-------------------|-----|

Table of Contents

Chapter 4

| | |
|--|------|
| EPROM | 4-1 |
| GMS34004TK/34112TK/34140TK | 4-1 |
| Mode Define | 4-1 |
| Port Define | 4-2 |
| Programming Data | 4-2 |
| Write/Read Data Conversion | 4-3 |
| Checksum | 4-3 |
| Programming Control | 4-3 |
| Programming DC Specification | 4-3 |
| EPROM read mode(1/2) | 4-4 |
| EPROM read mode (2/2) | 4-4 |
| EPROM write mode (1/2) | 4-5 |
| EPROM write mode (2/2) | 4-5 |
| Lock bit write mode (1/2) | 4-6 |
| Lock bit write mode (2/2) | 4-6 |
| Lock bit read mode (1/2) | 4-7 |
| Lock bit read mode (2/2) | 4-7 |
| GMS34004T/112T/140T (Pin assignment & Package) | 4-8 |
| EPROM (KHz) mode | 4-9 |
| EPROM write only mode | 4-9 |
| GMS34004TK/34112TK/34140TK | 4-10 |
| Mode Define | 4-10 |
| Port Define | 4-11 |
| Programming Data | 4-11 |
| Write/Read Data Conversion | 4-12 |
| Checksum | 4-12 |
| Programming Control | 4-12 |
| Programming DC Specification | 4-12 |
| EPROM read mode(1/2) | 4-13 |
| EPROM read mode (2/2) | 4-13 |
| EPROM write mode (1/4) | 4-14 |
| EPROM write mode (2/4) | 4-14 |
| EPROM write mode (3/4) | 4-15 |
| EPROM write mode (4/4) | 4-15 |
| Lock bit write mode (1/3) | 4-16 |
| Lock bit write mode (2/3) | 4-16 |
| Lock bit write mode (3/3) | 4-16 |
| Lock bit read mode (1/2) | 4-18 |
| Lock bit read mode (2/2) | 4-18 |

| | | |
|---------------------|----------|--|
| INTRODUCTION | 1 | |
| ARCHITECTURE | 2 | |
| INSTRUCTION | 3 | |
| EPROM | 4 | |

CHAPTER 1. Introduction

OUTLINE OF CHARACTERISTICS

The GMS340 series are remote control transmitter which uses CMOS technology, and the EPROM version of GMS34XXX series. This enables transmission code outputs of different configurations, multiple custom code output, and double push key output for easy fabrication. The GMS340 series are suitable for remote control of TV, VCR, FANS, Air-conditioners, Audio Equipments, Toys, Games etc.

Characteristics

- Program memory : 512bytes for GMS34004T
1,024 bytes for GMS34112T/140T
- Data memory : 32 i 4 bits
- 43 types of instruction set
- 3 levels of subroutine nesting
- 1 bit output port for a large current (REMOUT signal)
- Operating frequency : 300KHz~500KHz at KHz version
2.4MHz~4MHz at MHz version
300KHz~4.2MHz at WIDE version
- Instruction cycle : $f_{OSC}/6$ at KHz and WIDE version
 $f_{OSC}/48$ at MHz version
- CMOS process (3.0V or 5.0V power supply)
- Stop mode (Through internal instruction)
- Released stop mode by key input
- Built in capacitor for ceramic oscillation circuit at KHz version
- Built in a watch dog timer (WDT)
- Low operating voltage : 2.2~4.5V (at KHz and MHz version)
Normal operating voltage: 4.0~5.0V (at WIDE version)

| Series | GMS34004T | GMS34112T | GMS34140T |
|----------------|--------------|----------------|---------------|
| Program memory | 512 | 1,024 | i 4 |
| Data memory | 32 i 4 | i 4 | i 4 |
| I/O ports | - | 4 | i 4 |
| Input ports | 4 | i 4 | i 4 |
| Output ports | 6 D0 ~ D5 | i 4 i 4 | 10 D0 ~ D9 |
| Package | 16DIP | 20DIP/SOP/SSOP | 24DIP/SOP |
| KHz version | GMS34004TK | GMS34112TK | GMS34140TK |
| MHz version | GMS34004TM | GMS34112TM | GMS34140TM |
| WIDE version | GMS34004TW | GMS34112TW | GMS34140TW |

Table 1-1 GMS34XXXT series members

Chapter 1. Introduction

Block Diagram

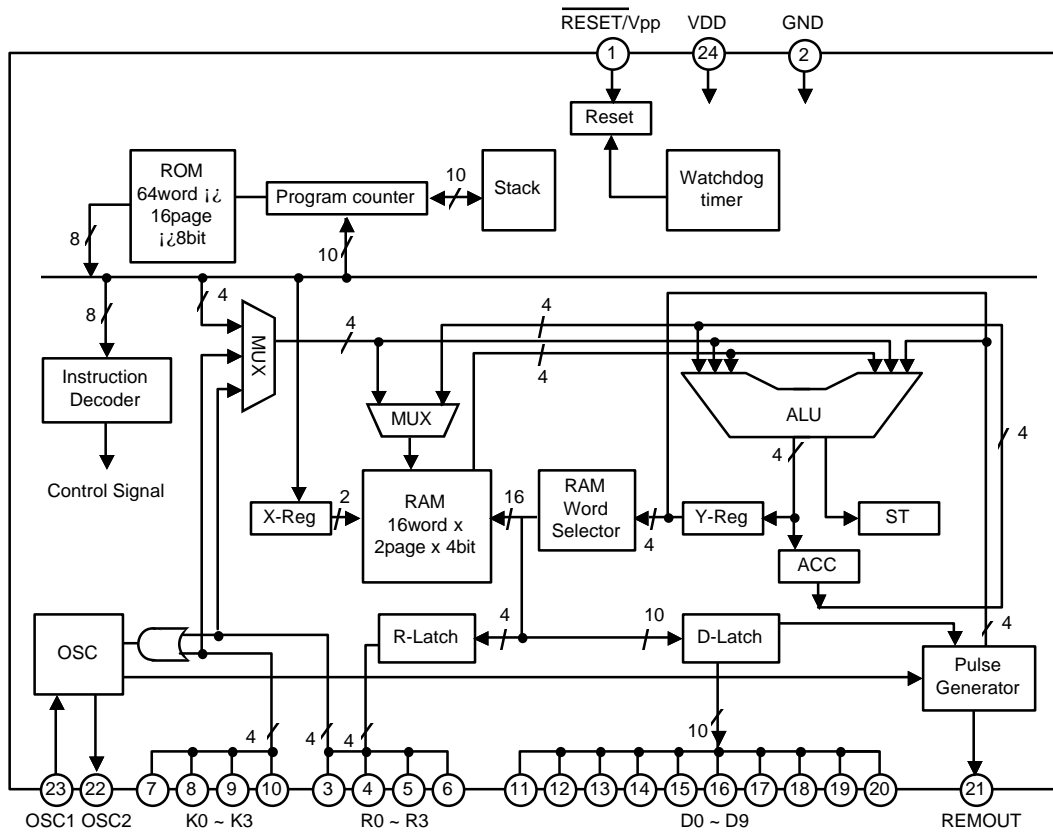


Fig 1-1 Block Diagram (In case of GMS34140T)

Pin Assignment and terminals

Pin Assignment

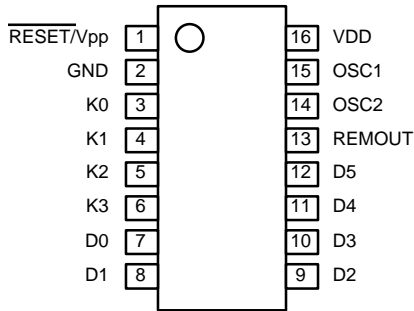


Fig 1-2 GMS34004T Pin Assignment (16PDIP)

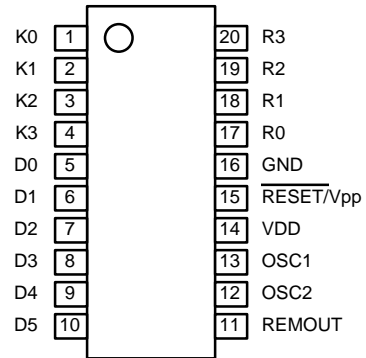


Fig 1-3 GMS34112T Pin Assignment (20DIP/SOP)

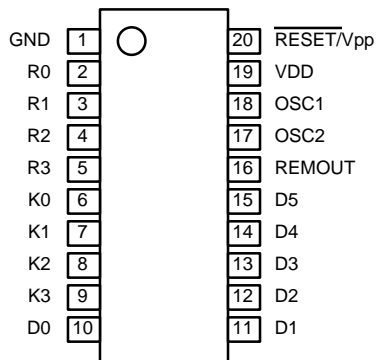


Fig 1-4 GMS34112T Pin Assignment (20SSOP only)

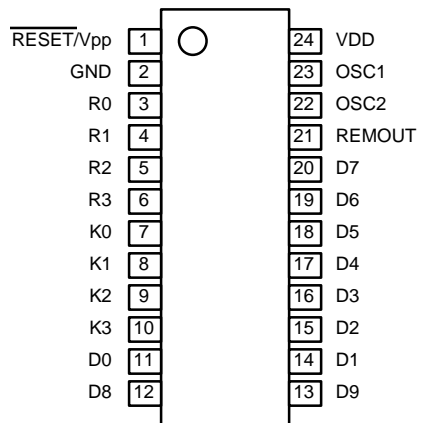


Fig 1-5 GMS34140T Pin Assignment (24DIP/SOP)

Chapter 1. Introduction

Pin Dimension

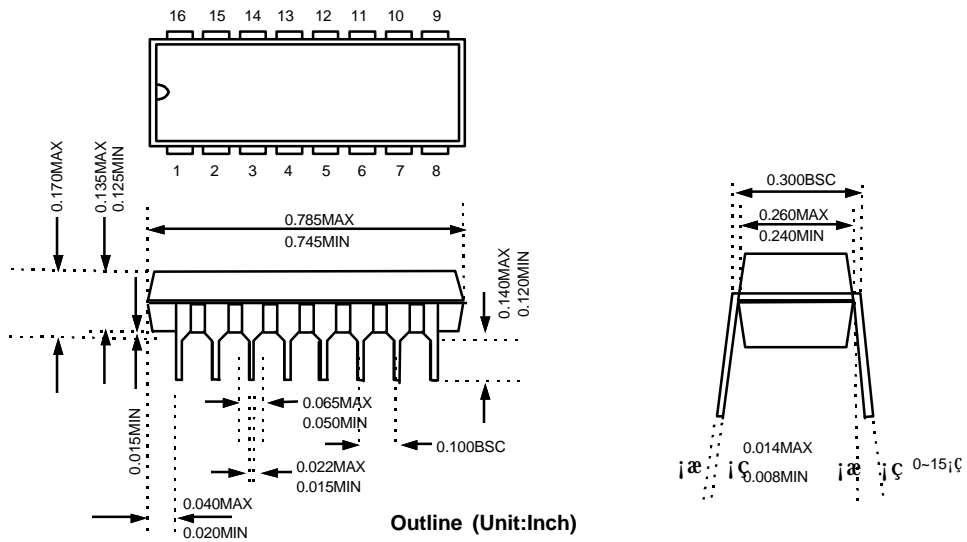


Fig 1-6 16PDIP Pin Dimension

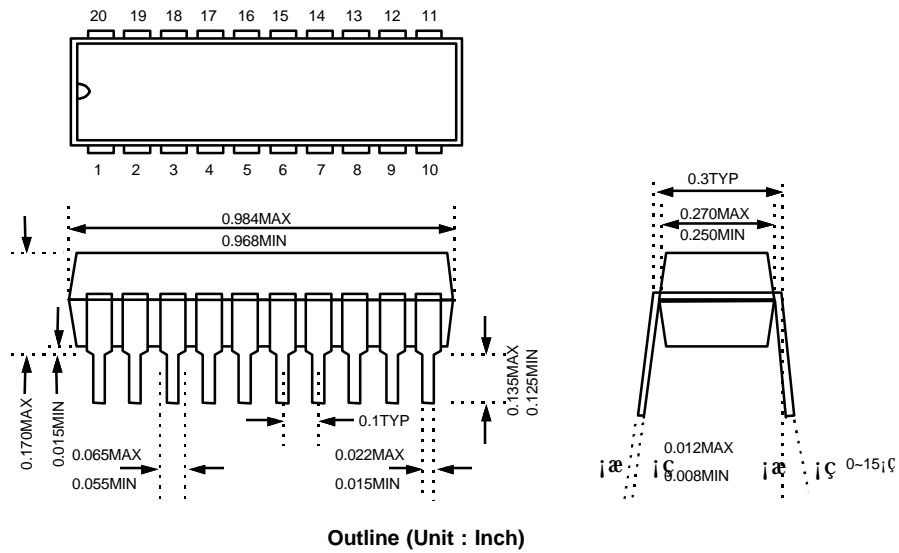


Fig 1-7 20PDIP Pin Dimension

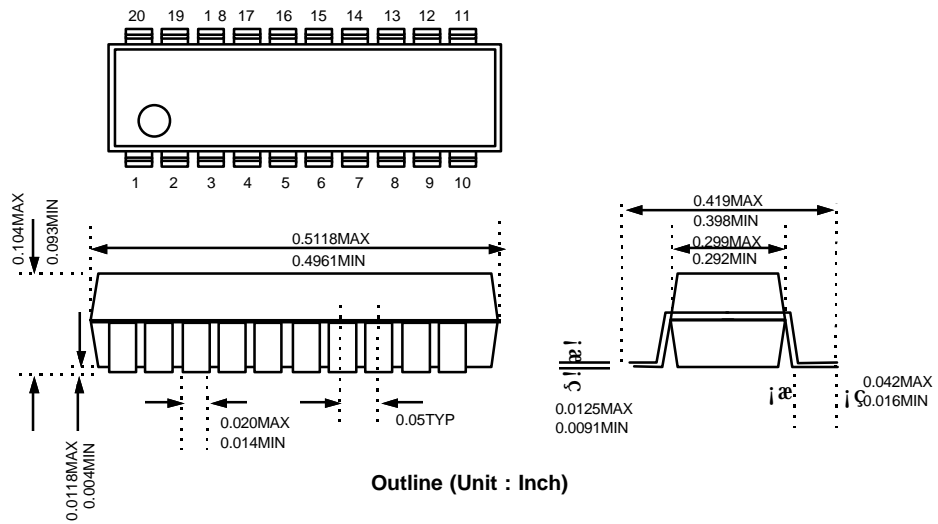


Fig 1-8 20SOP Pin Dimension

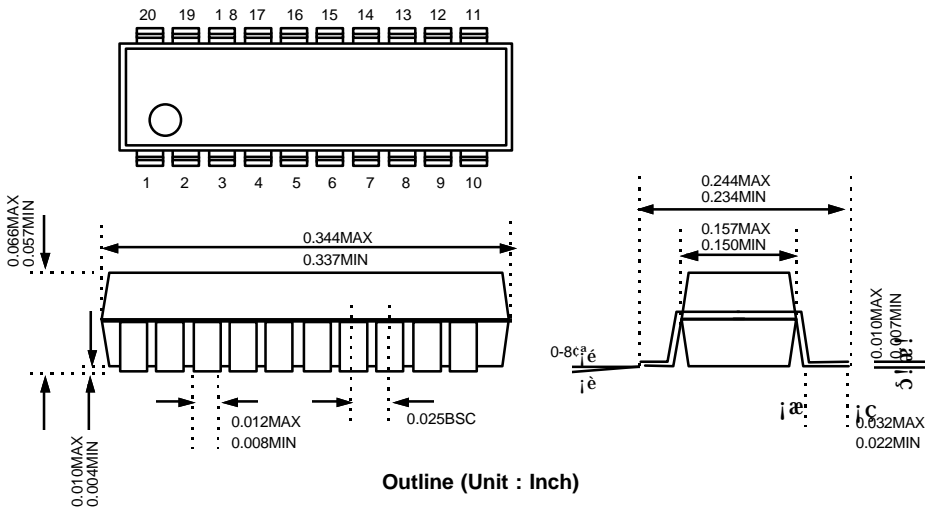


Fig 1-9 20SSOP Pin Dimension

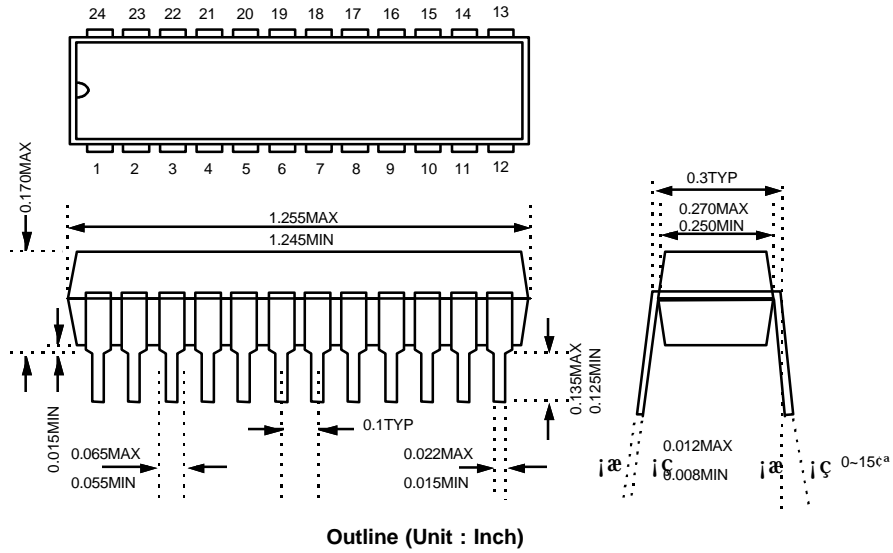


Fig 1-10 24Skinny DIP Pin Dimension

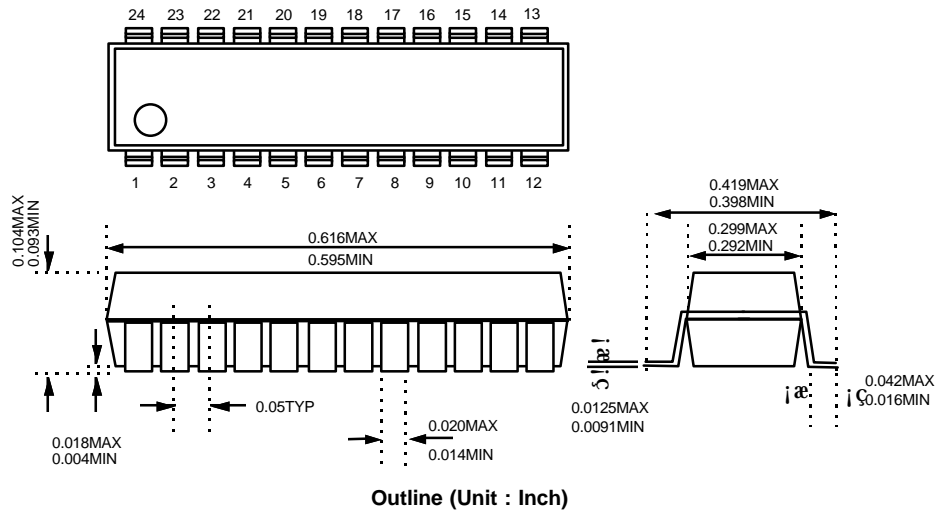


Fig 1-11 24SOP Pin Dimension

Pin Description and Circuit

Pin Description

| Pin | I/O | Function |
|---------------------------|--------|---|
| V _{DD} | - | Connected to 2.2~4.5V power supply at KHz and MHz version or 4.0 ~ 5.5V power supply at WIDE version. |
| GND | - | Connected to 0V power supply. |
| $\overline{\text{RESET}}$ | Input | Used to input a manual reset. When the pin goes "L", the D-output ports and REMOUT-output port are initialized to "L", and ROM address is set to address 0 on page 0. For programming, this pin receives 12.5V programming voltage. |
| K0~K3 | Input | 4-bit input port. STOP mode is released by "L" input of each pin. |
| D0~D9 | Output | The output is the structure of N-channel-open-drain. |
| R0~R3 | I/O | 4-bit I/O port. (Input mode is set only when each of them output "H".) In outputting, each can be set and reset independently(or at once.) The output is in the form of C-MOS. STOP mode is released by "L" input of each pin. |
| REMOUT | Output | High current output port. The output is in the form of C-MOS. The state of large current on is "H". |
| OSC1 | Input | Oscillator input. Input to the oscillator circuit and connection point for ceramic resonator. Internal capacitors available at KHz version. A feedback resistor is connected between this pin and OSC2. |
| OSC2 | Output | Connect a resonator between this pin and OSC1. |

Chapter 1. Introduction

I/O circuit types and options

| Pin | I/O | I/O circuit | Note |
|-----------|-----|-------------|--|
| Reset/Vpp | I | | Hysteresis Input Type. Built in pull-up-resistor, Typical 800Ω |
| R0-R3 | I/O | | CMOS output. "H" output at reset. Built in MOS Tr for pull-up about 120Ω. |
| K0-K3 | I | | Built in MOS Tr for pull-up About 120Ω. |
| D0-D9 | O | | Open drain output. "L" output at reset. |
| REMOUT | O | | CMOS output. "L" output at reset. High current output source. |

| Pin | I/O | I/O circuit | Note |
|------|-----|-------------|--|
| OSC2 | O | | <p>Built in feedback-resistor about $1\text{k}\Omega$</p> <p>Built in damping-resistor $R_d = 4\text{k}\Omega$ [No resistor in MHz operation]</p> <p>Built in resonance Capacitor at KHz version $C_1=C_2 = 100\text{pF} \pm 15\%$ [C_1, C_2 are not available for MHz and WIDE version]</p> |
| OSC1 | I | | |

| Frequency | Resonator Maker | Part Name | Load Capacitor |
|--------------------------------------|-----------------|-----------|-----------------------|
| 320KHz | CQ | ZTB320D | $C_1=C_2=\text{Open}$ |
| 500KHz | CQ | ZTB500E | $C_1=C_2=\text{Open}$ |
| CQ recommend 430KHz~500KHz resonator | | | |
| 3.43MHz | CQ | ZTA3.43MG | $C_1=C_2=30\text{pF}$ |
| 3.52MHz | TDK | FCR3.52M5 | $C_1=C_2=33\text{pF}$ |
| 3.64MHz | CQ | ZTA3.64MG | $C_1=C_2=30\text{pF}$ |
| | TDK | FCR3.64M5 | $C_1=C_2=33\text{pF}$ |
| 3.84MHz | CQ | ZTA3.84MG | $C_1=C_2=30\text{pF}$ |
| | TDK | FCR3.84M5 | $C_1=C_2=33\text{pF}$ |
| 4.00MHz | CQ | ZTA4.00MG | $C_1=C_2=30\text{pF}$ |

Chapter 1. Introduction

Electrical Characteristics

Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

| Parameter | Symbol | Max. rating | Unit |
|---------------------------|-----------|---------------------|------------------|
| Supply Voltage | V_{DD} | -0.3 ~ 7.0 | V |
| Programming Voltage | V_{PP} | -0.3 ~ 13.5 | V |
| Power dissipation | P_D | 700 * | mW |
| Storage temperature range | T_{stg} | -55 ~ 125 | $^\circ\text{C}$ |
| Input voltage | V_{IN} | -0.3 ~ $V_{DD}+0.3$ | V |
| Output voltage | V_{OUT} | -0.3 ~ $V_{DD}+0.3$ | V |

* Thermal derating above 25°C : 6mW per degree $^\circ\text{C}$ rise in temperature.

Recommended operation condition

| Parameter | Symbol | Condition | Rating | Unit |
|-----------------------|-----------|-----------------|-----------|------------------|
| Supply Voltage | V_{DD} | 300 ~ 500KHz | 2.2 ~ 4.5 | V |
| | | 2.4 ~ 4MHz | 2.2 ~ 4.5 | |
| | | 300KHz ~ 4.2MHz | 4.0 ~ 5.5 | |
| Operating temperature | T_{opr} | - | -20 ~ +70 | $^\circ\text{C}$ |

Chapter 1. Introduction

Electrical characteristics for low voltage products ($T_a=25^\circ\text{C}$, $V_{DD}=3\text{V}$)

| Parameter | Symbol | Limits | | | Unit | Condition | |
|-----------------------------|--------------|-----------|------|------|---------------|---|-------------|
| | | Min. | Typ. | Max. | | | |
| Input H current | I_{IH} | - | - | 1 | μA | $V_I=V_{DD}$ | |
| RESET input L current | I_{IL2} | -2 | -7.5 | -16 | μA | $V_I=\text{GND}$ | |
| K, R input L current | I_{IL1} | -9 | -25 | -50 | μA | $V_I=\text{GND}$, Output off, Pull-Up resistor provided. | |
| K, R input H voltage | V_{IH1} | 2.1 | - | - | V | - | |
| K, R input L voltage | V_{IL1} | - | - | 0.9 | V | - | |
| RESET input H voltage | V_{IH2} | 2.25 | - | - | V | - | |
| RESET input L voltage | V_{IL2} | - | - | 0.75 | V | V | |
| D, R output L voltage | V_{OL2} | - | 0.15 | 0.4 | V | $I_{OL}=1\text{mA}$ | |
| REMOUT output L voltage | V_{OL1} | - | 0.15 | 0.4 | V | $I_{OL}=100\mu\text{A}$ | |
| REMOUT output H voltage | V_{OH1} | 2.1 | 2.5 | - | V | $I_{OH}=-8\text{mA}$ | |
| OSC2 output L voltage | V_{OL3} | - | 0.4 | 0.9 | V | $I_{OL}=70\mu\text{A}$ | |
| OSC2 output H voltage | V_{OH3} | 2.1 | 2.5 | - | V | $I_{OH}=70\mu\text{A}$ | |
| D, R output leakage current | I_{OL} | - | - | 1 | μA | $V_{OUT}=V_{DD}$, Output off | |
| Current on STOP mode | I_{STOP} | - | - | 1 | μA | At STOP mode | |
| Operating supply current 1 | I_{DD1}^* | - | 0.3 | 4.0 | mA | $f_{OSC}=455\text{KHz}$ | |
| Operating supply current 2 | I_{DD2}^* | - | 0.5 | 4.0 | mA | $f_{OSC}=4\text{MHz}$ | |
| System clock frequency | $f_{OSC}/6$ | f_{OSC} | 300 | - | 500 | KHz | KHz version |
| | $f_{OSC}/48$ | f_{OSC} | 2.4 | - | 4 | MHz | MHz version |

* I_{DD1} , I_{DD2} , is measured at RESET mode.

Chapter 1. Introduction

Electrical characteristics ($T_a=25\text{ }^\circ\text{C}$, $V_{DD}=5\text{V}$)

| Parameter | Symbol | Limits | | | Unit | Condition | |
|-----------------------------|-------------|---------------|------|---------------|---------------|---|--------------|
| | | Min. | Typ. | Max. | | | |
| Input H current | I_{IH} | - | - | 5 | μA | $V_I=V_{DD}$ | |
| RESET input L current | I_{IL2} | -2 | - | -20 | μA | $V_I=\text{GND}$ | |
| K, R input L current | I_{IL1} | -9 | - | -150 | μA | $V_I=\text{GND}$, Output off, Pull-Up resistor provided. | |
| K, R input H voltage | V_{IH1} | $0.7*V_{DD}$ | - | - | V | - | |
| K, R input L voltage | V_{IL1} | - | - | $0.3*V_{DD}$ | V | - | |
| RESET input H voltage | V_{IH2} | $0.75*V_{DD}$ | - | - | V | - | |
| RESET input L voltage | V_{IL2} | - | - | $0.25*V_{DD}$ | V | V | |
| D, R output L voltage | V_{OL2} | - | - | 0.4 | V | $I_{OL}=2\text{mA}$ | |
| REMOUT output L voltage | V_{OL1} | - | - | 0.4 | V | $I_{OL}=100\mu\text{A}$ | |
| REMOUT output H voltage | V_{OH1} | $V_{DD}-1.0$ | - | - | V | $I_{OH}=-8\text{mA}$ | |
| OSC2 output L voltage | V_{OL3} | - | - | 0.9 | V | $I_{OL}=70\mu\text{A}$ | |
| OSC2 output H voltage | V_{OH3} | $V_{DD}-1.0$ | - | - | V | $I_{OH}=-70\mu\text{A}$ | |
| D, R output leakage current | I_{OL} | - | - | 5 | μA | $V_{OUT}=V_{DD}$, Output off | |
| Current on STOP mode | I_{STOP} | - | - | 10 | μA | At STOP mode | |
| Operating supply current | I_{DD} | - | - | 10 | mA | At RESET mode | |
| System clock frequency | $f_{osc}/6$ | f_{osc} | 0.3 | - | 4.2 | MHz | WIDE version |

| | |
|---------------------|----------|
| INTRODUCTION | 1 |
| ARCHITECTURE | 2 |
| INSTRUCTION | 3 |
| EPROM | 4 |

CHAPTER 2. Architecture

BLOCK DESCRIPTION

Program Memory (EPROM)

The GMS34XXXT series can incorporate maximum 1,024 words (64 words/page; 8bits) for program memory. Program counter PC (A0~A5) and page address register (A6~A9) are used to address the whole area of program memory having an instruction (8bits) to be next executed.

The program memory consists of 64 words on each page, and thus each page can hold up to 64 steps of instructions.

The program memory is composed as shown below.

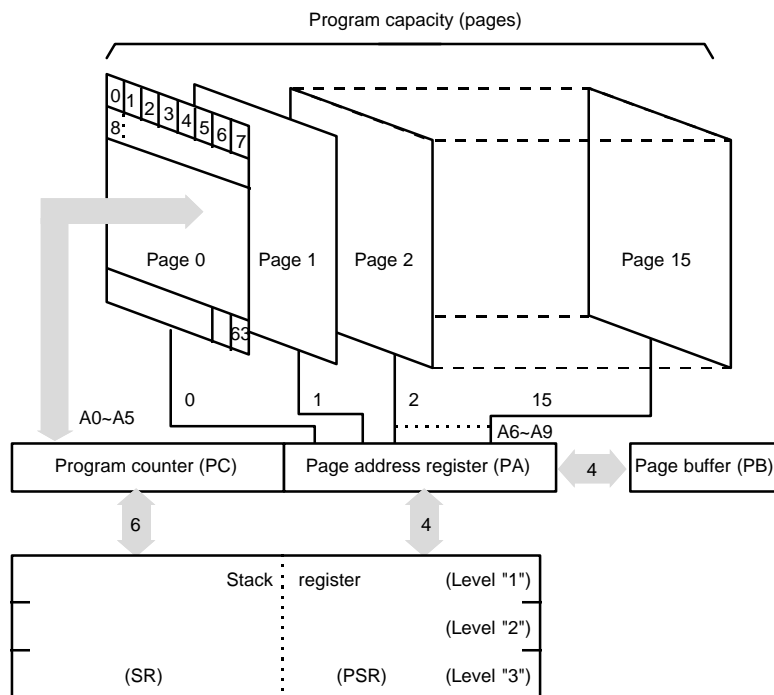


Fig 2-1 Configuration of Program Memory

EPROM Address Register

The following registers are used to address the EPROM.

- Page address register (PA) :
Holds EPROM's page number (0~Fh) to be addressed.
- Page buffer register (PB) :
Value of PB is loaded by an LPBI command when newly addressing a page. Then it is shifted into the PA when rightly executing a branch instruction (BR) and a subroutine call (CAL).
- Program counter (PC) :
Available for addressing word on each page.
- Stack register (SR) :
Stores returned-word address in the subroutine call mode.

(1) Page address register and page buffer register :

Address one of pages #0 to #15 in the EPROM by the 4-bit binary counter. Unlike the program counter, the page address register is usually unchanged so that the program will repeat on the same page unless a page changing command is issued. To change the page address, take two steps such as (1) writing in the page buffer what page to jump (execution of LPBI) and (2) execution of BR or CAL, because instruction code is of eight bits so that page and word can not be specified at the same time. In case a return instruction (RTN) is executed within the subroutine that has been called in the other page, the page address will be changed at the same time.

(2) Program counter :

This 6-bit binary counter increments for each fetch to address a word in the currently addressed page having an instruction to be next executed. For easier programming, at turning on the power, the program counter is reset to the zero location. The PA is also set to "0". Then the program counter specifies the next EPROM address in random sequence. When BR, CAL or RTN instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (a_0 to a_5), or for RTN, and address is fetched from stack register No. 1.

(3) Stack register :

This stack register provides two stages each for the program counter (6 bits) and the page address register (4bits) so that subroutine nesting can be made on two levels.

Data memory (RAM)

Up to 32 nibbles (16 words ; 2pages ; 4bits) is incorporated for storing data. The whole data memory area is indirectly specified by a data pointer (X,Y). Page number is specified by zero bit of X register, and words in the page by 4 bits in Y-register. Data memory is composed in 16 nibbles/page. Figure 2-2 shows the configuration.

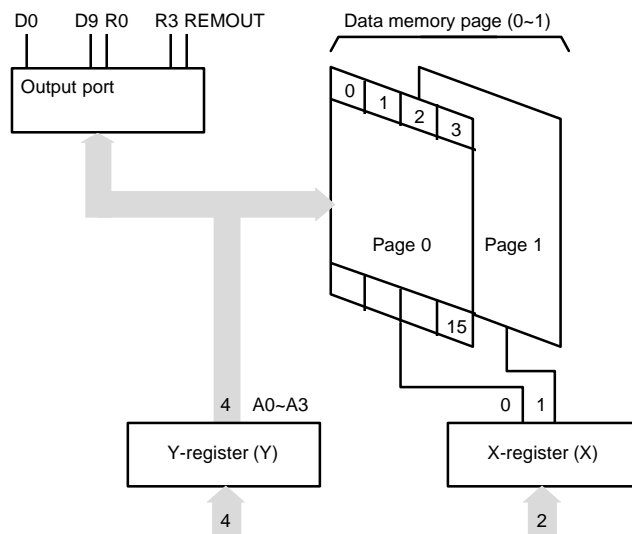


Fig 2-2 Composition of Data Memory

X-register (X)

X-register is consist of 2bit, X0 is a data pointer of page in the RAM, X1 is only used for selecting of D8~D9 with value of Y-register

| | X1=0 | X1=1 |
|-----|------|------|
| Y=0 | D0 | D8 |
| Y=1 | D1 | D9 |

Table 2-1 Mapping table between X and Y register

Y-register (Y)

Y-register has 4 bits. It operates as a data pointer or a general-purpose register. Y-register specifies an address ($a_0 \sim a_3$) in a page of data memory, as well as it is used to specify an output port. Further it is used to specify a mode of carrier signal outputted from the REMOUT port. It can also be treated as a general-purpose register on a program.

Accumulator (A_{CC})

The 4-bit register for holding data and calculation results.

Arithmetic and Logic Unit (ALU)

In this unit, 4bits of adder/comparator are connected in parallel as it's main components and they are combined with status latch and status logic (flag.)

(1) Operation circuit (ALU) :

The adder/comparator serves fundamentally for full addition and data comparison. It executes subtraction by making a complement by processing an inversed output of A_{CC} ($A_{CC}+1$)

(2) Status logic :

This is to bring an ST, or flag to control the flow of a program. It occurs when a specified instruction is executed in three cases such as overflow or underflow in operation and two inputs unequal.

State Counter (SC)

A fundamental machine cycle timing chart is shown below. Every instruction is one byte length. Its execution time is the same. Execution of one instruction takes 6 clocks for fetch cycle and 6 clocks for execute cycle (12 clocks in total). Virtually these two cycles proceed simultaneously, and thus it is apparently completed in 6 clocks (one machine cycle). Exceptionally BR, CAL and RTN instructions is normal execution time since they change an addressing sequentially. Therefore, the next instruction is prefetched so that its execution is completed within the fetch cycle.

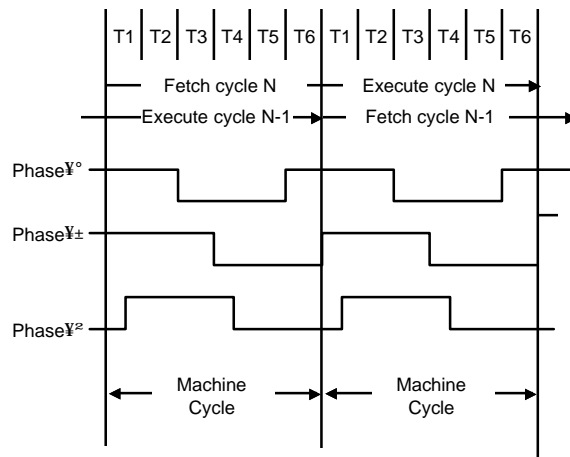


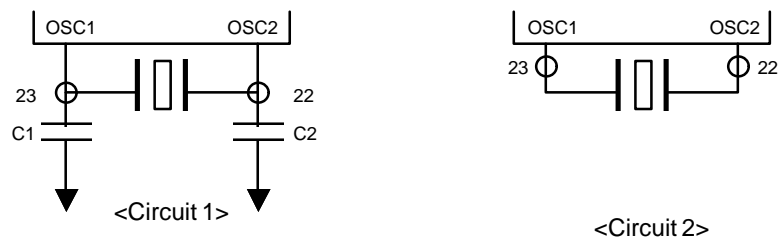
Fig. 2-3 Fundamental timing chart

Chapter 2. Architecture

Clock Generator

The GMS34XXXT series has an internal clock oscillator. The oscillator circuit is designed to operate with an external ceramic resonator. Internal capacitors are available at KHz version. Oscillator circuit is able to organize by connecting ceramic resonator to outside.

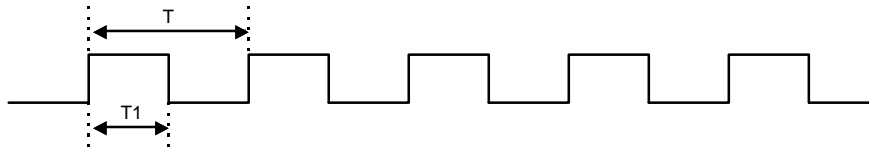
* It is necessary to connect capacitor to outside in order to change ceramic resonator, you must refer to a manufacturer's resonator matching guide.



| Version | Operating Frequency | Oscillation Circuit | |
|---------|---------------------|-----------------------|-----------|
| KHz | 300KHz ~ 500KHz | Internal capacitor | Circuit 2 |
| | | No Internal capacitor | Circuit 1 |
| MHz | 2.4MHz ~ 4MHz | No Internal capacitor | Circuit 1 |
| WIDE | 300KHz ~ 4.2MHz | No Internal capacitor | Circuit 1 |

Pulse generator

The following frequency and duty ratio are selected for carrier signal outputted from the REMOUT port depending on a PMR (Pulse Mode Register) value set in a program.



| PMR | REMOUT signal |
|-----|---|
| 0 | $T=1/f_{PUL} = 12/f_{OSC} [96/f_{OSC}]$, $T1/T = 1/2$ |
| 1 | $T=1/f_{PUL} = 12/f_{OSC} [96/f_{OSC}]$, $T1/T = 1/3$ |
| 2 | $T=1/f_{PUL} = 8/f_{OSC} [64/f_{OSC}]$, $T1/T = 1/2$ |
| 3 | $T=1/f_{PUL} = 8/f_{OSC} [64/f_{OSC}]$, $T1/T = 1/4$ |
| 4 | $T=1/f_{PUL} = 11/f_{OSC} [88/f_{OSC}]$, $T1/T = 4/11$ |
| 5 | No Pulse (same to D0~D9) |
| 6 | $T=1/f_{PUL} = 12/f_{OSC} [96/f_{OSC}]$, $T1/T = 1/4$ |
| 7 | No pulse (same to D0 ~ D9) |

* Default value is "0"

* [] means the value of "T", when Instruction cycle is $f_{OSC}/48$ in MHz version

Table 2-2 PMR selection table

Chapter 2. Architecture

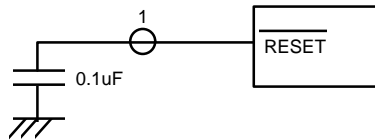
Initial Reset Circuit

$\overline{\text{RESET}}$ pin must be down to "L" more than 4 machine cycle by outside capacitor or other for power on reset.

The mean of 1 machine cycle is $6/f_{\text{OSC}}$ or $48/f_{\text{OSC}}$, however, operating voltage must be in recommended operating conditions, and clock oscillating stability.

* It is required to adjust C value depending on rising time of power supply.

(Example shows the case of rising time shorter than 10ms.)



Watch Dog Timer (WDT)

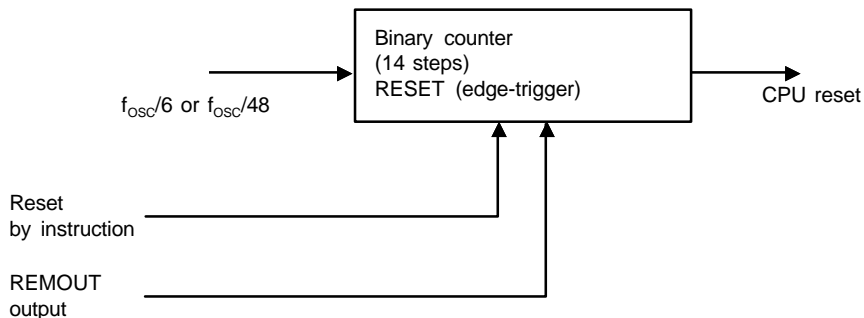
Watch dog timer is organized binary of 14 steps. The signal of $f_{\text{OSC}}/6$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized.

The overflow time is $6 \times 2^{13}/f_{\text{OSC}}$ (108.026ms at $f_{\text{OSC}}=455\text{KHz}$.)

$8 \times 6 \times 2^{13}/f_{\text{OSC}}$ (108.026ms at $f_{\text{OSC}} = 3.64\text{MHz}$)

Normally, the binary counter must be reset before the overflow by using reset instruction (WDTR) or / and REMOUT port HIGH(Y-reg=8, So instruction execution).

* It is constantly reset in STOP mode. When STOP is released, counting is restarted. (Refer to 2-9 STOP function>)



STOP Operation

Stop mode can be achieved by STOP instructions.

In stop mode :

1. Oscillator is stopped, the operating current is low.
2. Watch dog timer is reset, D8~D9 output and REMOUT output are "L".
3. Part other than WDT, D8~D9 output and REMOUT output have a value before come into stop mode.

Stop mode is released when one of K or R input is going to "L".

1. State of D0~D7 output and REMOUT output is return to state of before stop mode is achieved.
2. After 1,024 μ s enable clocks for stable oscillating, First instruction start to operate.
3. In return to normal operation, WDT is counted from zero again.

But, at executing stop instruction, if one of K or R input is chosen to "L", stop instruction is same to NOP instruction.

Port Operation

| Value of X-reg | Value of X-reg | Operation |
|----------------|----------------|--|
| 0 or 1 | 0 ~ 7 | S0 : D(Y) \bar{I} 1, R0 : D(Y) \bar{I} 0 |
| 0 or 1 | 8 | REMOUT port repeats "H" and "L" in pulse frequency. (When PMR = 5, it is fixed at "H") S0 : REMOUT(PMR) \bar{I} 1 R0 : REMOUT(PMR) \bar{I} 0 |
| 0 or 1 | 9 | S0 : D0 ~ D9 \bar{I} 1 (High-Z) R0 : D0 ~ D9 \bar{I} 0 |
| 0 or 1 | A ~ D | S0 : R(Y-Ah) \bar{I} 1 R0 : R(Y-Ah) \bar{I} 0 |
| 0 or 1 | E | S0 : R0 ~ R3 \bar{I} 1 R0 : R0 ~ R3 \bar{I} 0 |
| 0 or 1 | F | S0 : D0 ~ D9 \bar{I} 1, R0 ~ R3 \bar{I} 1 R0 : D0 ~ D9 \bar{I} 0, R0 ~ R3 \bar{I} 0 |
| 2 or 3 | 0 | S0 : D(8) \bar{I} 1 R0 : D(8) \bar{I} 0 |
| 2 or 3 | 1 | S0 : D(9) \bar{I} 1 R0 : D(9) \bar{I} 0 |

| | |
|---------------------|----------|
| INTRODUCTION | 1 |
|---------------------|----------|

| | |
|---------------------|----------|
| ARCHITECTURE | 2 |
|---------------------|----------|

| | |
|--------------------|----------|
| INSTRUCTION | 3 |
|--------------------|----------|

| | |
|--------------|----------|
| EPROM | 4 |
|--------------|----------|

CHAPTER 3. Instruction

Instruction Table

The GMS34XXXT series provides the following 43 basic instructions.

| | Category | Mnemonic | Function | ST ¹ |
|----|----------------------|----------|---|-----------------|
| 1 | Register to Register | LAY | $A \text{ } i \text{ } \zeta \text{ } Y$ | S |
| 2 | | LYA | $Y \text{ } i \text{ } \zeta \text{ } A$ | S |
| 3 | | LAZ | $A \text{ } i \text{ } \zeta \text{ } 0$ | S |
| 4 | RAM to Register | LMA | $M(X,Y) \text{ } i \text{ } \zeta \text{ } A$ | S |
| 5 | | LMAIY | $M(X,Y) \text{ } i \text{ } \zeta \text{ } A, Y \text{ } i \text{ } \zeta \text{ } Y+1$ | S |
| 6 | | LYM | $Y \text{ } i \text{ } \zeta \text{ } M(X,Y)$ | S |
| 7 | | LAM | $A \text{ } i \text{ } \zeta \text{ } M(X,Y)$ | S |
| 8 | | XMA | $A \text{ } i \text{ } \hat{e} \text{ } M(X,Y)$ | S |
| 9 | Immediate | LYI i | $Y \text{ } i \text{ } \zeta \text{ } i$ | S |
| 10 | | LMIIY i | $M(X,Y) \text{ } i \text{ } \zeta \text{ } i, Y \text{ } i \text{ } \zeta \text{ } Y+1$ | S |
| 11 | | LXI n | $X \text{ } i \text{ } \zeta \text{ } n$ | S |
| 12 | RAM Bit Manipulation | SEM n | $M(n) \text{ } i \text{ } \zeta \text{ } 1$ | S |
| 13 | | REM n | $M(n) \text{ } i \text{ } \zeta \text{ } 0$ | S |
| 14 | | TM n | TEST $M(n) = 1$ | E |
| 15 | ROM Address | BR a | if $ST = 1$ then Branch | S |
| 16 | | CAL a | if $ST = 1$ then Subroutine call | S |
| 17 | | RTN | Return from Subroutine | S |
| 18 | | LPBI i | $PB \text{ } i \text{ } \zeta \text{ } i$ | S |
| 19 | Arithmetic | AM | $A \text{ } i \text{ } \zeta \text{ } A + M(X,Y)$ | C |
| 20 | | SM | $A \text{ } i \text{ } \zeta \text{ } M(X,Y) - A$ | B |
| 21 | | IM | $A \text{ } i \text{ } \zeta \text{ } M(X,Y) + 1$ | C |
| 22 | | DM | $A \text{ } i \text{ } \zeta \text{ } M(X,Y) - 1$ | B |
| 23 | | IA | $A \text{ } i \text{ } \zeta \text{ } A + 1$ | S |
| 24 | | IY | $Y \text{ } i \text{ } \zeta \text{ } Y + 1$ | C |
| 25 | | DA | $A \text{ } i \text{ } \zeta \text{ } A - 1$ | B |

Chapter 3. Instruction

| | Category | Mnemonic | Function | ST ^{*1} |
|----|----------------|----------|---------------------------------|------------------|
| 26 | Arithmetic | DY | $Y \leftarrow Y - 1$ | B |
| 27 | | EORM | $A \leftarrow A \oplus M(X,Y)$ | S |
| 28 | | NEGA | $A \leftarrow \overline{A} + 1$ | Z |
| 29 | Comparison | ALEM | TEST $A \hat{=} M(X,Y)$ | E |
| 30 | | ALEI i | TEST $A \hat{=} i$ | E |
| 31 | | MNEZ | TEST $M(X,Y) \hat{=} 0$ | N |
| 32 | | YNEA | TEST $Y \hat{=} A$ | N |
| 33 | | YNEI i | TEST $Y \hat{=} i$ | N |
| 34 | | KNEZ | TEST $K \hat{=} 0$ | N |
| 35 | | RNEZ | TEST $R \hat{=} 0$ | N |
| 36 | Input / Output | LAK | $A \leftarrow K$ | S |
| 37 | | LAR | $A \leftarrow R$ | S |
| 38 | | SO | Output(Y) $\leftarrow 1^2$ | S |
| 39 | | RO | Output(Y) $\leftarrow 0^2$ | S |
| 40 | Control | WDTR | Watch Dog Timer Reset | S |
| 41 | | STOP | Stop operation | S |
| 42 | | LPY | $PMR \leftarrow Y$ | S |
| 43 | | NOP | No operation | S |


Note) i = 0~f, n = 0~3, a = 6bit PC Address

*1 Column ST indicates conditions for changing status. Symbols have the following meanings

- S : On executing an instruction, status is unconditionally set.
- C : Status is only set when carry or borrow has occurred in operation.
- B : Status is only set when borrow has not occurred in operation.
- E : Status is only set when equality is found in comparison.
- N : Status is only set when equality is not found in comparison.
- Z : Status is only set when the result is zero.

*2 Operation is settled by a value of Y-register.

| | |
|---------------------|----------|
| INTRODUCTION | 1 |
| ARCHITECTURE | 2 |
| INSTRUCTION | 3 |
| EPROM | 4 |



CHAPTER 4. EPROM

GMS34004TK / 34112TK / 34140TK

Mode define

| Item | | Device operation | Mode setting | | |
|-----------------------|-----------------|-----------------------------|-----------------|-----------|--|
| User mode | | Exact User pgm | RESETB = 0 ~ 3V | | Vcc=3V |
| EPROM read mode | | Address in, Data out | RESETB =12.5V | K3-0=0110 | Vcc=6.0V |
| EPROM Program mode | 1Byte PGM Write | Address in, Data in | RESETB =12.5V | K3-0=0110 | Vcc=6.0V |
| | 2Byte PGM Write | Address in, Data in | | K3-0=0111 | |
| | Program verify | Address in, Data out | | - | |
| Lock bit Program mode | Lock bit Write | Lock bit write(set D5 to 1) | RESETB =12.5V | K3-0=0100 | Vcc=6.0V, Lock bit is D5. (Default : unlock) |
| | Lock bit Read | Lock bit out | | K3-0=0101 | |

Chapter 4. EPROM

Port define

| Port Name | User Mode | EPROM Mode | | | |
|-----------|-----------------|--|----|-----|-----|
| VDD | 3.0V | 6.0V | | | |
| RESETB | Reset (0, 3.0V) | Vpp (0, 12.5V) | | | |
| OSC1 | Clock input | Clock input | | | |
| K0 | K0(Input) | Read / Write Control Address / Data Control | | | |
| K1 | K1(Input) | | | | |
| K2 | K2(Input) | | | | |
| K3 | K3(Input) | | | | |
| D0 | D0(Output) | A0 | A5 | Da0 | Da4 |
| D1 | D1(Output) | A1 | A6 | Da1 | Da5 |
| D2 | D2(Output) | A2 | A7 | Da2 | Da6 |
| D3 | D3(Output) | A3 | A8 | Da3 | Da7 |
| D4 | D4(Output) | A4 | A9 | - | - |
| D5 | D5(Output) | Lock bit output | | | |
| GND | 0V | | | | |

NMOS open drain I/O
in EPROM mode

* Undefined ports in this table are N.C (No Connection)

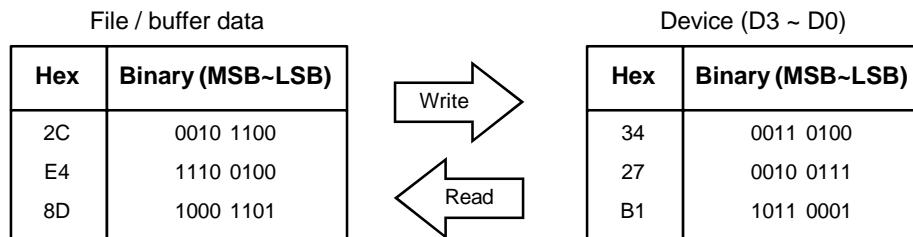
Programming data

| Device Name | ROM Size | Blank data (HEX) | Lock bit | Device address | File address |
|-------------|------------|---------------------|----------|----------------|--------------|
| GMS34004TK | 512bytes | FF | Yes | 0000 ~ 01FF | 0000 ~ 01FF |
| GMS34112TK | 1,024bytes | FF | Yes | 0000 ~ 03FF | 0000 ~ 03FF |
| GMS34140TK | 1,024bytes | FF | Yes | 0000 ~ 03FF | 0000 ~ 03FF |

- If lock bit is set, the EPROM of the device can not be read, because output is always FF.
- Input file : Intel Hexa format (*.RHX)

Write / Read data conversion

- You must change MSB ~ LSB ↔ LSB ~ MSB.
- Example



Checksum

- It is calculated from the Buffer of the programmer.
- Address range is the same as device address.
- Calculate method is the same as normal EPROM devices (ex:27C128, 256 etc)

Programming control

- OSC1 & RESETB control OTP device, so you must count OSC1 clocks in every state.
- K ports control the internal state of the OTP device(ex: Read, Write...).
- D5~D0 ports are NMOS open drain I/O in EPROM mode.
It must be pulled up by resistors (about 4.7~ 47K ohm).
- The frequency rate of the OSC1 clock is 10KHz ~ 500KHz.
You can hold OSC1 HIGH or LOW state when you need.

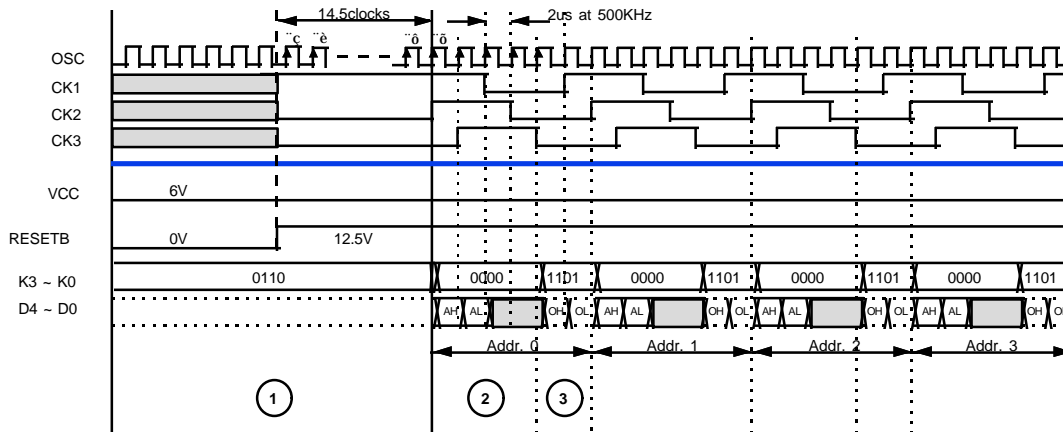
Programming DC specification

| Item | Range |
|--------|---------------------|
| VCC | 0 ~ 6.0V ±0.25V |
| RESETB | 0 ~ 12.5V ±0.5V |
| K-port | 0 ~ 0.2VCC(Low) |
| D-port | 0.8VCC ~ VCC (High) |

Chapter 4. EPROM

EPROM read mode (1/2)

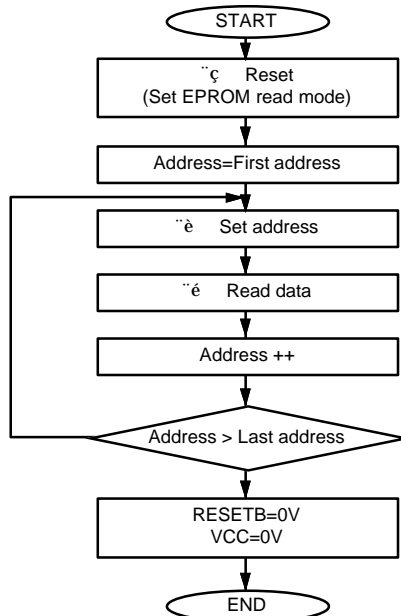
For device verify or read.
If you set Lock bit, output data is always FF.



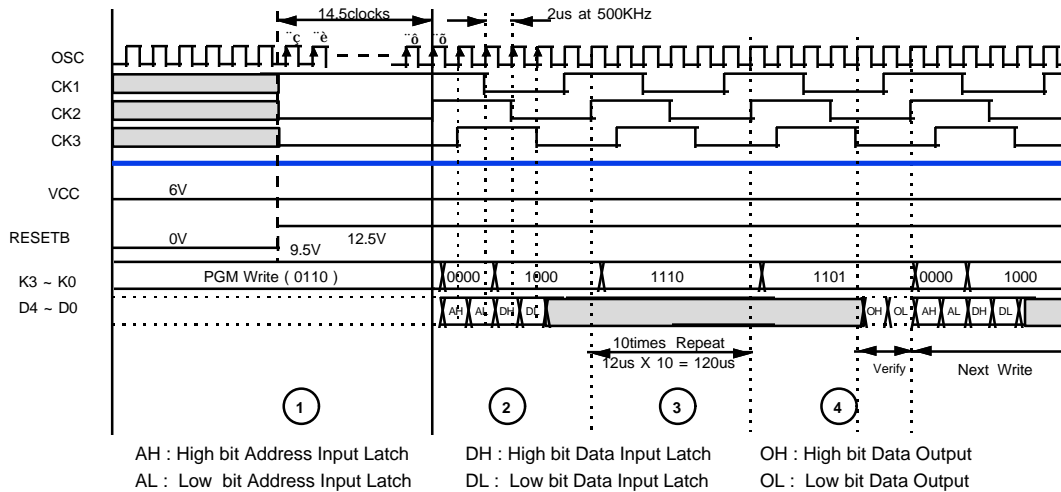
AH : High Address (A9~5) Input Latch OH : High Data (D7~4) Output
AL : Low Address (A4~0) Input Latch OL : Low Data (D3~0) Output

* Note : 1. AH, AL, DH, DL Inputs released at 100~200nS after OSC rising edge and width is 1OSC cycle (if OSC is 500KHz, width is 2µS).

EPROM read mode (2/2)

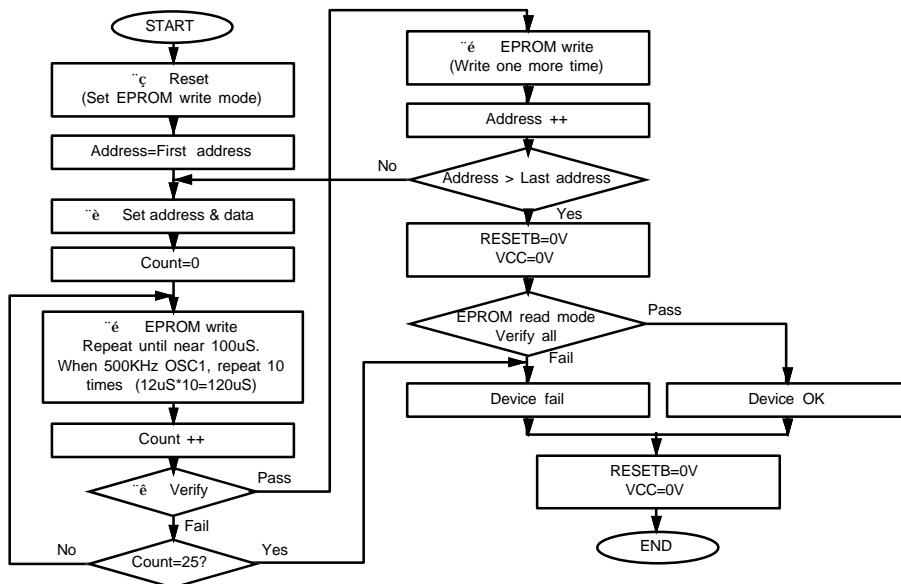


EPROM write mode (1/2)



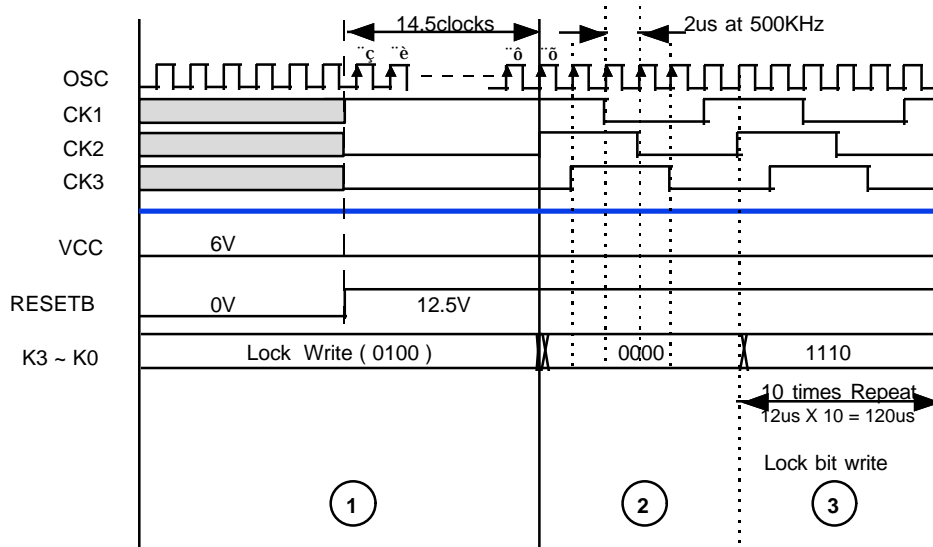
* Note : 1. AH, AL, DH, DL Inputs are released at 100~200nS after OSC rising edge and width is 1OSC cycle (if OSC is 500KHz, width is 2uS).

EPROM write mode (2/2)

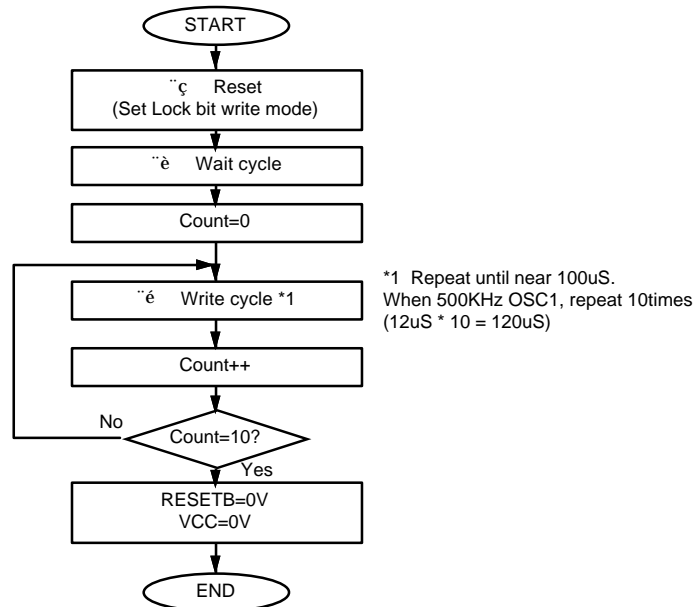


Chapter 4. EPROM

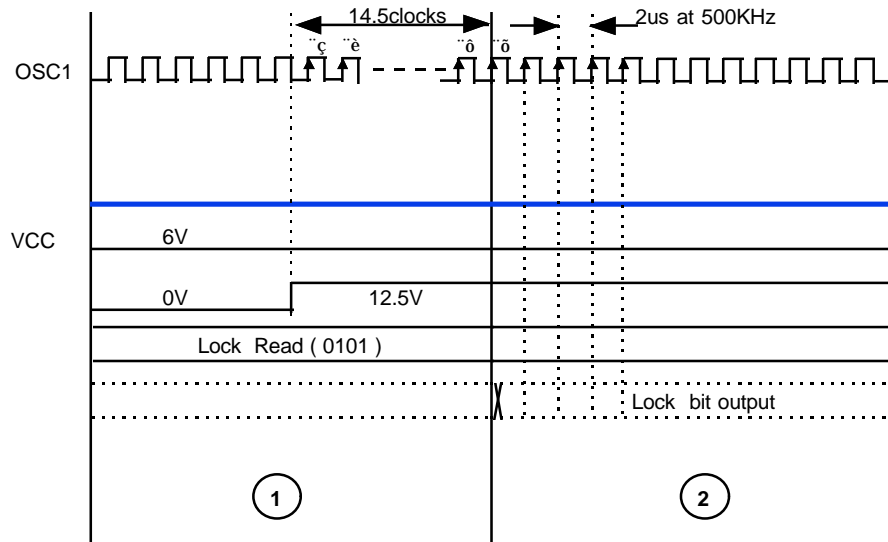
Lock bit write mode (1/2)



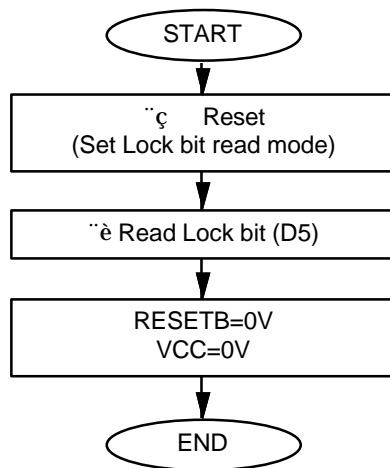
Lock bit write mode (2/2)



Lock bit read mode (1/2)

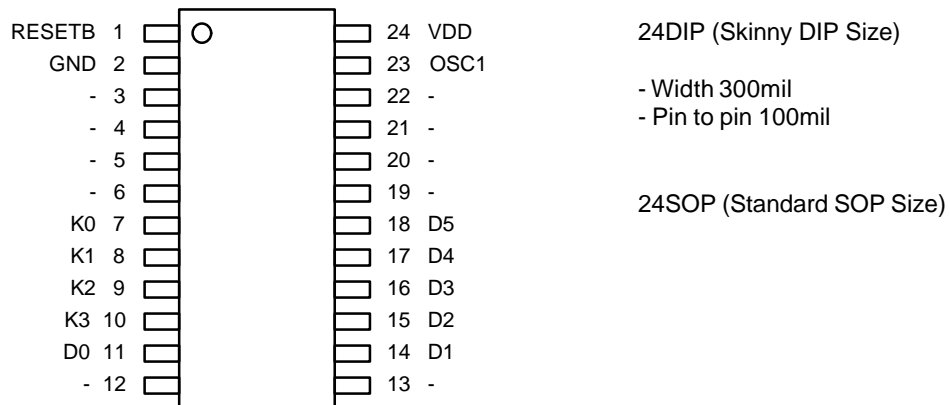
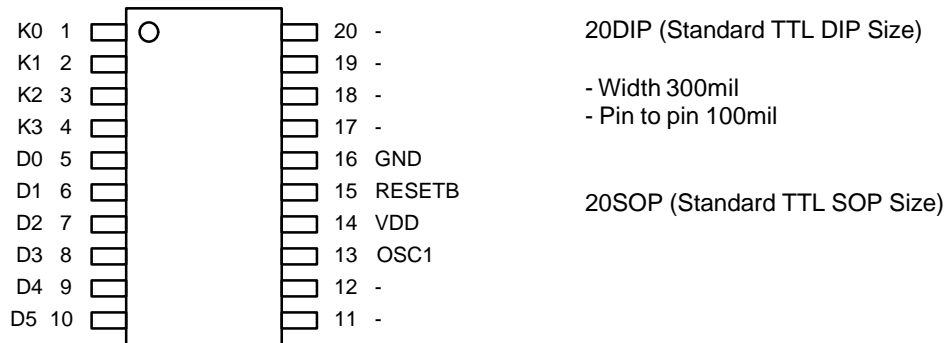
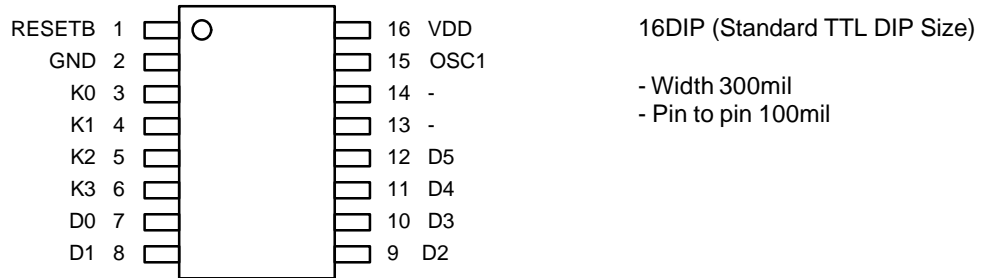


Lock bit read mode (2/2)



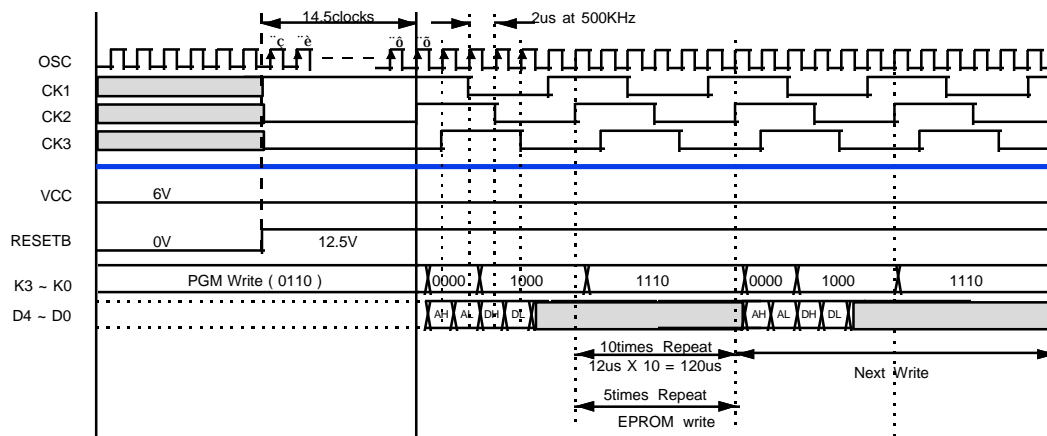
Chapter 4. EPROM

GMS34004T/112T/140T (Pin assignment & Package)



EPROM(KHz) mode

EPROM write only mode



GMS34004TM / 34112TM / 34140TM

Mode define

| Item | | Device operation | Mode setting | | |
|-----------------------|-----------------|-----------------------------|-----------------|-----------|--|
| User mode | | Execute User pgm | RESETB = 0 ~ 3V | | Vcc=3V |
| EPROM read mode | | Address in, Data out | RESETB =12.5V | K3-0=0010 | Vcc=6.0V |
| EPROM Program mode | 1Byte PGM Write | Address in, Data in | RESETB =12.5V | K3-0=0110 | Vcc=6.0V |
| | 2Byte PGM Write | Address in, Data in | | K3-0=0111 | |
| | Program verify | Address in, Data out | | - | |
| Lock bit Program mode | Lock bit Write | Lock bit write(set D5 to 1) | RESETB =12.5V | K3-0=0100 | Vcc=6.0V, Lock bit is D5. (Default : unlock) |
| | Lock bit Read | Lock bit out | | K3-0=0101 | |

Port define

| Port Name | User Mode | EPROM Mode | | | |
|-----------|-----------------|--|----|-----|-----|
| VDD | 3.0V | 6.0V | | | |
| RESETB | Reset (0, 3.0V) | Vpp (0, 12.5V) | | | |
| OSC1 | Clock input | Clock input | | | |
| K0 | K0(Input) | Read / Write Control Address / Data Control | | | |
| K1 | K1(Input) | | | | |
| K2 | K2(Input) | | | | |
| K3 | K3(Input) | | | | |
| D0 | D0(Output) | A0 | A5 | Da0 | Da4 |
| D1 | D1(Output) | A1 | A6 | Da1 | Da5 |
| D2 | D2(Output) | A2 | A7 | Da2 | Da6 |
| D3 | D3(Output) | A3 | A8 | Da3 | Da7 |
| D4 | D4(Output) | A4 | A9 | - | - |
| D5 | D5(Output) | Lock bit output | | | |
| GND | 0V | | | | |

NMOS open drain I/O
in EPROM mode

* Undefined ports in this table are N.C (No Connection)

Programming data

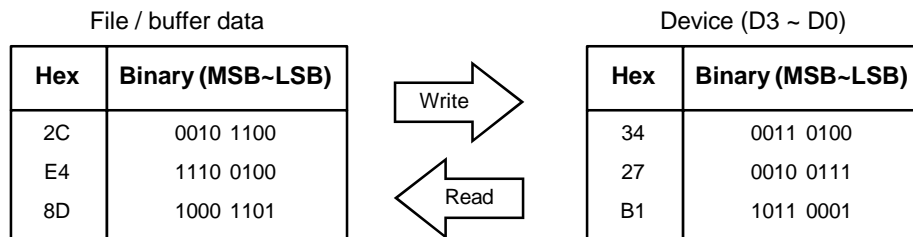
| Device Name | ROM Size | Blank data (HEX) | Lock bit | Device address | File address |
|-------------|------------|------------------|----------|----------------|--------------|
| GMS34004TK | 512bytes | FF | Yes | 0000 ~ 01FF | 0000 ~ 01FF |
| GMS34112TK | 1,024bytes | FF | Yes | 0000 ~ 03FF | 0000 ~ 03FF |
| GMS34140TK | 1,024bytes | FF | Yes | 0000 ~ 03FF | 0000 ~ 03FF |

- If lock bit is set, the EPROM of the device can not be read, because output is always FF.
- Input file : Intel Hexa format (*.RHX)

Chapter 4. EPROM

Write / Read data conversion

- You must change MSB ~ LSB ↔ LSB ~ MSB.
- Example



Checksum

- It is calculated from the Buffer of the programmer.
- Address range is the same as device address.
- Calculate method is the same as normal EPROM devices (ex:27C128, 256 etc)

Programming control

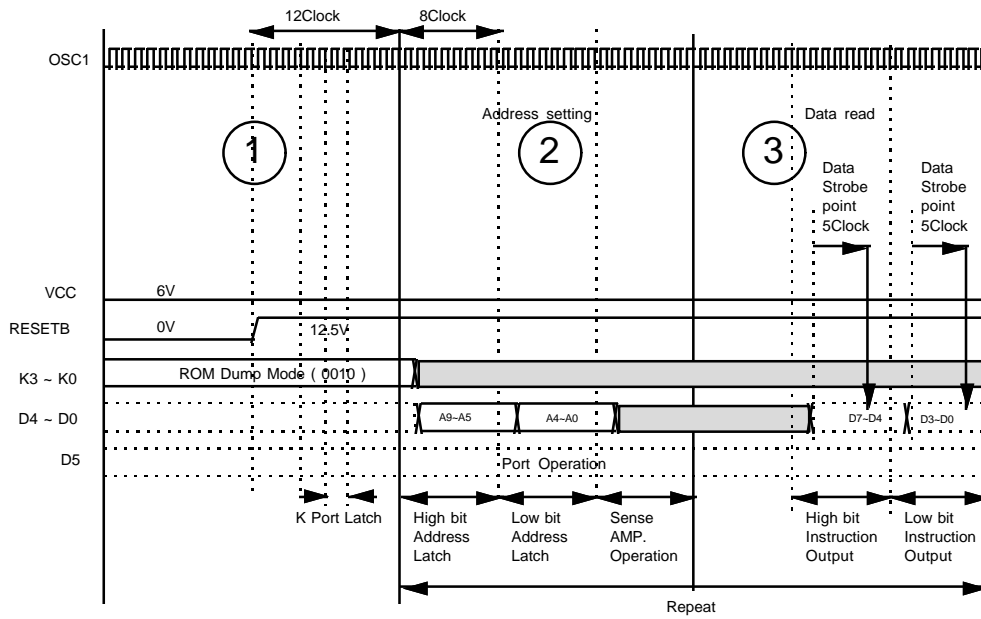
- OSC1 & RESETB control OTP device, so you must count OSC1 clocks in every state.
- K ports control the internal state of the OTP device(ex: Read, Write...).
- D5~D0 ports are NMOS open drain I/O in EPROM mode.
It must be pulled up by resistors (about 4.7~ 47K ohm).
- The frequency rate of the OSC1 clock is 10KHz ~ 500KHz.
You can hold OSC1 HIGH or LOW state when you need.

Programming DC specification

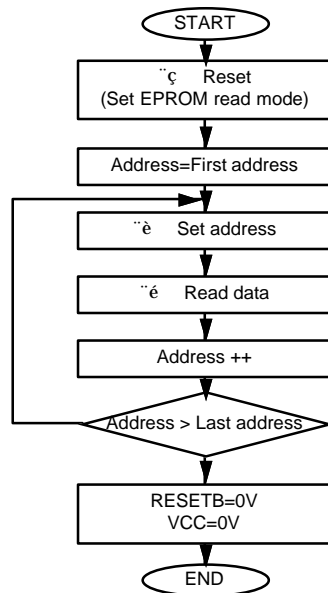
| Item | Range |
|--------|---------------------|
| VCC | 0 ~ 6.0V ±0.25V |
| RESETB | 0 ~ 12.5V ±0.5V |
| K-port | 0 ~ 0.2VCC(Low) |
| D-port | 0.8VCC ~ VCC (High) |

EPROM read mode (1/2)

For device verify or read.
If you set Lock bit, output data is all 'FF'

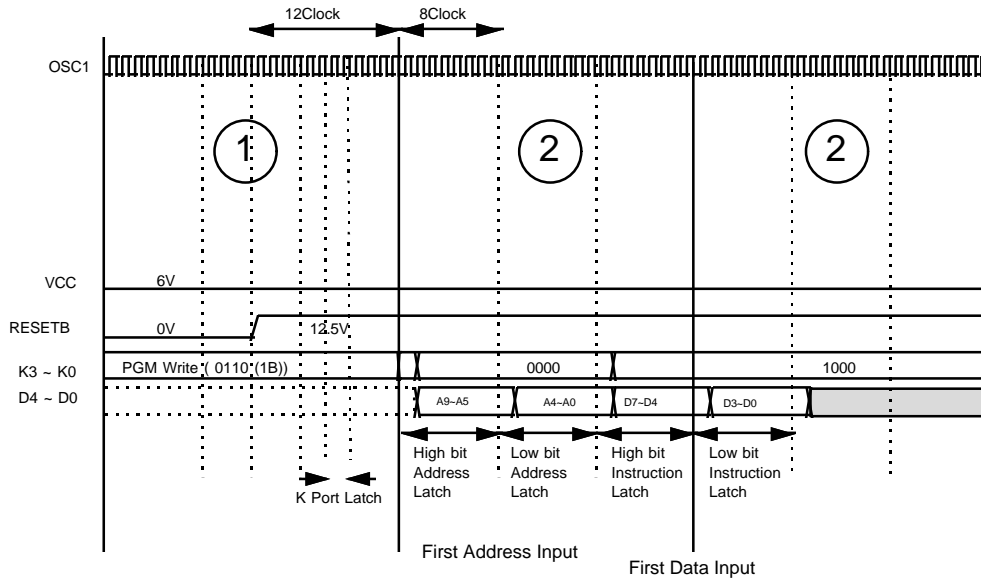


EPROM read mode (2/2)

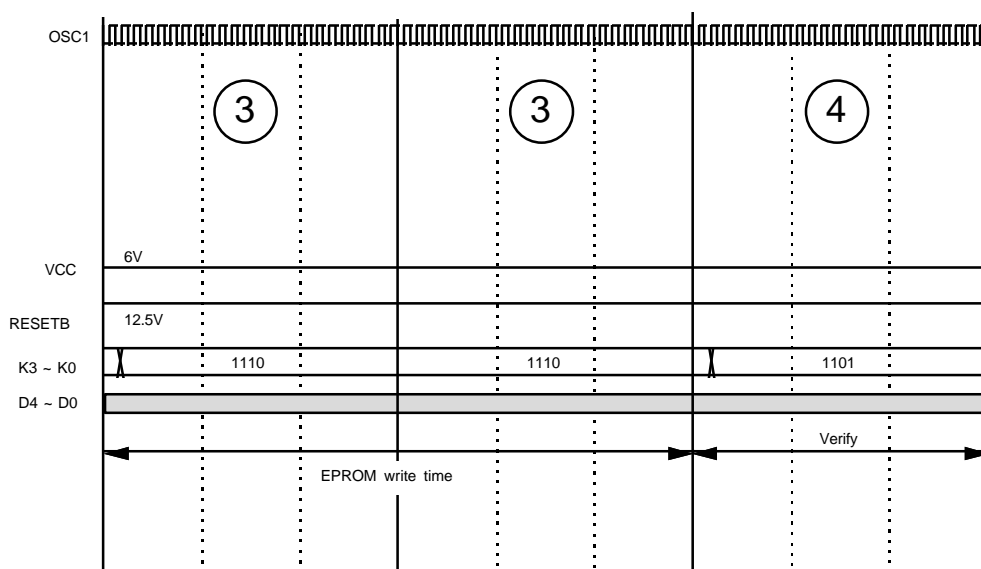


Chapter 4. EPROM

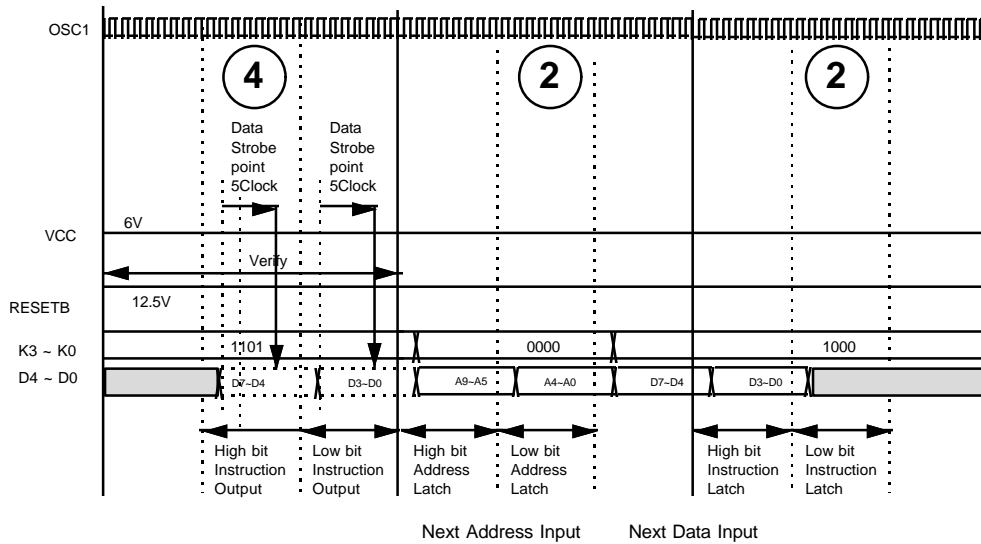
EPROM write mode (1/4)



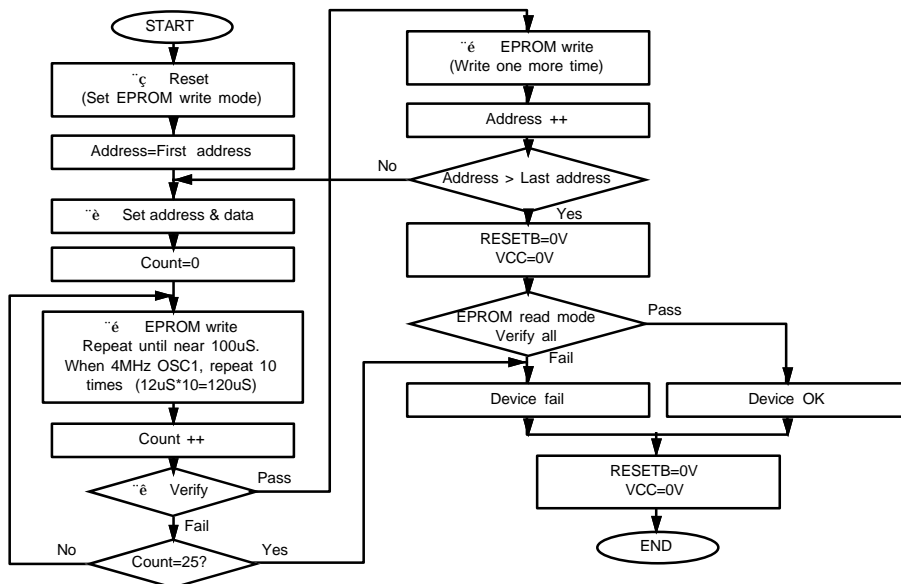
EPROM write mode (2/4)



EPROM write mode (3/4)

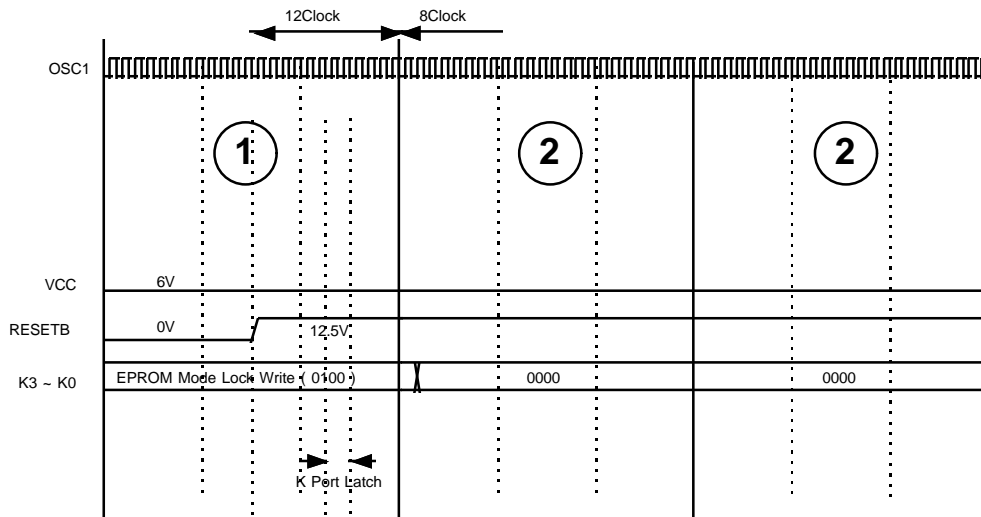


EPROM write mode (4/4)

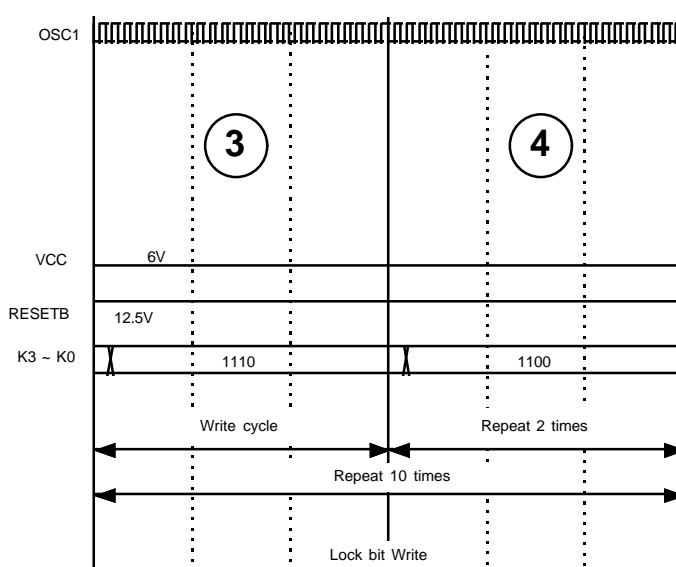


Chapter 4. EPROM

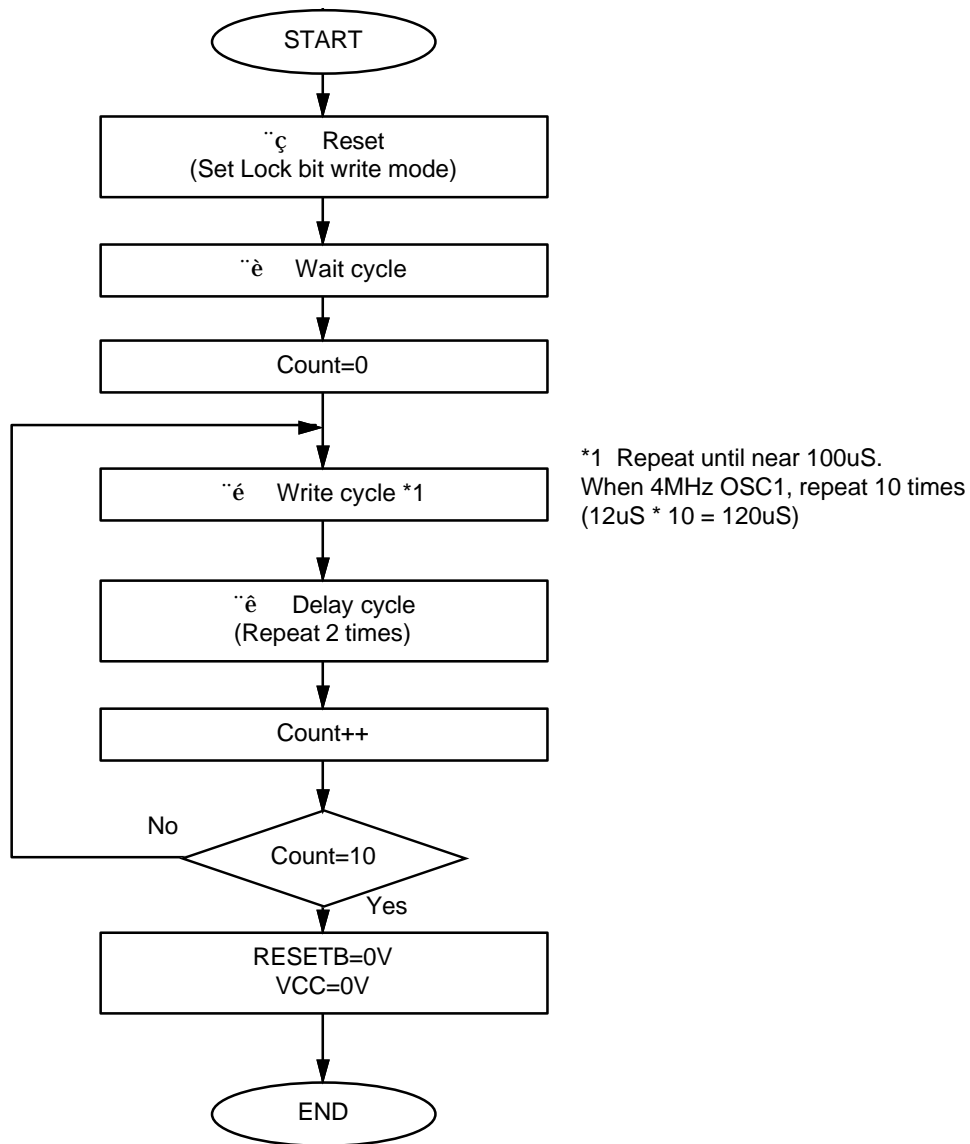
Lock bit write mode (1/3)



Lock bit write mode (2/3)

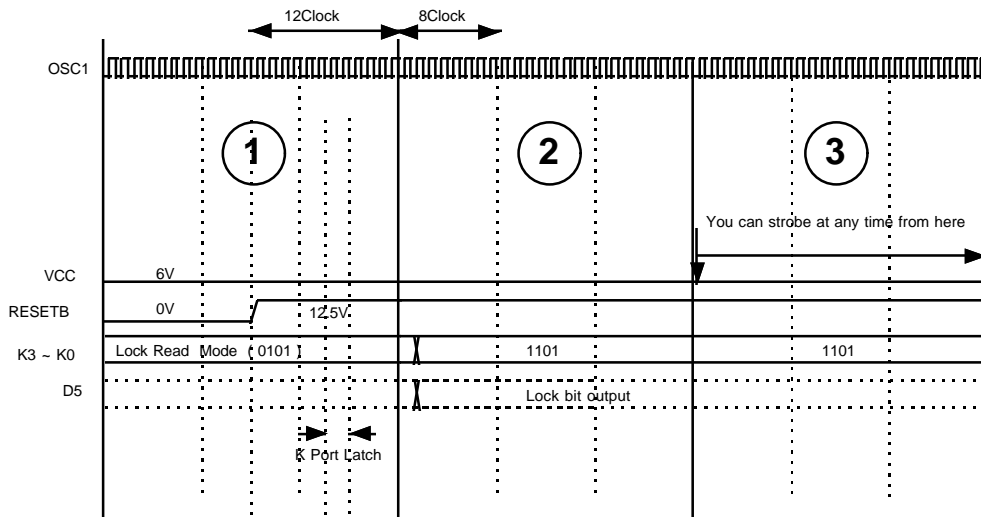


Lock bit write mode (3/3)



Chapter 4. EPROM

Lock bit read mode (1/2)



Lock bit read mode (2/2)

