



FAST CMOS 16-BIT REGISTERED/LATCHED TRANSCEIVER WITH PARITY

IDT54/74FCT162511AT/CT

FEATURES:

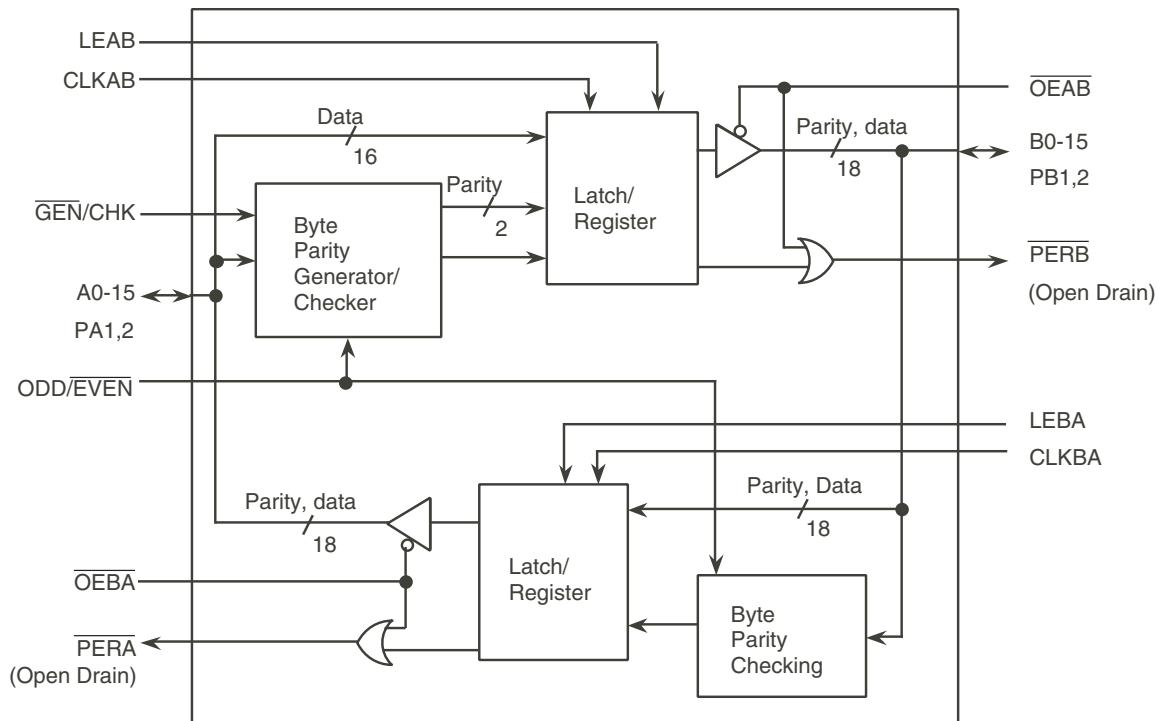
- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps, clocked mode
- Low input and output leakage $\leq 1\mu A$ (max)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 5V \pm 10\%$
- **Balanced Output Drivers:**
 - $\pm 24mA$ (industrial)
 - $\pm 16mA$ (military)
- Series current limiting resistors
- Generate/Check, Check/Check modes
- Open drain parity error allows wire-OR
- Available in the following packages:
 - Industrial: SSOP, TSSOP
 - Military: CERPACK

DESCRIPTION:

The FCT162511T 16-bit registered/latched transceiver with parity is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The device has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. Separate error flag exits for each direction with a single error flag indicating an error for either byte in the A-to-B direction and a second error flag indicating an error for either byte in the B-to-A direction. The parity error flags are open drain outputs which can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. The parity error flags are enabled by the $\overline{OE_{xx}}$ control pins allowing the designer to disable the error flag during combinational transitions.

The control pins LEAB, CLKAB, and \overline{OEAB} control operation in the A-to-B direction while LEBA, CLKBA, and \overline{OEBA} control the B-to-A direction. $\overline{GEN/CHK}$ is only for the selection of A-to-B operation. The B-to-A direction is always in checking mode. The $ODD/EVEN$ select is common between the two directions. Except for the $ODD/EVEN$ control, independent operation can be achieved between the two directions by using the corresponding control lines.

FUNCTIONAL BLOCK DIAGRAM

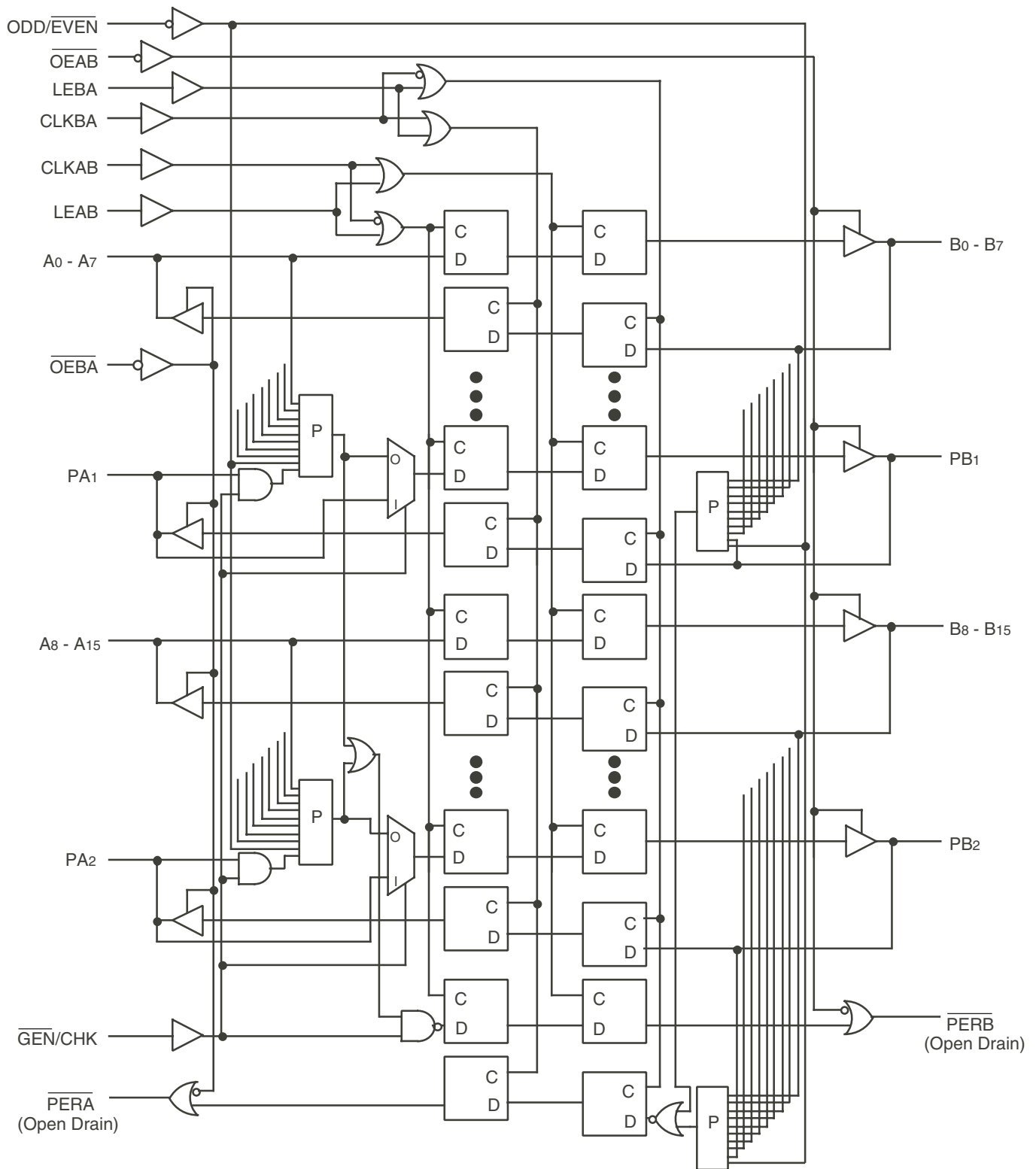


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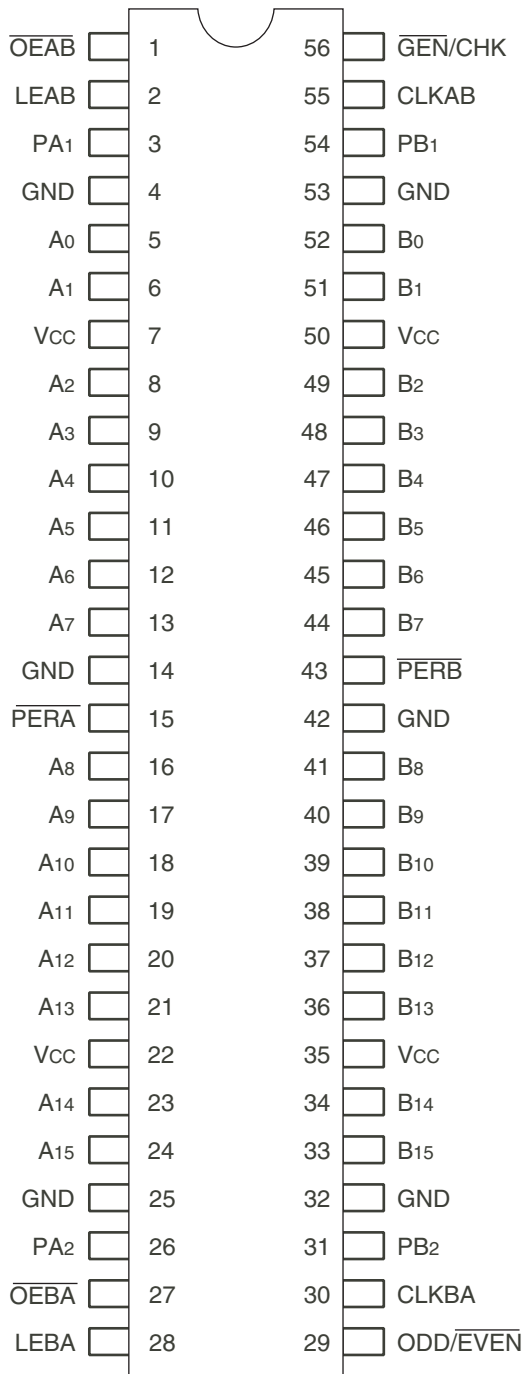
MILITARY AND INDUSTRIAL TEMPERATURE RANGES

SEPTEMBER 2009

BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to 7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Output and I/O terminals for FCT162XXX.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
C _{I/O}	I/O Capacitance	VOUT = 0V	3.5	8	pF
C _O	Open Drain Capacitance	VOUT = 0V	3.5	6	pF

PIN DESCRIPTION

Pin Names	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs
\overline{PERA}	Parity Error (Open Drain) on A Outputs
\overline{PERB}	Parity Error (Open Drain) on B Outputs
PA _x ⁽¹⁾	A-to-B Parity Input, B-to-A Parity Output
PB _x	B-to-A Parity Input, A-to-B Parity Output
ODD/ \overline{EVEN}	Parity Mode Selection Input
$\overline{GEN/CHK}$	A to B Port Generate or Check Mode Input

NOTE:

- The PA_x pin input is internally disabled during parity generation. This means that when generating parity in the A to B direction there is no need to add a pull up resistor to guarantee state. The pin will still function properly as the parity output for the B to A direction.

FUNCTION TABLE (1, 4)

Inputs				Outputs
\overline{OEAB}	LEAB	CLKAB	Ax	Bx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B ⁽²⁾
L	L	H	X	B ⁽³⁾

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-impedance
↑ = LOW-to-HIGH Transition

FUNCTION TABLE (PARITY CHECKING) (1, 2, 3, 4)

A0 – A7 and PA1 ⁽⁵⁾ Number of inputs that are high	ODD/ \overline{EVEN}	\overline{PERB}
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H ⁽⁶⁾
0, 2, 4, 6 or 8	L	H ⁽⁶⁾
0, 2, 4, 6 or 8	H	L

NOTES:

1. Conditions shown are for $\overline{GEN}/CHK = H$, $\overline{OEAB} = L$, $\overline{OEBA} = H$.
2. A-to-B parity checking is shown. B-to-A parity checking is similar but uses $\overline{OEBA} = L$, $\overline{OEAB} = H$ and errors will be indicated on \overline{PERA} .
3. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors (PB1 = PA1).
4. The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
5. Conditions shown are for the byte A0–A7 and PA1. The byte A8–A15 and PA2 is similar.
6. The parity error flag \overline{PERB} is a combined flag for both bytes A0–A7 and A8–A15. If a parity error occurs on either byte \overline{PERB} will go low. \overline{PERB} is an open drain output which must be externally pulled up to achieve a logic HIGH.

FUNCTION TABLE (PARITY GENERATION) (1, 2, 3, 4, 5)

A0 – A7 Number of inputs that are high	ODD/ \overline{EVEN}	PB1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

1. Conditions shown are for $\overline{GEN}/CHK = L$, $\overline{OEAB} = L$, $\overline{OEBA} = H$.
2. A-to-B parity checking is shown. B-to-A is capable of parity checking while A-to-B is performing generation. B-to-A will not generate parity.
3. The response shown is for LEAB = H. If LEAB = L then CLKAB will control as an edge triggered clock.
4. Conditions shown are for the byte A–A7. The byte A8–A15 is similar but will output the parity on PB2.
5. The error flag \overline{PERB} will remain in a high state during parity generation.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	All other Input Pins	—	0.5	1.5	mA
			Parity Input Pins (PAX, PBx)	—	1	2.5	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OEAB} = \text{GND}, \overline{OEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu\text{A}/\text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz (CLKAB)}$ 50% Duty Cycle $\overline{OEAB} = \text{GND}, \overline{OEBA} = V_{CC}$ LEAB = GND One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾		
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	9	21.8 ⁽⁵⁾		

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (PROPAGATION DELAYS)

Symbol	Parameter	Condition ⁽¹⁾	FCT162511AT				FCT162511CT				Unit
			Ind.		Mil.		Ind.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay, P _{Ax} to P _{Bx} A _x to B _x or B _x to A _x , P _{Bx} to P _{Ax}	CL = 50pF RL = 500Ω	1.5	5	1.5	5.3	1.5	4.2	1.5	4.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _x to P _{Bx} $\overline{\text{GEN/CHK}} \text{ LOW}$		1.5	7.5	1.5	8	1.5	6.5	1.5	6.8	ns
t _{PLH} ⁽³⁾ t _{PHL}	Propagation Delay A _x to P _{ERB} , P _{Ax} to $\overline{\text{PERB}}$		1.5	9	1.5	9	1.5	7.5	1.5	7.8	ns
t _{PLH} ⁽³⁾ t _{PHL}	Propagation Delay B _x to P _{ERA} , P _{Bx} to $\overline{\text{PERA}}$		1.5	8	1.5	8	1.5	6.5	1.5	6.8	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _x and P _{Ax} LEAB to B _x and P _{Bx}		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
t _{PLH} ⁽³⁾ t _{PHL}	Propagation Delay LEBA to $\overline{\text{PERA}}$, LEAB to $\overline{\text{PERB}}$		1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to A _x and P _{Ax} CLKAB to B _x and P _{Bx}		1.5	5.6	1.5	6	1.5	5.3	1.5	5.5	ns
t _{PLH} ⁽³⁾ t _{PHL}	Propagation Delay CLKBA to $\overline{\text{PERA}}$ CLKAB to $\overline{\text{PERB}}$		1.5	7	1.5	7	1.5	6	1.5	6.3	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to $\overline{\text{PERA}}$ CLKAB to $\overline{\text{PERB}}$		1.5	6	1.5	6	1.5	5	1.5	5.3	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OEBA}}$ to A _x and P _{Ax} $\overline{\text{OEAB}}$ to B _x and P _{Bx}		1.5	6	1.5	6.5	1.5	5.6	1.5	5.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OEBA}}$ to A _x and P _{Ax} $\overline{\text{OEAB}}$ to B _x and P _{Bx}		1.5	5.6	1.5	6	1.5	5.2	1.5	5.5	ns
t _{PLZ} ⁽³⁾ t _{PZL}	Parity ERROR Enable $\overline{\text{OEBA}}$ to P _{ERA} , $\overline{\text{OEAB}}$ to $\overline{\text{PERB}}$		1.5	6	1.5	6.3	1.5	6	1.5	6.3	ns
t _{PLH} ⁽³⁾ t _{PHL}	ODD/ $\overline{\text{EVEN}}$ to P _{ERx}		1.5	10	1.5	10	1.5	10	1.5	10	ns
t _{PLH} t _{PHL}	ODD/ $\overline{\text{EVEN}}$ to P _{Bx}		1.5	10	1.5	10	1.5	10	1.5	10	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On Open Drain Outputs t_{PLH} is measured at V_{OUT} = V_{OL} + 0.3V.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (SET UP TIMES)

Symbol	Parameter	Test Conditions ^(1, 3)		CL = 50pF RL = 500Ω	FCT162511AT		FCT162511CT		Unit			
					Ind.		Mil.					
					Min.	Max.	Min.	Max.				
tsu	Set-up Time HIGH or LOW Ax to CLKAB	$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx valid	4	—	4	—	3	—	3.5	—	ns
			PBx not valid	3	—	3	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ valid	4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
tsu	Set-up Time PAx to CLKAB	$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ valid	4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
tsu	Set-up Time Bx to CLKBA, PBx to CLKBA		$\overline{\text{PERA}}$ valid	4	—	4	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid	3	—	4	—	3	—	3	—	ns
tsu	Set-up Time Ax to LEAB	CLKAB LOW	PBx valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx not valid	3	—	3	—	3	—	3	—	ns
		CLKAB LOW	$\overline{\text{PERB}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	PBx valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ LOW	PBx not valid	3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{\text{PERB}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
tsu	Set-up Time PAx to LEAB	CLKAB LOW	$\overline{\text{PERB}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
		CLKAB HIGH	$\overline{\text{PERB}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK}$ HIGH	$\overline{\text{PERB}}$ not valid	3	—	3	—	3	—	3	—	ns
tsu	Set-up Time Bx to LEBA PBx to LEBA	CLKBA LOW	$\overline{\text{PERA}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid	3	—	3	—	3	—	3	—	ns
		CLKBA HIGH	$\overline{\text{PERA}}$ valid	3.5	—	3.5	—	3	—	3	—	ns
			$\overline{\text{PERA}}$ not valid	3	—	3	—	3	—	3	—	ns
tsk(O)	Output Skew ⁽⁴⁾			—	0.5	—	0.5	—	0.5	—	0.5	ns

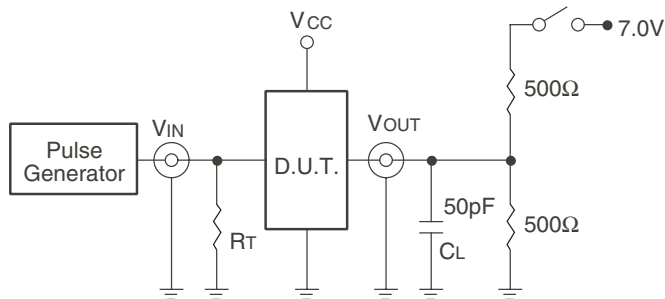
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (HOLD TIMES)

Symbol	Parameter	Condition ⁽¹⁾	FCT162511AT		FCT162511CT		Unit			
			Ind.		Mil.					
			Min.	Max.	Min.	Max.				
th	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	CL = 50pF RL = 500Ω	1	—	1	—	1	—	ns	
th	Hold Time HIGH or LOW PAx to LEAB		1	—	1	—	1	—	ns	
th	Hold Time HIGH or LOW PBx to LEBA		1	—	1	—	1	—	ns	
th	Hold Time Ax to CLKAB, PAx to CLKAB		1	—	1	—	0	—	0	ns
th	Hold Time Bx to CLKBA, PBx to CLKBA		1	—	1	—	0	—	0	ns
tw	LEAB or LEBA Pulse Width HIGH ⁽²⁾		3	—	3	—	3	—	3	ns
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽²⁾		3	—	3	—	3	—	3	ns

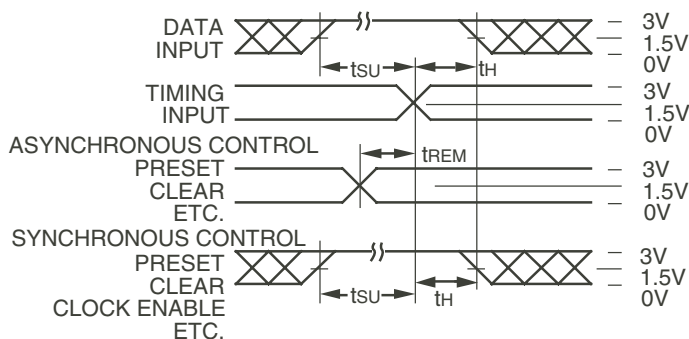
NOTES:

- See test circuits and waveforms.
- This parameter is guaranteed but not tested.
- "Not valid" means the set-up time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A to B or B to A port respective to the indicated direction.
- Skew between any two outputs of the same package, switching in the same direction, excluding $\overline{\text{PERx}}$ in clocked mode, and $\overline{\text{Pxx}}$ (parity bits) and $\overline{\text{PERx}}$ in transparent/latched mode. This parameter is guaranteed by design.

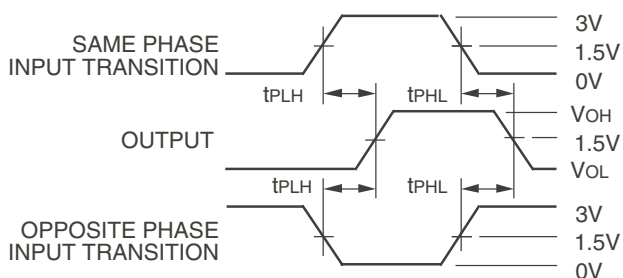
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-up, Hold, and Release Times



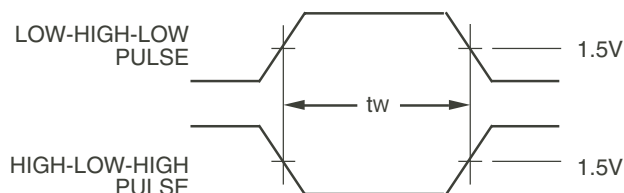
Propagation Delay

SWITCH POSITION

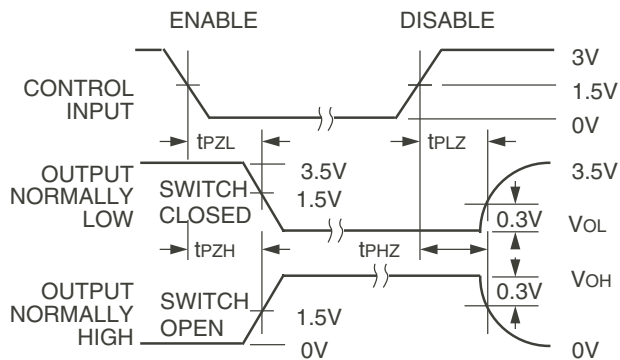
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



Pulse Width

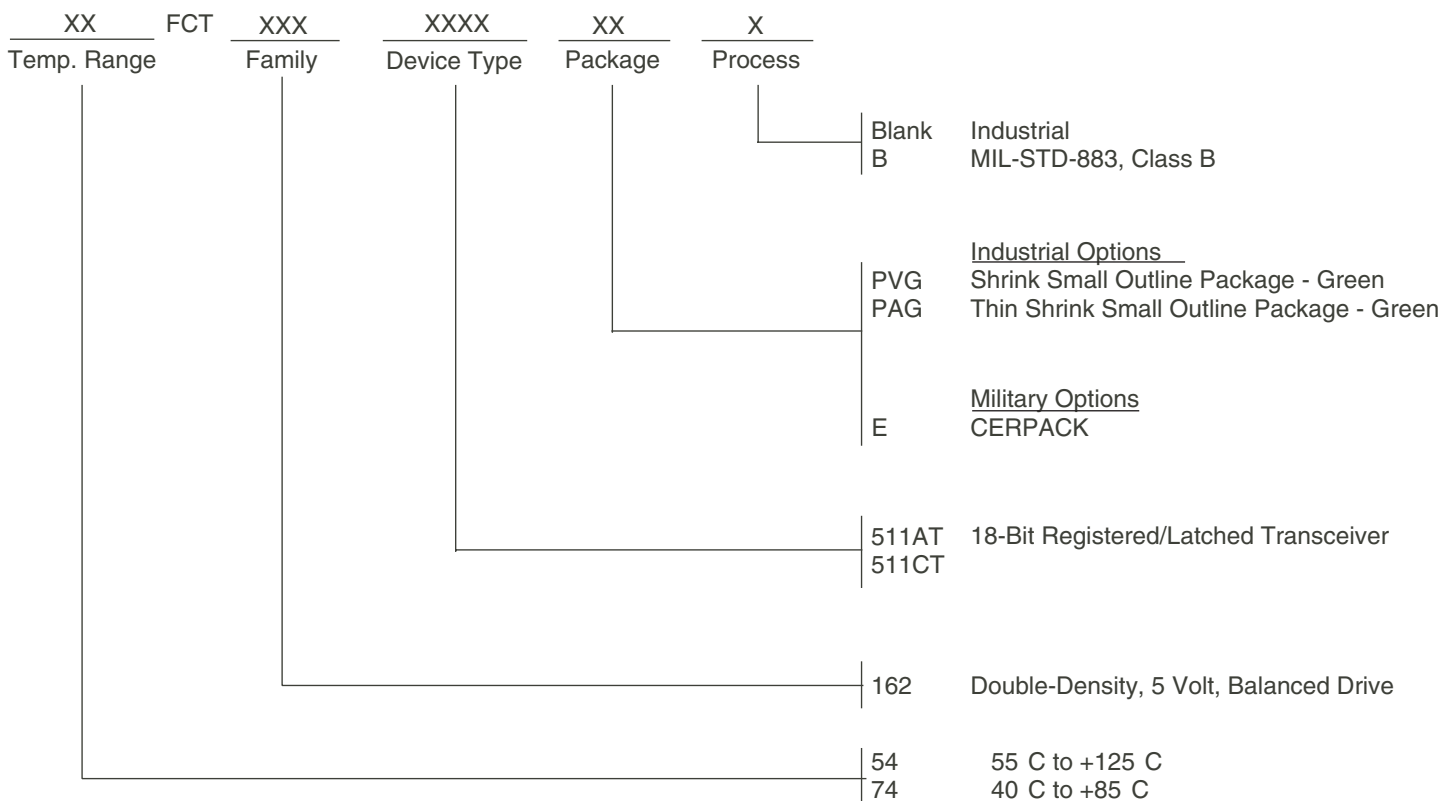


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



Datasheet Document History

09/06/09 Pg.6 Updated the ordering information by removing the "IDT" notation and non RoHS part.



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 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
 www.idt.com

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 logichelp@idt.com