

# FDZ3N513ZT

## Integrated NMOS and Schottky Diode

### Features

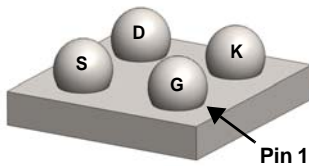
- Monolithic NMOS and Schottky Diode
- Ultra-small form factor 1mm x 1mm WLCSP
- Max  $r_{DS(on)}$  = 462 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 0.3$  A
- Max  $r_{DS(on)}$  = 520 mΩ at  $V_{GS} = 3.2$  V,  $I_D = 0.3$  A
- HBM ESD protection level > 2000V (Note3)
- RoHS Compliant

### General Description

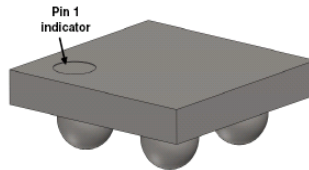
The FDZ3N513ZT is a monolithic NMOS/ Schottky combination (FETky) and is designed and wired to function as a discontinuous conduction mode (DCM) boost LED power train for mobile LED backlighting applications.

### Application

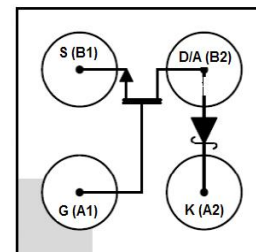
- Boost Converter Power Train for single cell Li-ion LED backlighting



WL-CSP 3D Bumps Facing Up View



WL-CSP 3D Bumps Facing Down View



WL-CSP 1.0X1.0 Bumps Facing Up View

### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
$V_{DS}$	NMOS Drain to Source Voltage	30	V
$V_{GS}$	NMOS Gate to Source Voltage	-0.3/5.5	V
$P_D$	Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1a)	1	W
$I_D$	Maximum Continuous NMOS Drain Current (Note 1a)	1.1	A
$V_{RRM}$	Schottky Repetitive Peak Reverse Voltage	25	V
$I_O$	Schottky Average Forward Current	0.3	A
$T_J, T_{STG}$	Operating Junction and Storage Temperature	-55/125	$^\circ\text{C}$
ESD	Electrostatic Discharge Protection	CDM 2000	V

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient - 1in <sup>2</sup> , 2oz. Copper (Note 1a)	100	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient - Minimum Pad (Note 1b)	260	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Part Number	Device Marking	Package	Reel Size	Tape Width	Quantity
FDZ3N513ZT	Z3	WL-CSP 1.0X1.0	7"	8mm	5000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		47		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = +5\text{ V}/-0.3\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	0.5	0.7	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-1.6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 0.3\text{ A}$ $V_{GS} = 3.2\text{ V}$ , $I_D = 0.3\text{ A}$		384 410	462 520	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 0.3\text{ A}$		0.5		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		45	85	pF
$C_{oss}$	Output Capacitance			45	85	pF
$C_{rss}$	Reverse Transfer Capacitance			10	25	pF
$R_g$	Gate Resistance			2.0		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 0.3\text{ A}$ $V_{GS} = 5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		3.1	10	ns
$t_r$	Rise Time			1.9	10	ns
$t_{d(off)}$	Turn-Off Delay Time			9.6	20	ns
$t_f$	Fall Time			2.7	10	ns
$Q_g$	Total Gate Charge ( $V_{GS} = 4.5\text{ V}$ )		$V_{DD} = 15\text{ V}$ $I_D = 0.3\text{ A}$		1.0	
$Q_{gs}$	Gate to Source Gate Charge			0.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.3		nC

### Drain-Source Diode Characteristics

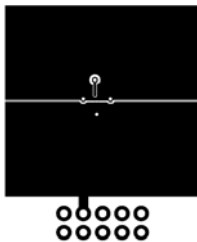
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 0.3\text{ A}$ (Note 2)		0.75	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 0.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		16	29	ns
$Q_{rr}$	Reverse Recovery Charge			6.0	10	nC

### Schottky Diode Characteristics

$I_R$	Reverse Leakage	$V_R = 20\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		15	30	$\mu\text{A}$
			$T_J = 85\text{ }^\circ\text{C}$		300		$\mu\text{A}$
$V_F$	Forward Voltage	$I_F = 300\text{ mA}$	$T_J = 25\text{ }^\circ\text{C}$		0.72	1.2	V
			$T_J = 85\text{ }^\circ\text{C}$		0.74		

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a. 100  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 260  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

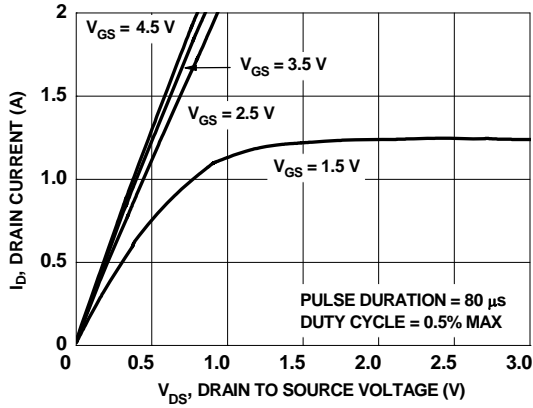


Figure 1. On Region Characteristics

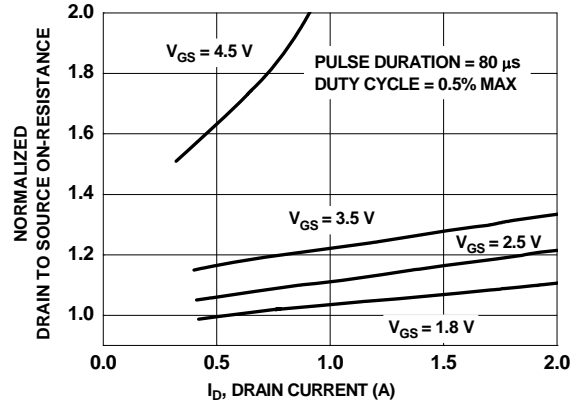


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

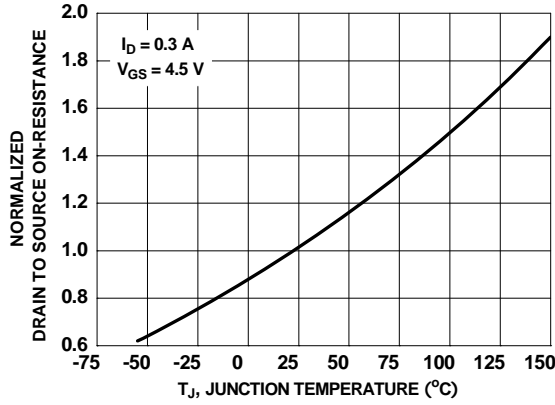


Figure 3. Normalized On Resistance vs Junction Temperature

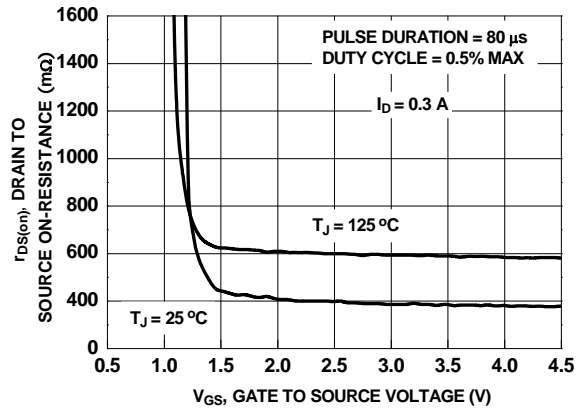


Figure 4. On-Resistance vs Gate to Source Voltage

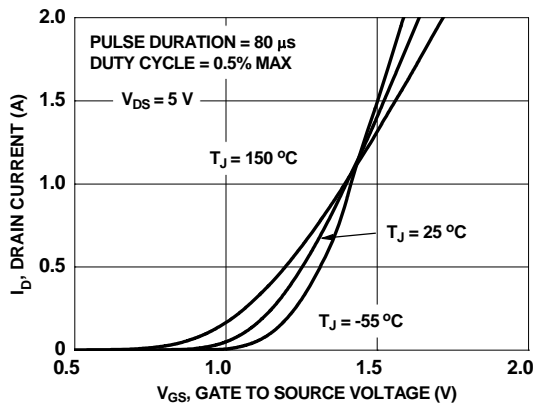


Figure 5. Transfer Characteristics

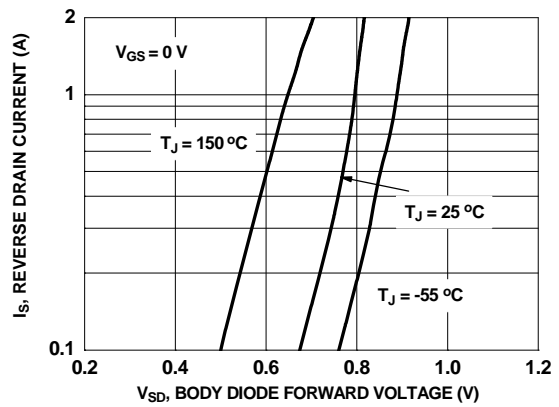
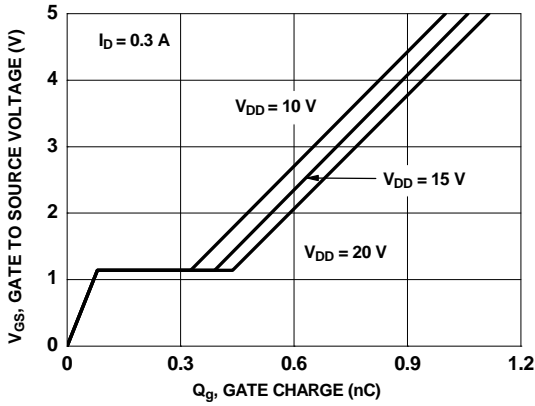
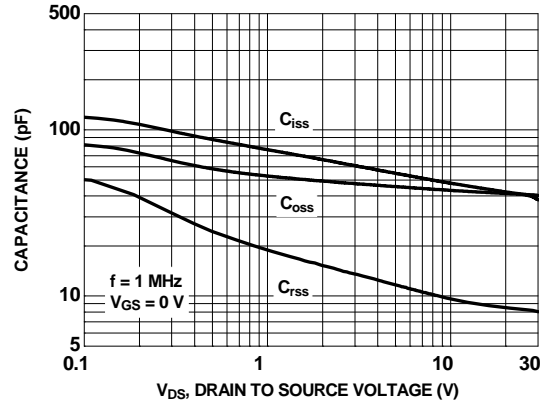


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

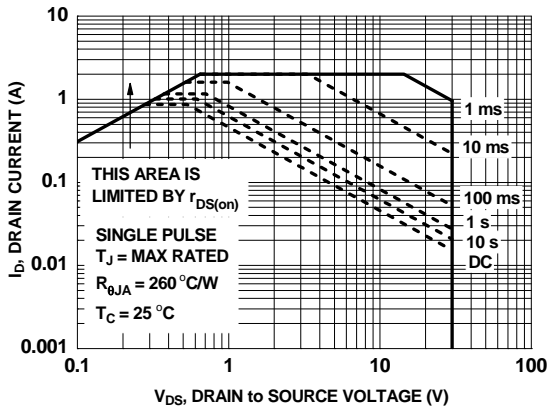
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



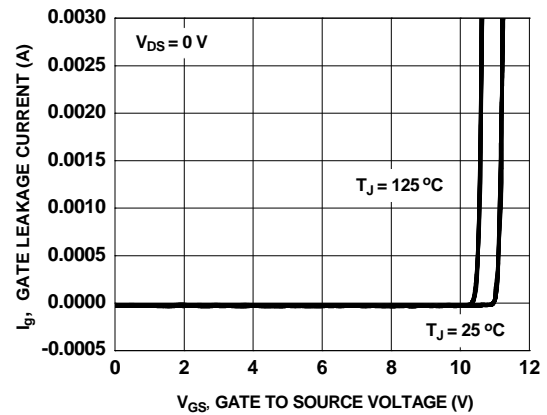
**Figure 7. Gate Charge Characteristics**



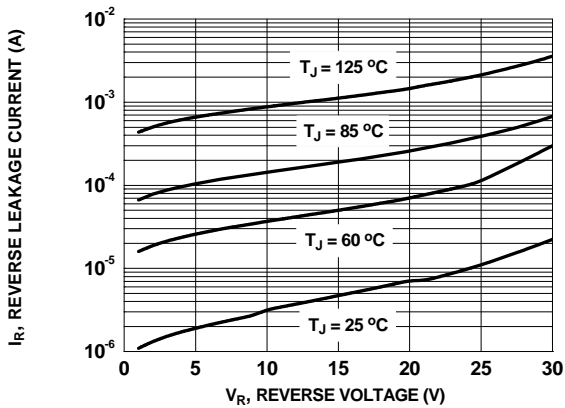
**Figure 8. Capacitance vs Drain to Source Voltage**



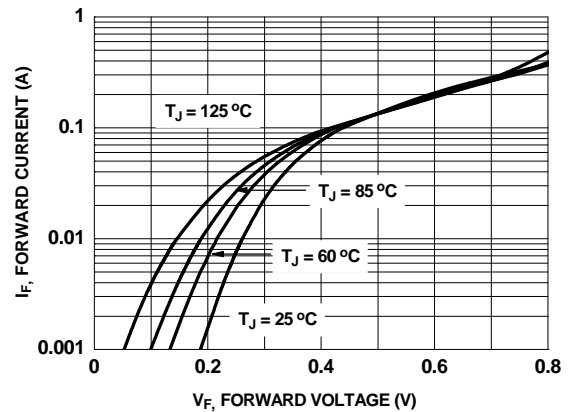
**Figure 9. Forward Bias Safe Operating Area**



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

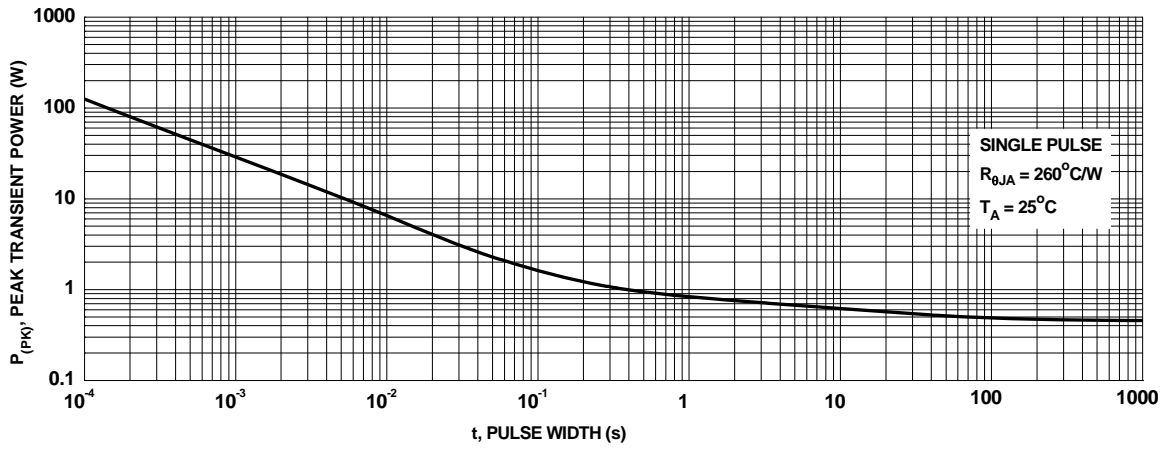


**Figure 11. Schottky Diode Reverse Current**

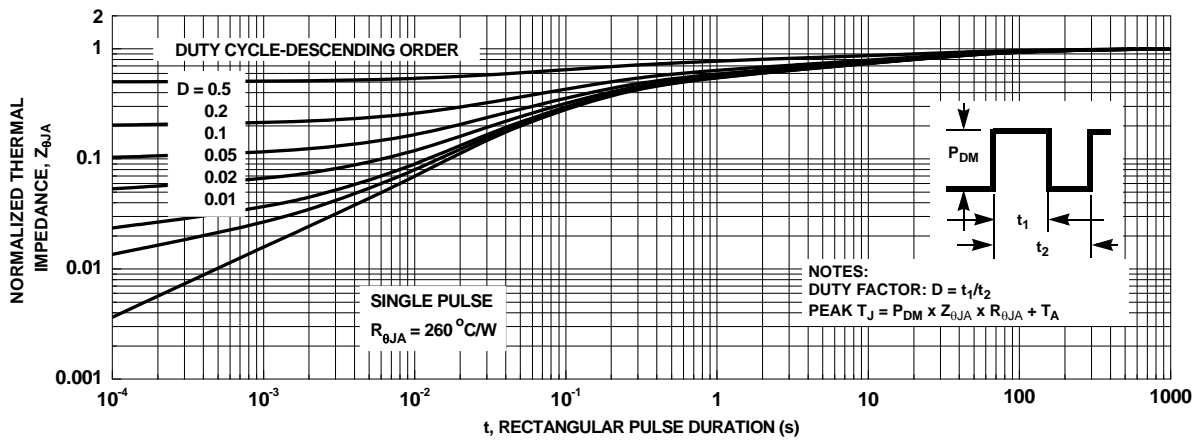


**Figure 12. Schottky Diode Forward Voltage**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

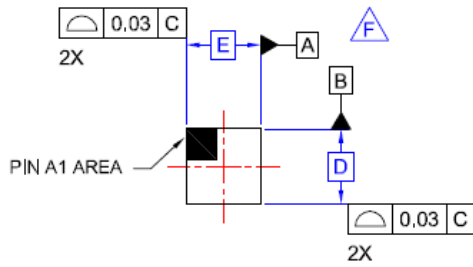


**Figure 13. Single Pulse Maximum Power Dissipation**

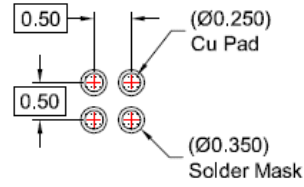


**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

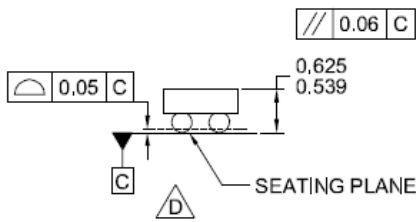
## Dimensional Outline and Pad Layout



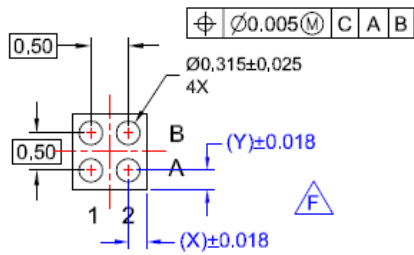
TOP VIEW



RECOMMENDED LAND PATTERN  
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

### NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D.** DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).
- F.** FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.






### Product Specific Dimensions

Product	D	E	X	Y
FDZ3N513ZTUCX	1.000 +/-0.030	1.000 +/-0.030	0.018	0.018



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| FETBench™   |  ™ | SyncFET™  |   |
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| FPS™  | PDP SPM™  |   |   |

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**Definition of Terms**

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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