

OKI Semiconductor MR27V3252J

Oki, Network Solutions for a Global Society

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2M–Word \times 16–Bit or 4M–Word \times 8–Bit Page Mode OTP

GENERAL DESCRIPTION

The MR27V3252J is a 32 Mbit electrically One Time Programmable Read-Only Memory with page mode. Its configuration can be electrically switched between 2,097,152-word × 16-bit and 4,194,304-word × 8-bit by the state of the BYTE# pin. The MR27V3252J supports high speed asynchronous read operation using a single 3.3V power supply.

FEATURES

 \cdot 2,097,152-word \times 16-bit / 4,194,304-word \times 8-bit electrically switchable configuration

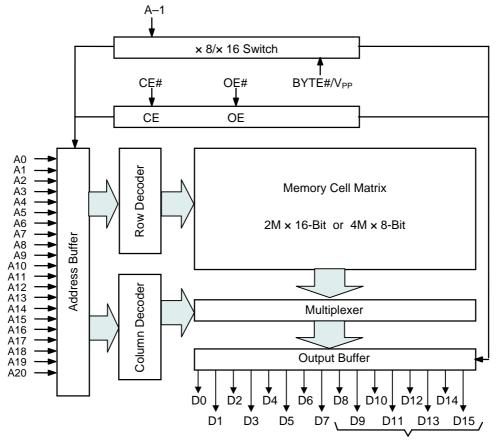
- Page size of 8-word x 16-Bit or 16-word x 8-Bit
- \cdot 3.0 V to 3.6 V power supply
- Random Access time 70 ns MAX
- Page Access time 25 ns MAX
- Operating current 50 mA MAX
- \cdot Standby current 10 μ A MAX
- · Input/Output TTL compatible
- \cdot Three-state output

PACKAGES

•MR27V3252JTN 48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

PIN CONF	[GU]	RATION	N (TOP VIEW)
		<u></u>	_
A15 1	\bigcirc	>>	48 A16
A14 2	Ŭ		47 BYTE#/V _{PP}
A13 3			46 V _{SS}
A12 4 A11 5			45 D15/A-1 44 D7
A10 6			43 D14
A9 7			42 D6
A8 8			41 D13
A19 9			40 D5
A20 10			39 D12
NC 11 NC 12			38 D4 37 V _{CC}
NC 13			36 D11
NC 14			35 D3
NC 15			34 D10
A18 16			33 D2
A17 17 A7 18			32 D9 31 D1
A6 19			30 D8
A5 20			29 D0
A4 21			28 OE#
A3 22			27 V _{SS}
A2 23 A1 24			26 CE# 25 A0
AT 24		- \$\$	25 40
		TYPE I	

BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions					
D15 / A–1	Data output / Address input					
A0 to A20	Address inputs					
D0 to D14	Data outputs					
CE#	Chip enable input					
OE#	Output enable input					
BYTE#/V _{PP}	Mode switch/Program power supply voltage					
Vcc	Power supply voltage					
V _{SS}	Ground					
NC	No connect					

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A–1				
Read (16-Bit)	L	L	Н		D _{оит}						
Read (8-Bit)	L	L	L		D _{OUT}	Hi–Z	L/H				
Output disable		Ц	н	221		Hi–Z					
Output disable	L	Н	L	3.3 V		*					
Oton dhu			н			11: 7					
Standby	Н	*	L			Hi–Z					
Program	L	Н			D _{IN}						
Program inhibit	Н	Н	V _{PP}	Vcc	Hi–Z						
Program verify	Н	L			D _{OUT}						

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	—	-55 to 125	°C
Input voltage	VI		–0.5 to V _{CC} +0.5	V
Output voltage	Vo	relative to V	–0.5 to V _{CC} +0.5	V
Power supply voltage	Vcc	relative to V _{SS}	–0.5 to 5	V
Program power supply voltage	V _{PP}		-0.5 to 11.5	V
Power dissipation per package	PD	Ta = 25°C	1.0	W
Output short circuit current	I _{OS}	_	10	mA

RECOMMENDED OPERATING CONDITIONS

					(Ta	= 0 to 70°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V _{CC} power supply voltage	V _{cc}		3.0	_	3.6	V
V _{PP} power supply voltage	V _{PP}	$\lambda = 2.0 \text{ to } 2.6 \lambda$	-0.5		V _{CC} +0.5	V
Input "H" level	V _{IH}	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$	2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C _{IN1}	$V_1 = 0 V$	—	—	8	
BYTE#/V _{PP}	C _{IN2}	$v_1 = 0 v$	_	_	200	pF
Output	COUT	$V_0 = 0 V$	—	_	10	

ELECTRICAL CHARACTERISTICS

DC Characteristics

			(\	/ _{CC} = 3.0 V	to 3.6 V, Ta	= 0 to 70°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_1 = 0$ to V_{CC}	—	—	5	μA
Output leakage current	I _{LO}	$V_{O} = 0$ to V_{CC}	—	—	5	μA
V _{CC} power supply current	Iccsc	$CE\# = V_{CC}$	—	—	10	μA
(Standby)	I _{CCST}	$CE\# = V_{IH}$	—	—	1	mA
V _{CC} power supply current (Read)	I _{CCA1}	OE# = V _{IH,} f = 10MHz	—	—	50	mA
V _{PP} power supply current	I _{PP}	$V_{PP} = V_{CC}$	—	—	10	μA
Input "H" level	VIH	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	VIL	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{ОН} = —1 mA	2.4	_	_	V
Output "L" level	V _{OL}	$I_{OL} = 2 \text{ mA}$		_	0.4	V

Voltage is relative to V_{SS}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

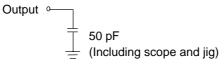
AC Characteristics

			(vcc =	3.0 V 10 3.6 V, Ta	= 0 (0 70 C)
Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	70	—	ns
Address access time	t _{ACC}	$CE\# = OE\# = V_{IL}$		70	ns
Page cycle time	t _{PC}	—	25	—	ns
Page access time	t _{PAC}	—		25	ns
CE# access time	t _{CE}	$OE\# = V_{IL}$		70	ns
OE# access time	t _{OE}	$CE\# = V_{IL}$		25	ns
Output disable time	t _{CHZ}	$OE\# = V_{IL}$	0	20	ns
Output disable time	t _{OHZ}	$CE\# = V_{IL}$	0	20	ns
Output hold time	t _{он}	$CE\# = OE\# = V_{IL}$	0		ns

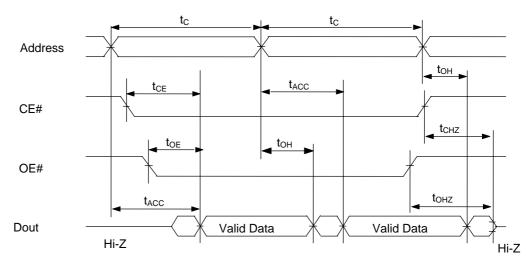
(V_{CC} = 3.0 V to 3.6 V, Ta = 0 to 70°C)

Measurement conditions

Output load

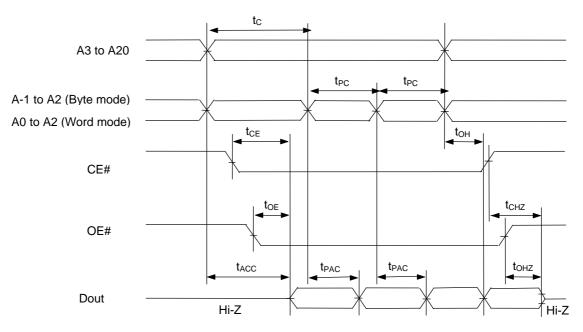


TIMING CHART (READ CYCLE)



Random Access Mode Read Cycle

Page Access Mode Read Cycle



ELECTRICAL CHARACTERISTICS (PROGRAMMING OPERATION)

DC CHARACTERISTICS

					(Ta = 2	5°C ± 5°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = V_{CC}$ +0.5 V	—		10	μA
V _{PP} power supply current (Program)	I _{PP2}	$CE\# = V_{IL}$	—		50	mA
V _{CC} power supply current	Icc	—	—		50	mA
Input "H" level	V _{IH}	—	V _{CC} -0.5		V _{CC} +0.5	V
Input "L" level	VIL	—	-0.5		0.8	V
Output "H" level	V _{OH}	I _{OH} = -400 μA	2.4		—	V
Output "L" level	V _{OL}	I _{OL} = 2.1 mA	—		0.45	V
Program voltage	V_{PP}	_	8.0	8.2	8.4	V
V _{CC} power supply voltage	V _{CC}		3.9	4.0	4.1	V

Voltage is relative to V_{SS}.

AC CHARACTERISTICS

	$(V_{CC} = 4.0 \text{ V} \pm 0.1 \text{ V}, \text{BYTE} \# / V_{PP} = 8.2 \text{ V} \pm 0.25 \text{ V}, \text{Ta} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C})$									
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit				
Address set-up time	t _{AS}	—	100	_	—	ns				
OE# set-up time	t _{OES}	—	2	_	—	μS				
Data set-up time	t _{DS}	—	100	_	—	ns				
Address hold time	t _{AH}	_	2	_	—	μS				
Data hold time	t _{DH}	—	100	—	—	ns				
Output float delay time from OE#	t _{OHZ}	—	0	_	100	ns				
V _{PP} voltage set-up time	t _{VS}	_	2	_	—	μS				
Program pulse width	t _{PW}	—	7	8	9	μS				
Data valid from OE#	t _{OE}	—		_	100	ns				
Address hold from OE# high	t _{AOH}	_	0	_	—	ns				

Pin Check Function

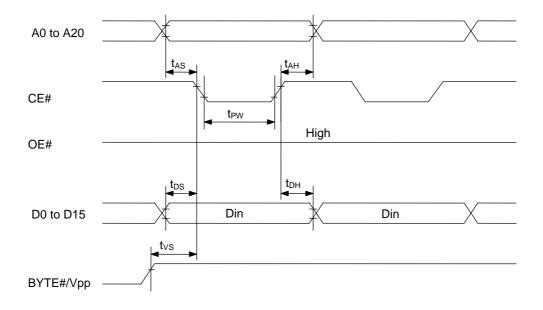
Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer. Setting up address as following condition call the preprogrammed codes on device outputs.

							(- 00				,		, -					11	- 11 13		
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	DATA
0	1	0	1	0	1	0	1	0	VH	0	1	0	1	0	1	0	0	1	1	0	FF00
1	0	1	0	1	0	1	0	1	VH	1	0	1	0	1	0	1	1	0	0	1	00FF
	Other conditions									FFFF											

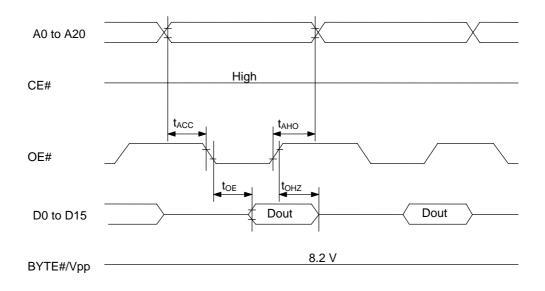
 $(V_{CC} = 3.0 \text{ V} \pm 0.1 \text{ V}, CE\# = \text{VIL}, OE\# = \text{VIL}, BYTE\#/V_{PP} = V_{IH}, Ta = 25^{\circ}C \pm 5^{\circ}C)$

*: VH = 7 V ± 0.25 V

Consecutive Programming Waveforms



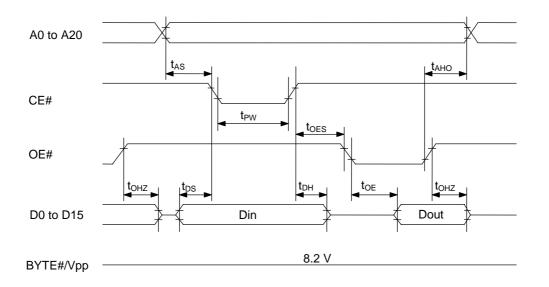
Consecutive Program Verify Waveforms



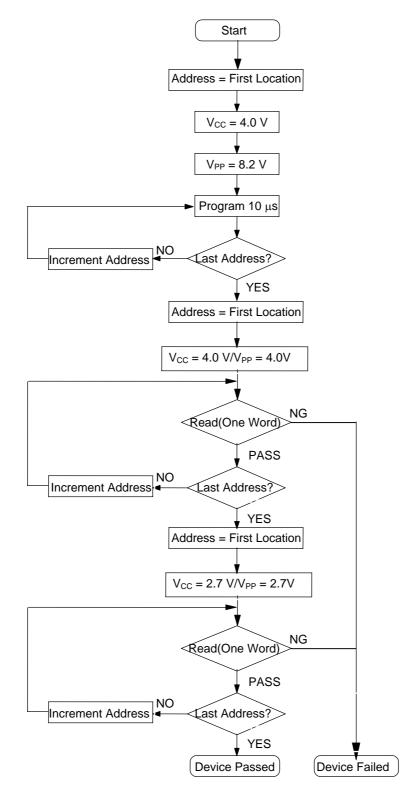
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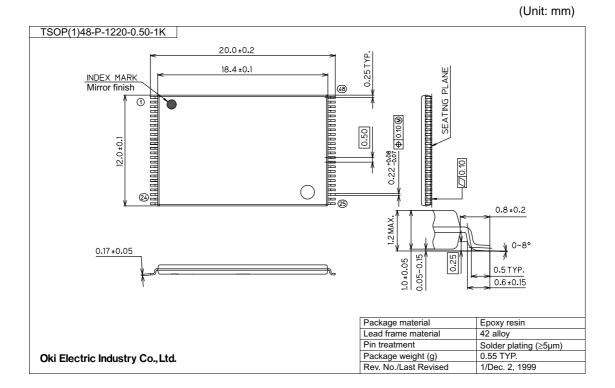
Program and Program Verify Cycle Waveforms



Programming Flow Chart



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document		Pa	ge			
No.	Date	Previous Edition	Current Edition	Description		
FEDR27V3252J-01-01	Mar. 26, 2004	-	-	Final edition 1		
FEDR27V3252J-01-02	Jul. 9, 2004	3	3	Add P_D condition and $I_{OS} = 10mA$		

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