

June 1998

### Features

- **12A, 500V, RDS(on) = 0.410Ω**
- **Second Generation Rad Hard MOSFET Results From New Design Concepts**
- **Gamma**
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- **Gamma Dot**
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- **Photo Current**
  - 45.0nA Per-RAD(Si)/sec Typically
- **Neutron**
  - Pre-RAD Specifications for 3E12 Neutrons/cm<sup>2</sup>
  - Usable to 3E13 Neutrons/cm<sup>2</sup>

### Description

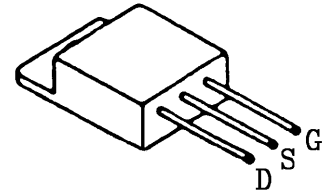
The Intersil has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100KRAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm<sup>2</sup> for 500V product to 1E14n/cm<sup>2</sup> for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n<sup>0</sup>) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

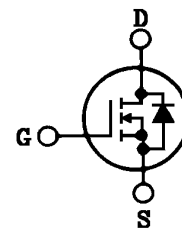
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Intersil High-Reliability Marketing group for any desired deviations from the data sheet.

### Package

TO-258AA



### Symbol



### Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

	FRE460D, R, H	UNITS	
Drain-Source Voltage . . . . .	VDS	500	V
Drain-Gate Voltage (RGS = 20kΩ) . . . . .	VDGR	500	V
Continuous Drain Current			
TC = +25°C . . . . .	ID	12	A
TC = +100°C . . . . .	ID	7	A
Pulsed Drain Current . . . . .	IDM	36	A
Gate-Source Voltage . . . . .	VGS	±20	V
Maximum Power Dissipation			
TC = +25°C . . . . .	PT	150	W
TC = +100°C . . . . .	PT	60	W
Derated Above +25°C . . . . .		1.20	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure) . . . . .	ILM	36	A
Continuous Source Current (Body Diode) . . . . .	IS	12	A
Pulsed Source Current (Body Diode) . . . . .	ISM	36	A
Operating And Storage Temperature . . . . .	TJC, TSTG	-55 to +150	°C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max. . . . .	TL	300	°C

# FRE460D, FRE460R, FRE460H

## Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS		UNITS	
			MIN	MAX		
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	500	-	V	
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V	
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA	
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA	
Zero-Gate Voltage Drain Current	IDSS1	VDS = 500V, VGS = 0	-	1	mA	
	IDSS2	VDS = 400V, VGS = 0	-	0.025		
	IDSS3	VDS = 400V, VG65S = 0, TC = +125°C	-	0.25		
Rated Avalanche Current	IAR	Time = 20μs	-	36	A	
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 12A	-	5.17	V	
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 7A	-	0.410	Ω	
Turn-On Delay Time	td(on)	VDD = 250V, ID = 12A Pulse Width = 3μs Period = 300μs Rg = 10Ω 0 ≤ VGS ≤ 10 (See Test Circuit)	-	88	ns	
Rise Time	tr		-	96		
Turn-Off Delay Time	td(off)		-	556		
Fall Time	tf		-	108		
Gate-Charge Threshold	QG(th)	VDD = 250V, ID = 12A IGS1 = IGS2 0 ≤ VGS ≤ 20	7	28	nc	
Gate-Charge On State	QG(on)		107	430		
Gate-Charge Total	QGM		202	808		
Plateau Voltage	VGP		2	10		V
Gate-Charge Source	QGS		19	76		nc
Gate-Charge Drain	QGD		43	172		nc
Diode Forward Voltage	VSD	ID = 12A, VGD = 0	0.6	1.8	V	
Reverse Recovery Time	TT	I = 12A; di/dt = 100A/μs	-	3000	ns	
Junction-To-Case	Rθjc		-	0.83	°C/W	
Junction-To-Ambient	Rθja	Free Air Operation	-	48		

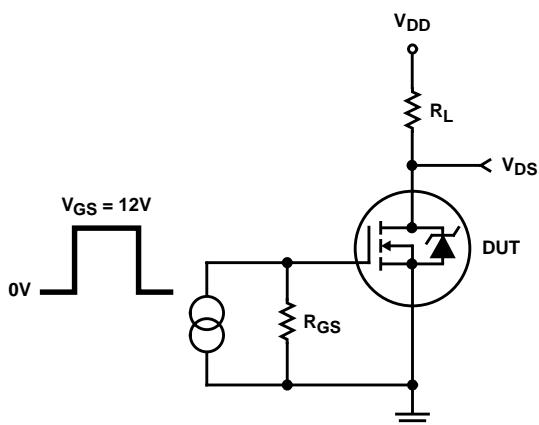


FIGURE 1. RESISTIVE SWITCHING TEST CIRCUIT

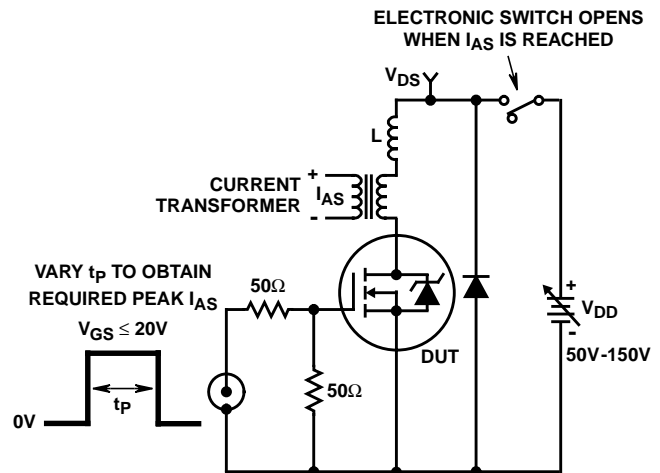


FIGURE 2. UNCLAMPED ENERGY TEST CIRCUIT

## FRE460D, FRE460R, FRE460H

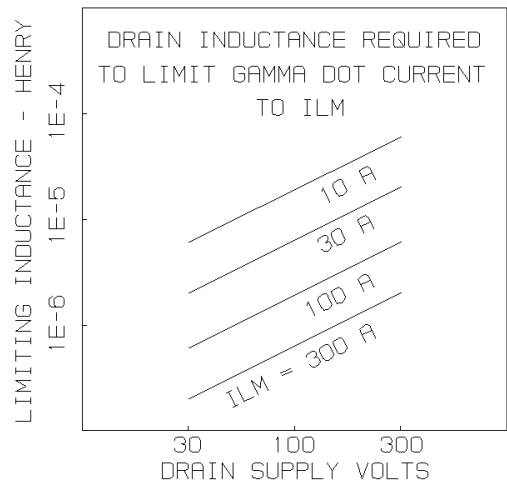
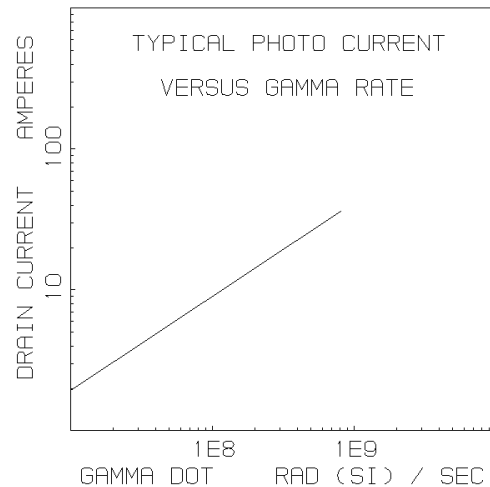
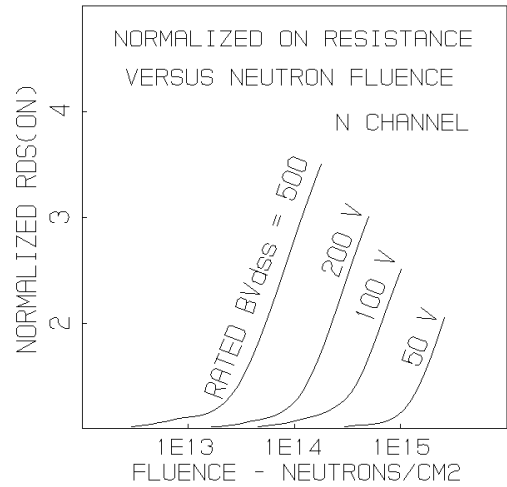
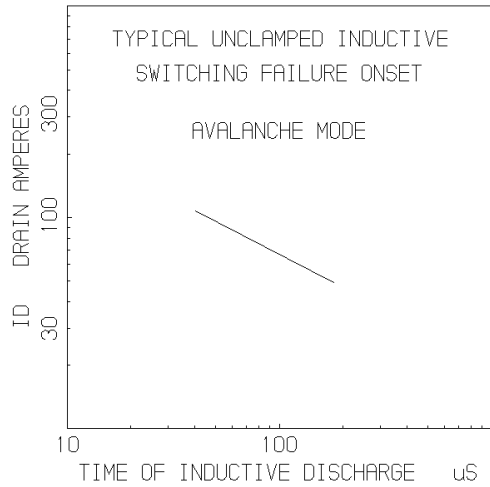
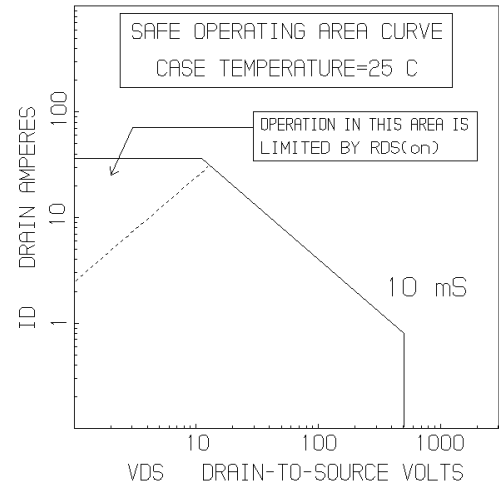
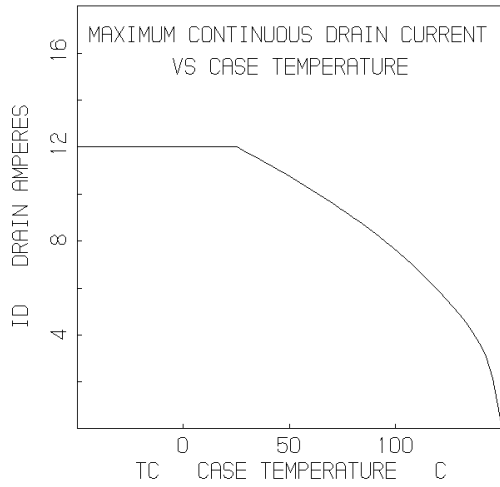
### Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS	
				MIN	MAX		
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	FRE460D, R	VGS = 0, ID = 1mA	500	-	V
	(Note 5, 6)	BVDSS	FRE460H	VGS = 0, ID = 1mA	475	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	FRE460D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	FRE460H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	FRE460D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	FRE460H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	FRE460D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	FRE460H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	FRE460D, R	VGS = 0, VDS = 400V	-	25	μA
	(Note 5, 6)	IDSS	FRE460H	VGS = 0, VDS = 400V	-	100	μA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	FRE460D, R	VGS = 10V, ID = 12A	-	5.17	V
	(Note 1, 5, 6)	VDS(on)	FRE460H	VGS = 16V, ID = 12A	-	7.75	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	FRE460D, R	VGS = 10V, ID = 7A	-	.410	Ω
	(Note 1, 5, 6)	RDS(on)	FRE460H	VGS = 14V, ID = 7A	-	.615	Ω

**NOTES:**

1. Pulse test, 300μs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R" Neutron = 3E12
5. Gamma = 1000KRAD(Si) Neutron = 3E12
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 11/14/90 on TA 17665 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, INTERSIL Application Note AN-8831, Oct. 1988

Typical Performance Characteristics



**Rad Hard Data Packages - Intersil Power Transistors**

**TXV Equivalent**

**1. Rad Hard TXV Equivalent - Standard Data Package**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
- F. Group C - Attributes Data Sheet
- G. Group D - Attributes Data Sheet

**2. Rad Hard TXV Equivalent - Optional Data Package**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
  - Precondition Lot Traveler
  - Pre and Post Burn-In Read and Record Data
- D. Group A - Attributes Data Sheet
  - Group A Lot Traveler
- E. Group B - Attributes Data Sheet
  - Group B Lot Traveler
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
  - Bond Strength Data (Subgroup B3)
  - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
- F. Group C - Attributes Data Sheet
  - Group C Lot Traveler
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
  - Bond Strength Data (Subgroup C6)
- G. Group D - Attributes Data Sheet
  - Group D Lot Traveler
  - Pre and Post RAD Read and Record Data

**Class S - Equivalents**

**1. Rad Hard "S" Equivalent - Standard Data Package**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report

- E. Preconditioning Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

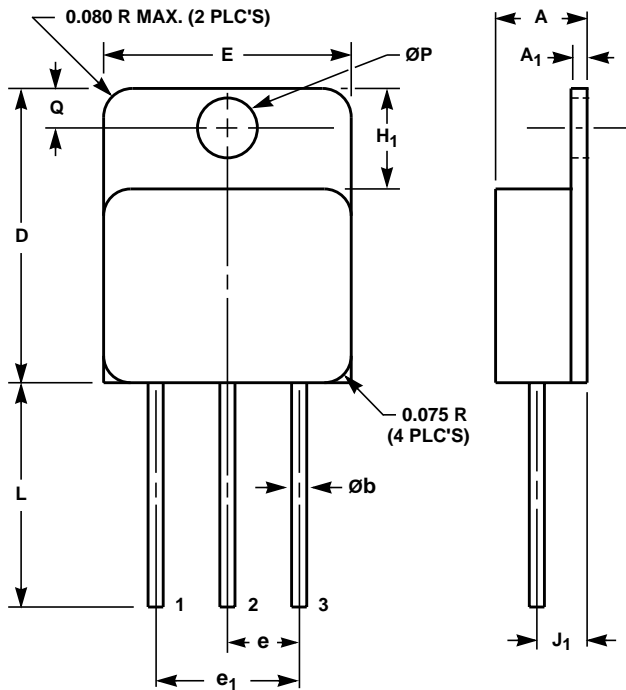
**2. Rad Hard Max. "S" Equivalent - Optional Data Package**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
  - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
  - Hi-Rel Lot Traveler
  - Pre and Post Radiation Data

# FRE460D, FRE460R, FRE460H

## TO-258AA

3 LEAD JEDEC STYLE TO-258AA HERMETIC METAL PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.250	0.270	6.35	6.85	-
A <sub>1</sub>	0.035	0.045	0.89	1.14	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.815	0.830	20.71	21.08	-
E	0.685	0.695	17.40	17.65	-
e	0.200 TYP		5.08 TYP		4
e <sub>1</sub>	0.400 BSC		10.16 BSC		4
H <sub>1</sub>	0.270	0.290	6.86	7.36	-
J <sub>1</sub>	0.130	0.150	3.31	3.81	4
L	0.600	0.650	15.24	16.51	-
ØP	0.155	0.165	3.94	4.19	-
Q	0.115	0.125	2.93	3.17	-

**NOTES:**

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-258AA outline dated 2-88. Except Øb.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 2 dated 5-98.

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