

May 2002 Revised July 2002

FST33X257

24:12 Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST33X257 is a 24:12 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{\text{OE}}_x$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{\text{OE}}_x$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

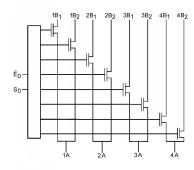
- \blacksquare 4 Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level

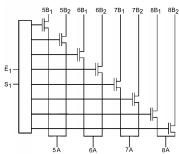
Ordering Code:

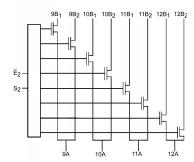
Order Number	Package Number	Package Description
FST33X257QSP	MQA48A	48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

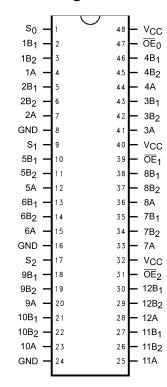
Logic Diagram







Connection Diagram



Pin Descriptions

Pin Name	Description				
<u>OE</u> _x	Bus Switch Enable				
S _x	Select Input				
Α	Bus A				
B ₁ –B ₂	Bus B				

Truth Table

S _x	OE _x	Function
Х	Н	Disconnect
L	L	$A = B_1$
Н	L	$A = B_2$

Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions (Note 3)

 $\begin{array}{ll} \mbox{Power Supply Operating (V_{CC})} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \end{array}$

Input Rise and Fall Time (t_r, t_f)

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

		V _{CC} (V)	$T_A = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$				
Symbol	Parameter		Min	Typ (Note 4)	Max	Units	Conditions
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18 \text{ mA}$
V _{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V _{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I _I	Input Leakage Current	5.5			±1.0	^	$0 \le V_{IN} \le 5.5V$
		0			10	μΑ	V _{IN} = 5.5V
I _{OZ}	OFF-STATE Leakage Current	5.5			±1.0	μΑ	0 ≤ A, B ≤ V _{CC}
R _{ON}	Switch On Resistance	4.5		4	7	Ω	V _{IN} = 0V, I _{IN} = 64 mA
	(Note 5)	4.5		4	7	Ω	V _{IN} = 0V, I _{IN} = 30 mA
		4.5		8	15	Ω	V _{IN} = 2.4V, I _{IN} = 15 mA
		4.0		11	20	Ω	V _{IN} = 2.4V, I _{IN} = 15 mA
I _{CC}	Quiescent Supply Current (Note 6)	5.5			3	μΑ	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
ΔI _{CC}	Increase in I _{CC} per Input	5.5			2.5	mA	One Input at 3.4V
	(Note 7)						Other Inputs at V _{CC} or GND

Note 4: Typical values are at $V_{CC} = 5.0 V$ and $T_A = +25 ^{\circ} C$

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 6: Per V_{CC} pin.

Note 7: Per TTL driven input, control pins only.

AC Electrical Characteristics

Symbol	Parameter	$\begin{aligned} T_{A} &= -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C}, \\ C_{L} &= 50 \text{ pF, RU} = \text{RD} = 500\Omega \\ \\ V_{CC} &= 4.5 - 5.5\text{V} & V_{CC} = 4.0\text{V} \end{aligned}$			Units	Conditions	Figure Number	
		Min	Max	Min	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 8)		0.25		0.25	ns	V _I = OPEN F	Figures
	Propagation Delay, Select to Bus A	1.0	4.7		5.2	115		1, 2
t _{PZH} , t _{PZL}	Output Enable Time, Select to Bus B	1.0	5.2		5.7	ns	$V_I = 7V$ for t_{PZL}	Figures 1, 2
	Output Enable Time, OE to Bus A, B	1.0	5.1		5.6		$V_I = OPEN$ for t_{PZH}	
t _{PHZ} , t _{PLZ}	Output Disable Time, Select to Bus B	1.0	5.2		5.5	ns	$V_I = 7V$ for t_{PLZ}	Figures 1, 2
	Output Disable Time, Output Enable Time,	1.5	5.5		5.5	115	$V_I = OPEN$ for t_{PHZ}	
	OE to Bus A, B							

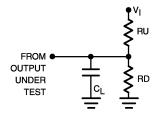
Note 8: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 9)

Symbol		Parameter	Тур	Max	Units	Conditions
C _{IN}		Control Pin Input Capacitance	3		pF	V _{CC} = 5.0V
C _{I/O}	A Port Input/Output Capacitance		7		pF	V_{CC} , $\overline{OE} = 5.0V$
	B Port		5		pF	VCC, OL = 5.0 V

Note 9: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

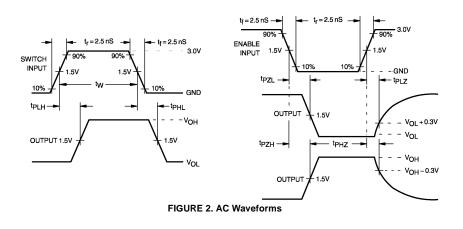
AC Loading and Waveforms

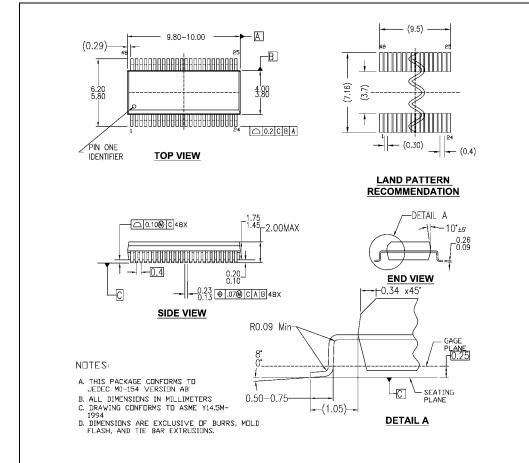


Note: Input driven by 50 Ω source terminated in 50 Ω Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit





MQA48AREVA

48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide Package Number MQA48A

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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