GENERAL DESCRIPTION

The ft4888 is a dual bridge-connected audio power amplifier. When supplied with 5V voltage, the ft4888 can deliver 2.1W to a 4Ω load or 2.4W to a 3Ω load with THD+N less than 1.0%.

The ft4888's dual power amplifier topology provides high quality dual outputs while requiring fewer external components and consuming minimum PCB space. With two device selection inputs (HP_LOGIC and HP_SENSE) of different logic level thresholds respectively, the ft4888 can connect to a pair of dual-channel speakers or to a stereo headphone. The HP_SENSE logic connects to the headphone jack to detect if headphone is present. The other logic, HP_LOGIC, is determined by standard logic level standards.

The ft4888 also features an optional 3D enhancement design which can help widen the perceived soundstage from a stereo audio signal to improve stereo channel sounding effect.

FEATURES

- P_O @ 1% THD+N, V_{DD} = 5V
  - R_L = 3Ω , P_O = 2.4W (typical)
  - R_L = 4Ω , P_O = 2.1W (typical)
  - R_L = 8Ω , P_O = 1.3W (typical)
- 3D effect enhancement
- User-configurable headphone selection scheme
- Shutdown current: 0.04μA
- Supply voltage range: 2.7V to 5.5V
- PSRR @ 217Hz: 85dB (typical)
- Micro power shutdown mode
- Improved "click and pop" suppression circuitry
- Space-saving QFN4X4-24L package

APPLICATIONS

- Cell phone
- Personal digital assistant (PDA)
- Powered electronic devices

APPLICATION CIRCUIT

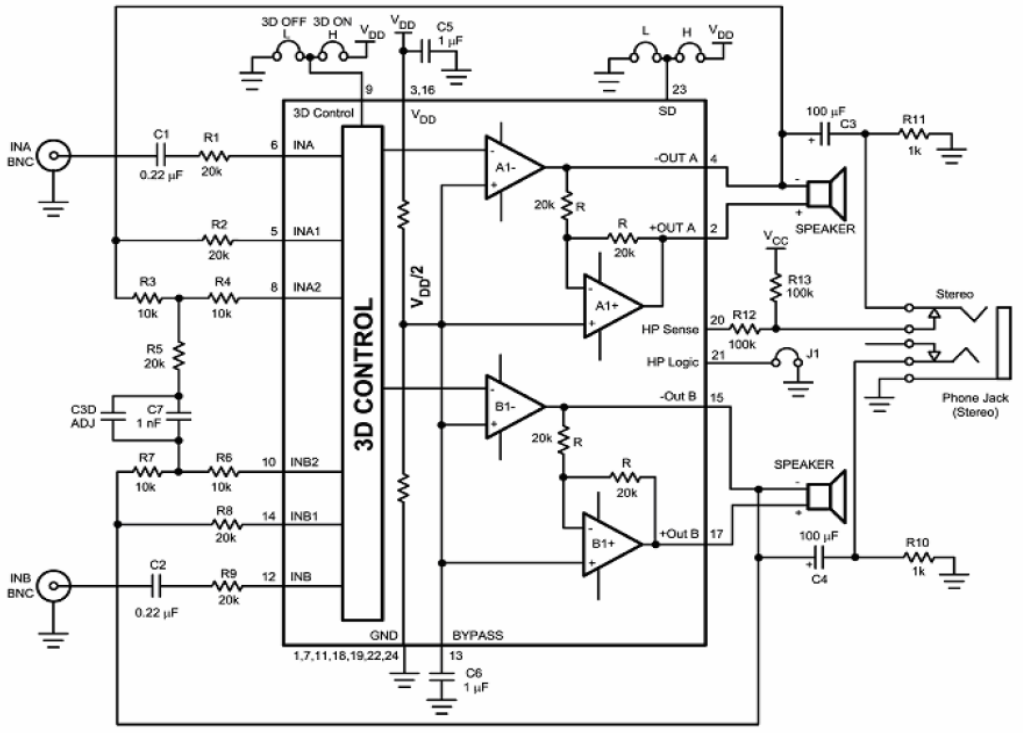
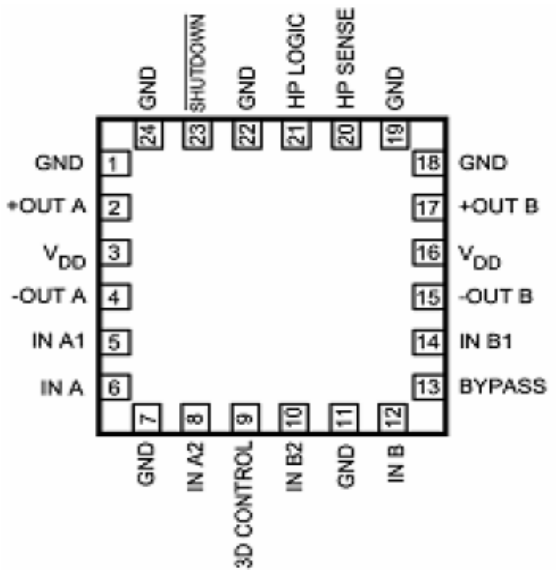


Figure 1: Typical Application Circuit

PIN CONFIGURATION AND DESCRIPTION

ft4888 QFN4X4-24L Package （TOP VIEW）



PIN	PIN	I/O	DESCRIPTION
+OUTA	2	O	Left channel +output
V_{DD}	3,16		Supply voltage
-OUTA	4	O	Left channel -output
-OUTB	15	O	Right channel -output
+OUTB	17	O	Right channel +output
INA	6	I	Left channel input
INA1	5	I	Left channel feedback for no stereo enhancement mode
INA2	8	I	Left channel feedback for stereo enhancement mode
GND	1,7,11,18,19,22,24		GND
INB	12	I	Right channel input
INB1	14	I	Right channel feedback for no stereo enhancement mode
INB2	10	I	Right channel feedback for stereo enhancement mode
Stereo Enhancement Control	9	I	Active high for stereo enhancement mode Active low for general stereo mode
BYPASS	13		Bypass capacitor which provides the common mode voltage
HP Logic	21	I	Headphone logic control
HP Sense	20	I	Headphone sense control
$\overline{\text{SHUTDOWN}}$	23	I	Active low shutdown control

ORDERING INFORMATION

P/N	TEMPERATURE RANGE	PACKAGE
ft4888	-40°C to +85°C	QFN4X4-24L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply voltage	-0.3V to 6.0V
Input voltage	−0.3V to VDD +0.3V
Junction temperature	150°C
Storage temperature	−65°C to +150°C
Vapor phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Note: Stresses beyond those listed under absolute maximun ratings may cause permanent damage to the device. These are stress ratings only,and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ JC	Θ JA	UNIT
LLP-24L	3	42	°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage	2.7		5.5	V
Operating free-air temperature, TA	-40		85	°C

ELECTRICAL CHARACTERISTICS

VDD = 5V, T_A = 25°C, Gain = 2V/V, BTL Mode, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A， BTL Mode		6.0	10	mA
		V_{IN} = 0V, I_O = 0A, SE Mode		4.0	7.0	
I_{SD}	Shutdown Current			0.04	2.0	μ A
V_{IHSD}	Shutdown, Headphone Logic, 3D control, High Input Voltage		1.3			V
V_{ILSD}	Shutdown, Headphone Logic, 3D control, Low Input Voltage				0.4	V
V_{IH}	Headphone Sense High Input Voltage		4.0			V
V_{IL}	Headphone Sense Low Input Voltage				0.8	V
T_{WU}	Turn On Time	1μ F Bypass Cap (C6)		100		ms
V_{OS}	Output Offset Voltage	V_{IN} = 0V		5.0		mV
P_O	Output Power (BTL Mode)	THD+N = 1%, f = 1kHz, R_L = 8Ω		1.3		W
		THD+N = 1%, f = 1kHz, R_L = 4Ω		2.1		W
P_O	Output Power, SE Mode	THD+N = 0.5%, f = 1kHz, R_L = 32Ω		90		mW
		f = 1kHz, R_L = 8Ω , P_O = 0.9W		0.06		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		85		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C6= 1μ F, R_L = 8Ω		80		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		66		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		72		dB
Xtalk	Channel separation	f=1KHz, C6 = 1μ F		85		dB

VDD = 3V, T_A = 25°C, Gain = 2V/V, BTL Mode, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A， BTL Mode		4.5		mA
		V_{IN} = 0V, I_O = 0A, SE Mode		3.0		
I_{SD}	Shutdown Current			0.01	2	μ A
V_{IHSD}	Shutdown, Headphone Logic, 3D control, High Input Voltage		1.2			V
V_{ILSD}	Shutdown, Headphone Logic, 3D control, Low Input Voltage				0.4	V

V_{IH}	Headphone Sense High Input Voltage		2.5			V
V_{IL}	Headphone Sense Low Input Voltage				0.7	V
T_{WU}	Turn On Time	1μ F Bypass Cap (C6)		140		ms
V_{OS}	Output Offset Voltage	V_{IN} = 0V		2.5		mV
P_O	Output Power (BTL Mode)	THD+N = 1%, f = 1kHz, R_L = 8Ω		0.45		W
		THD+N = 1%, f = 1kHz, R_L =4Ω		0.7		W
P_O	Output Power, SE Mode	THD+N = 0.5%, f = 1kHz, R_L = 32Ω		35		mW
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, R_L = 8Ω , P_O =0.35W		0.08		%
PSRR	Power Supply Rejection Ratio	Input un-terminated, 217Hz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		85		dB
		Input un-terminated, 1kHz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		80		dB
		Input grounded, 217Hz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		65		dB
		Input grounded, 1kHz, V_{ripple} = 200mV_{p-p}, C6 = 1μ F, R_L = 8Ω		70		dB
Xtalk	Channel separation	f=1kHz, C6 = 1μ F		85		dB

TYPICAL CHARACTERISTICS

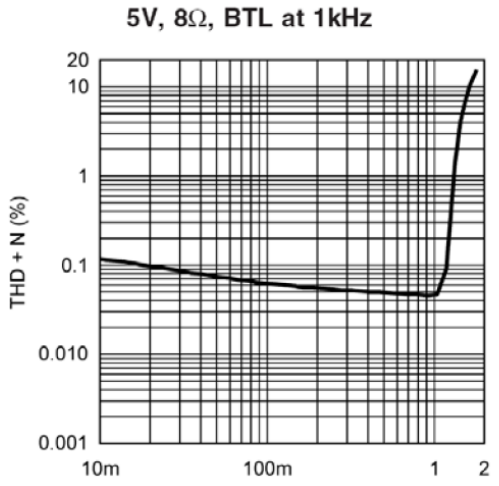


Figure 2: THD+N vs. Output Power

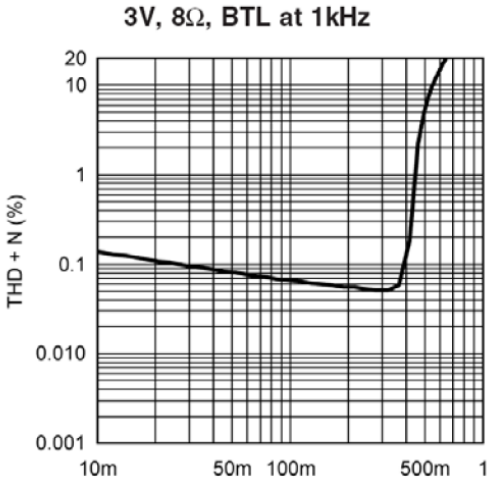


Figure 3: THD+N vs. Output Power

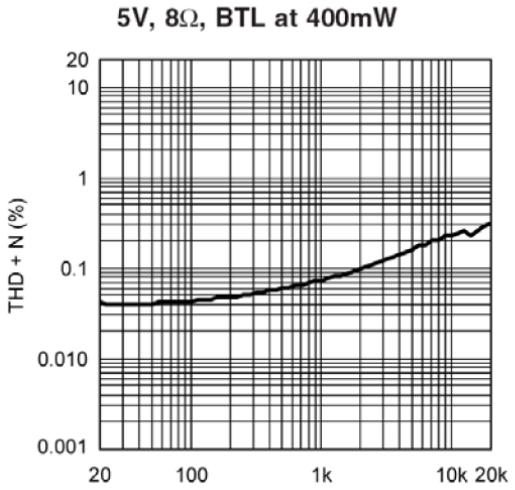


Figure 4: THD+N vs. Frequency

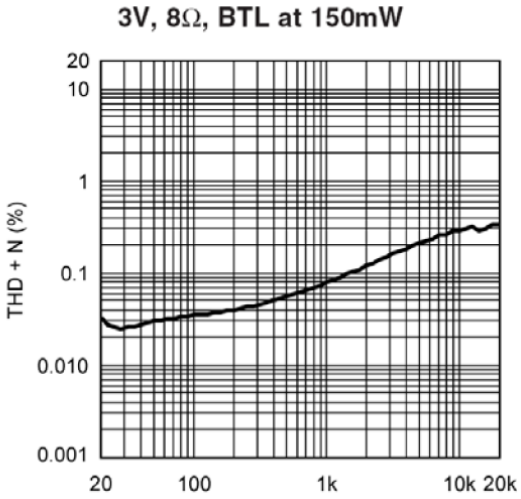


Figure 5: THD+N vs. Frequency

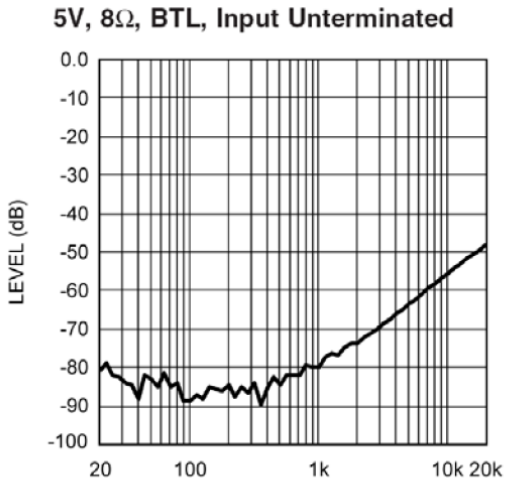


Figure 6: PSRR vs. Frequency

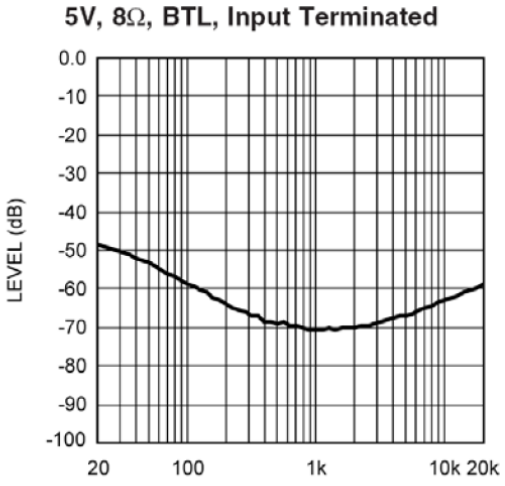


Figure 7: PSRR vs. Frequency

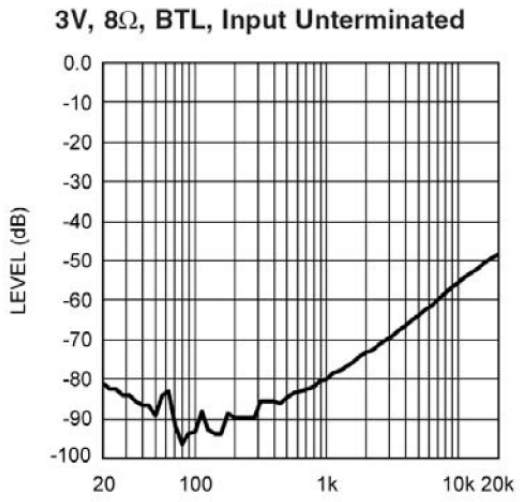


Figure 8: PSRR vs. Frequency

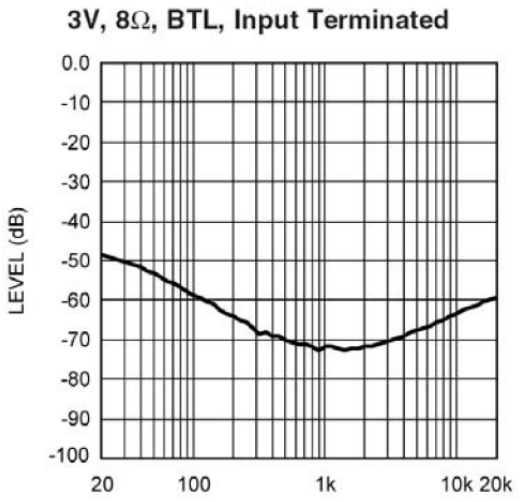


Figure 9: PSRR vs. Frequency

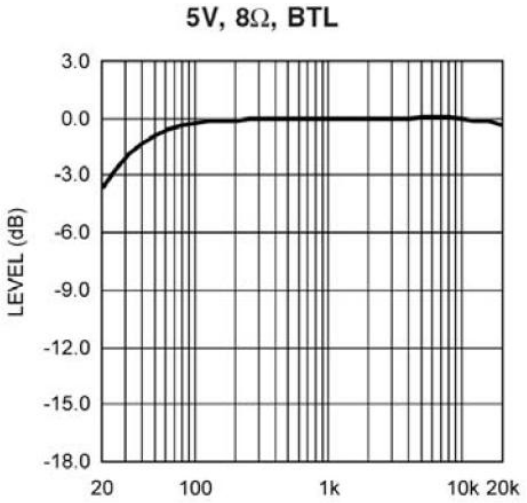


Figure 10: Frequency Response

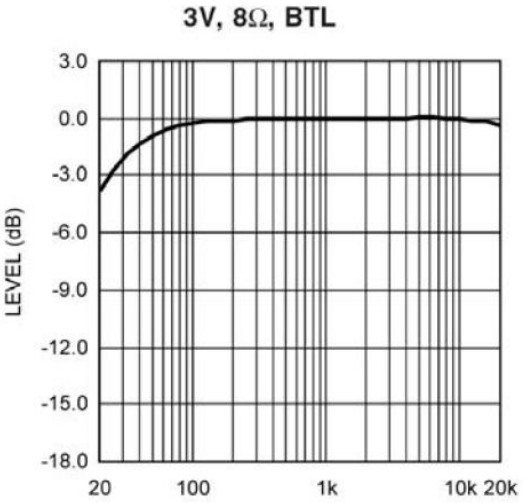


Figure 11: Frequency Response

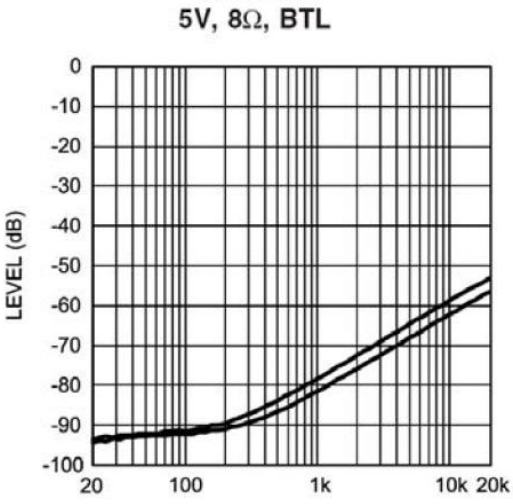


Figure 12: Crosstalk

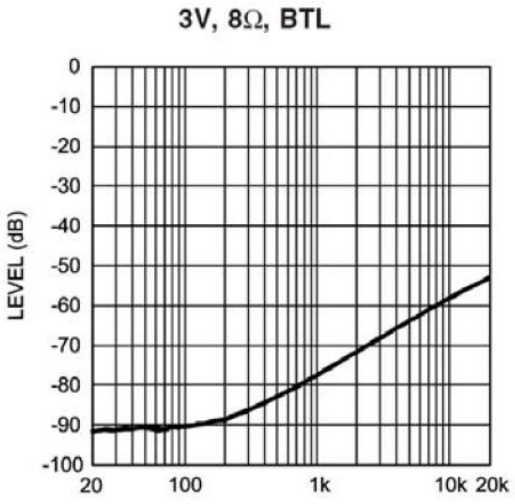


Figure 13: Crosstalk

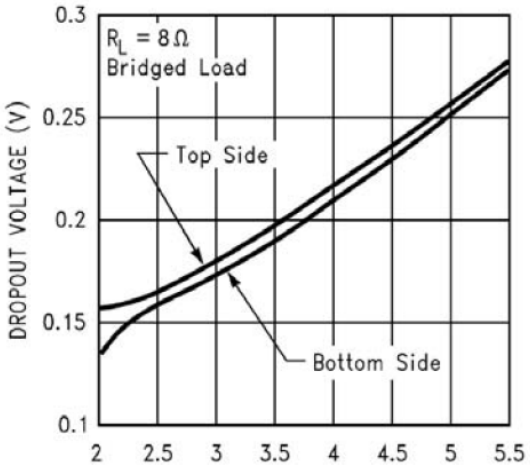


Figure 14: Dropout Voltage vs. Supply Voltage

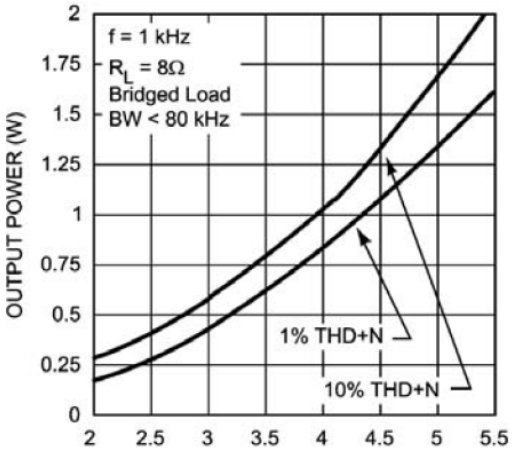


Figure 15: Dropout Voltage vs. Supply Voltage

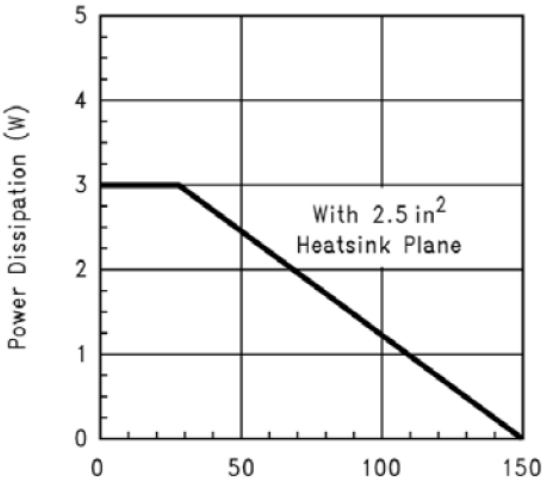


Figure 16: Power Dissipation vs. Temperature

APPLICATION INFORMATION

BRIDGED AMPLIFIER

As shown in Figure 1, the ft4888 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors R2 (or R3, R4) and R8 (or R6, R7) and input resistors R1 and R9 set the closed-loop gain of Amp A (-OUT) and Amp B (-OUT), whereas two internal 20kΩ resistors set Amp A's (+OUT) and Amp B's (+OUT) gain at 1. Each channel's (+OUT) signal identical in magnitude, but opposite in phase with (-OUT) signal. Hence the load between the (+OUT) and (-OUT) is driven differentially, or in another word, in bridge mode (BTL mode).

The gain of BTL mode:

$$A_{VD} = 2 * (R_F / R_I) \qquad (1)$$

or

$$A_{VD} = 2 * (R2 / R1)$$

Bridge mode amplifier provides four times the output power of that from single-ended amplifier under the same condition. However, the power increase calculation assumes that amplifier is not current limited or that the output signal is not clipped. Therefore, to ensure minimum output signal clipping, care must be taken when choosing an amplifier's closed-loop gain.

POWER DISSIPATION

Power dissipation is critical for either single-ended or bridged amplifier board design. Equation (2) indicates the maximum power dissipation for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Single-ended} \qquad (2)$$

For ft4888 where two operational amplifiers per channel are adopted, the internal power dissipation per channel is four times that of a single-ended amplifier, as indicated in Equation (3). Given a 5V input power and a 8Ω output load, the maximum total power dissipation is 0.63W for single channel or 1.26W for stereo output.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Bridge mode} \qquad (3)$$

Twice the maximum power dissipation given by Equation (3) must not exceed the power dissipation given by Equation (4). The ft4888's T_{JMAX} is 150°C; Θ_{JA} is 20°C/W given that the package is soldered to a DAP pad that expands to a copper area of 5 square inches on PCB. Equation (5) is a variation of Equation (4) for calculating the maximum ambient temperature at maximum stereo power dissipation when junction temperature limitation is not exceeded.

$$P_{DMAX}' = (T_{JMAX} - T_A) / \Theta_{JA} \qquad (4)$$

$$T_A = T_{JMAX} - 2*P_{DMAX}\Theta_{JA} \qquad (5)$$

The examples above assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If twice the P_{DMAX} in Equation (2) or (3) exceeds P_{DMAX}' in Equation (4), measures should be taken by decreasing the supply voltage, increasing load impedance, reducing the ambient temperature or adding external heat sink. When heat sink is applied to system design, the Θ_{JA} equals (Θ_{JC} + Θ_{CS} + Θ_{SA}). (Θ_{JC}: junction-to-case thermal impedance; Θ_{CS}: case-to-sink thermal impedance; Θ_{SA}: sink-to-ambient thermal impedance.)

POWER SUPPLY BYPASSING

Proper power supply bypassing is critical for low noise performance and high power supply rejection in a power amplifier. Applications employing 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a 1.0µF tantalum bypass capacitor connected between the ft4888's power supply pins and the ground. Do not substitute a ceramic capacitor for the tantalum, or it would cause oscillation. Optimizing the length of leads and traces between the ft4888 and ground also help to improve the power supply bypassing.

MICRO-POWER SHUTDOWN

The ft4888's power saving scheme is realized through the SHUTDOWN pin and the voltage applied on it. The micro-power shutdown is performed to turn off the amplifier's bias circuitry as long as the SHUTDOWN pin is grounded. Typically, supply current as low as 0.04µA can be achieved by applying a voltage close to GND to the SHUTDOWN pin.

The Micro-Power shutdown can be initiated and controlled by either a single-pole, single-throw switch, or a microprocessor, or a microcontroller. A switch is employed in the reference design illustrated Figure 1. Connect an external 100k resistor between the SHUTDOWN pin and the ground; connect the switch between the SHUTDOWN pin and V_{DD}. Closing the switch sets the amplifier in normal function, while opening the switch sets the SHUTDOWN pin to ground through the 100k resistor and consequently activates the shutdown. The switch and resistor design guarantees that the SHUTDOWN pin is not float to prevent unwanted state changes. In digital systems, where microprocessors or microcontrollers are deployed, digital output can be applied to control the SHUTDOWN input voltage.

HEADPHONE AND SPEAKER SELECTION

The headphone and speaker selection in ft4888 is achieved with the HP_SENSE and HP_LOGIC pins. When both HP_SENSE and HP_LOGIC pins are pulled low, the bridged mode is enabled. When either pin is pulled high, the (+OUT) outputs are cut off and the amplifier is set to single-ended mode. Figure 17 illustrates the headphone and speaker selection scheme using HP_SENSE pin. When headphone is not present, the HP_SENSE pin receives a voltage as low as 50mV which pulled the pin low and set the amplifier in bridged mode. When headphone is inserted into the jack, the sense pin is disconnected and the HP_SENSE is pulled high. Therefore the amplifier is set to single-ended mode. The HP_LOGIC pin can also be used to select headphone or speaker. When HP_LOGIC is pulled high, the ft4888 operates in single-ended mode; when pulled low, the ft 4888 operates in bridged mode subjected to that the HP_SENSE pin is also pulled low.

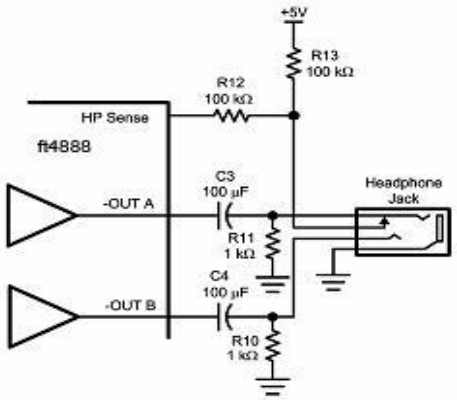


Figure 17: Headphone Circuit with HP_SENSE

Headphone and Speaker Selection Pin Signals:

HP_LOGIC Pin	HP_SENSE Pin	Operational output
High	Don't care	Single-ended mode
Low	Low (Headphone not present)	Bridged mode
Don't care	High (Headphone present)	Single-ended mode

3D ENHANCEMENT

The ft4888 provides a 3D enhancement feature which help to improve the stereo sound channel separation when the left and right speakers are too close to each other. This feature is achieved by widening the perceived soundstage from the analog audio signal. In the reference design, an external RC network is added to enable or disable the 3D enhancement. The degree of 3D enhancement is decided by R5 and C7 or C3D_ADJ. Decreasing the R5 resistance will increase the 3D effect. Increasing the C7 or C3D capacitance will decrease the low cutoff frequency at which point the 3D enhancement starts to function. Refer to Equation below.

$$f_{3D(-3dB)} = 1/2\pi\ (R_{3D})(C_{3D}) \qquad (6)$$

To activate the 3D enhancement, apply VDD to the 3D_CONTROL pin to increase the gain by a multiplication factor of (1 + 20kΩ/R5). When R5 is 20KΩ, the multiplication factor is 2, and the gain increases by 6dB. Note that when 3D enhancement mode is enabled, R3 and R4 replace R2, and R6 and R7 replace R8.

INPUT CAPACITOR VALUE SELECTION

High value input coupling capacitors (C1, C2) are required to amplifying the low inputting audio signal as illustrated in Figure 1. However, high value capacitor can be expensive in cost and big in size which may become a fatal defect for handheld devices. Besides, the speakers in handheld and portable devices, either internal or external, seldom reproduce signals below 150Hz. Therefore, big input capacitor has very little influence in output signal quality in applications using limited frequency response speakers. Besides the cost and size, C1 and C2 also influence the click and pop performance. When the supply voltage is fed in, a transient (pop) is generated as the charge on the input capacitor changes from 0 to a quiescent state. The magnitude of the pop is proportional to the input capacitance. The higher the capacitance is, the more time it requires to reach quiescent DC voltage (usually 0.5VDD) when charged with a fixed current. The amplifier output charges the input capacitor through the feedback resistors (R2, R8). Therefore, pops can be minimized with input capacitance no higher than necessary to provide -3dB frequency. R1 and R9 are input resistors. C1 and C2 produce -3dB high pass filter cutoff frequency as stated in Equation (7).

$$f_{-3dB} = 1 / (2\pi\ R_{IN}C_{IN}) = 1 / (2\pi\ R1C1) \qquad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C1, using Equation (7), is 0.053µF. The 0.33µF C1 shown in Figure 1 allows the ft4888 to drive high efficiency, full range speaker whose response extends below 30Hz.

BYPASS CAPACITOR VALUE SELECTION

Bypass capacitor determines the time needed for setting ft4888 to quiescent operation and plays an important role in minimizing turn-on pops. The slower the output ramp to quiescent DC voltage (0.5VDD nominal), the smaller the turn-on pops is. The relationship between the capacitance and turn-on time is listed in the table below. In Figure 1, C6 is a 1.0µF bypass capacitor, minimizes the pops and clicks, improves the amplifier's

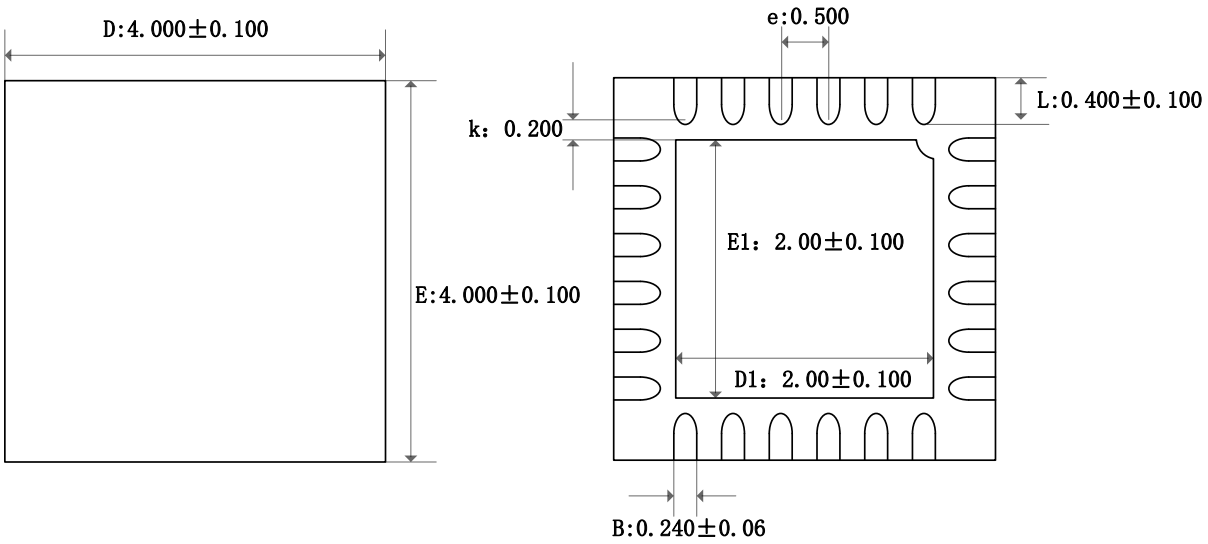
PSRR.

Here are some typical turn-on times for various values of C6:

C6	0.1μF	0.22μF	0.47μF	1.0μF
TON	40ms	60ms	80ms	140ms

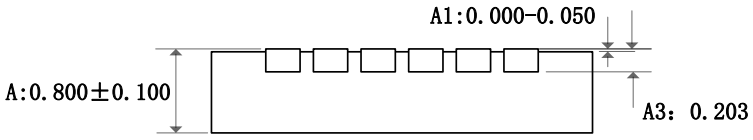
PHYSICAL DIMENSIONS

QFN4X4-24L PACKAGE OUTLINE DIMENSIONS



Top View

Bottom View



Side View

All dimensions are in millimeters

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

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Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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