



# CML Semiconductor Products

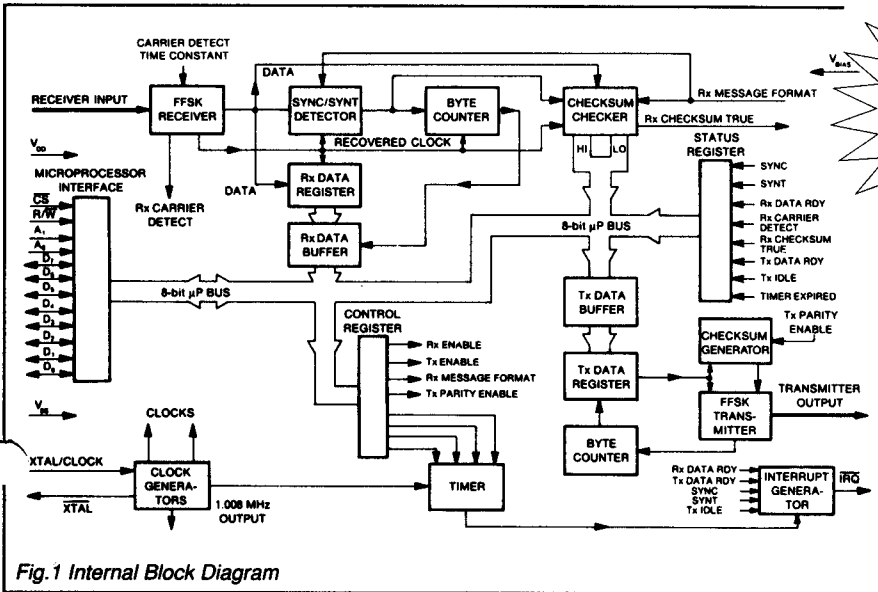
PRODUCT INFORMATION

## FX429 Band III FFSK Modem for Trunked Radio Systems

Publication D/429/6 July 1994

### Features/Applications

- Band III and General Purpose Trunked Radio Applications
- Full-Duplex 1200 Baud Operation
- High Intelligence
- Error Checking in Receive
- Error Check Word Generation
- Frame SYNC and SYNT Detection
- Preamble Generation
- $\mu$ Processor Compatible Interface
- Carrier Detection On-Chip
- Low Power Consumption
- General Purpose Timer



**NEW**  
1200/2400Baud  
Version Available  
**FX429A**

**FX429**

Fig.1 Internal Block Diagram

### Brief Description

The FX429 is a single-chip CMOS 1200 baud FFSK Modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications.

The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The FX429 is full duplex at 1200 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits.

Preamble and an error-check word are automatically generated in the transmit mode.

Error checking is performed and the 16-bit SYNC or SYNT words are detected in the receive mode.

An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides all microcircuit filter sampling clocks and modem timings whilst also supplying a "Clock + 4" output (1.008MHz).

The FX429, which has a powersaving facility, requires a single 5-volt power supply and is available in both cerdip DIL and plastic SMD packages.

# Pin Number

# Function

DIL Quad  
FX429J FX429LG/LS

1 1  
2 2  
3 4  
5 5  
6 6  
7 7  
8 8  
9 9  
10 10  
11 11  
12 12  
13 13  
14 14  
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21 21  
23 22  
24 23  
4, 22 3, 24

**V<sub>BIAS</sub>** : The internal circuitry bias line, held at V<sub>DD</sub>/2 this pin must be decoupled to V<sub>SS</sub> by capacitor C<sub>4</sub>, see Figure 3. **Warning Note** – In order to reduce current consumption, the potential at this pin is lowered to V<sub>SS</sub> when both Tx and Rx are disabled.

**Transmit Output** : The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not enabled by the Control Register ( D<sub>0</sub> ) its output impedance is set high.

**Receiver Input** : The 1200 baud received FFSK signal input. The 1200Hz/1800Hz audio to this pin must be a.c. coupled via capacitor C<sub>3</sub>, see Figure 3.

**V<sub>DD</sub>** : Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V<sub>SS</sub> by capacitor C<sub>6</sub>, see Figure 3.

**Carrier Detect Time Constant** : The on-chip Carrier Detect integration function requires two external components on this pin. A capacitor, C<sub>5</sub>, to V<sub>SS</sub>, together with a resistor, R<sub>2</sub>, to V<sub>DD</sub>. See Figure 3.

**Xtal/Clock** : The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here. See Figure 3.

**Xtal** : The output of the 4.032 MHz clock oscillator.

**D<sub>0</sub> :** **Microprocessor Data Interface**

**D<sub>1</sub> :**  
**D<sub>2</sub> :**  
**D<sub>3</sub> :** These 8 lines are used by the device to communicate with a microprocessor  
**D<sub>4</sub> :** with the A<sub>2</sub>, A<sub>0</sub> and A<sub>1</sub> inputs determining register selection.  
**D<sub>5</sub> :**  
**D<sub>6</sub> :**  
**D<sub>7</sub> :**

**A<sub>0</sub> :** **Register Selection.** These inputs, with the A<sub>2</sub> input, select the required register to the data bus as shown in Table 1 (below).  
**A<sub>1</sub> :**

**Table 1**

Register	A <sub>2</sub>	A <sub>0</sub>	A <sub>1</sub>
Control	0	1	1
Status	1	1	1
Rx Data	1	0	1
Tx Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

**Strobe** : Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating high-order address bits with a read/write clock. The FX429 is selected when Strobe = logic "0." See Figure 5.

**A<sub>2</sub>** : Used in conjunction with A<sub>1</sub> and A<sub>0</sub> to determine which internal registers are connected to the data interface pins ( D<sub>0</sub> – D<sub>7</sub> ) during Strobe (see Table 1 and Figure 5).

**IRQ** : Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kΩ pullup to V<sub>DD</sub>). The conditions that cause the interrupts are indicated at the Status Register and are as follows:

*Timer Expired*                      *Rx Data Ready*                      *Tx Data Ready*  
*Tx Idle*                                      *Rx SYNC Detect*                      *Rx SYNT Detect*

**V<sub>SS</sub>** : Negative Supply (GND).

**Clock + 4** : A 1.008 MHz ( X<sub>1</sub> + 4 ) clock is available at this output for external circuit use, note the source impedance and source current limits.

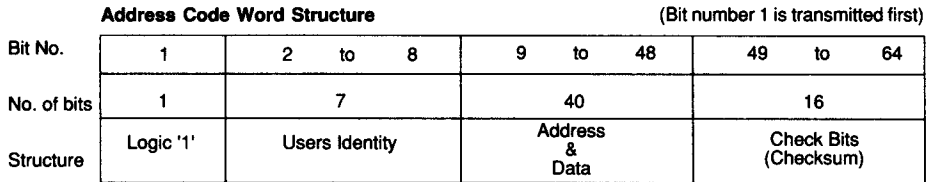
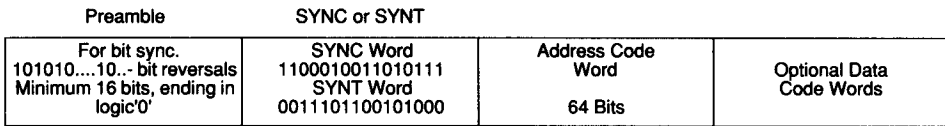
These pins are not connected internally, leave open circuit.

# Modems in Mobile Data Signalling ..... An Introduction

## Digital Code Format

The recommended Digital Code Format for use over Land Mobile Radio Systems is detailed in the Department of Trade and Industry, Radio Regulatory Division's publications MPT 1317 and MPT 1327, and is as described briefly below.

Fig. 2 The Data stream – Rx and Tx at 1200baud, the minimum, overall transmission length is 96 bits.



## Operation

The FX429 can be used for Full-Duplex operation with the host microprocessor only having to operate on the data whilst the modem (FX429) handles all other signalling routines and requirements.

In the Tx mode the FX429 will :-

- (1) Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
- (2) Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
- (3) Accept from the host, and transmit, 6 bytes of data (Address Code Word).
- (a) Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes. – or –
- (b) Upon a software command, disable internal checksum generation and allow continuous data transmission.
- (c) Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the Rx mode the FX429 will :-

- (1) Detect and achieve bit synchronization within 16 bits.
- (2) Search for and detect the 16-bit 'SYNC'/SYNT' word.
- (3) Output all received data after 'SYNC/SYNT,' in byte form.
- (4) Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.

**Note** – In Rx a software command is used to determine whether a 'SYNC'/SYNT' word is required after every 8 (6 data + 2 checksum ) received bytes, or "data" is received continually.

Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

## Non MPT Application – Full-Duplex

The functions described in this section, to allow the FX429 modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

**Tx** – When enabled the device transmits a "101010.....10" preamble until data for transmission is loaded by the host microprocessor.

Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages). Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

**Rx** – When enabled requires the 16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

# Control Register

A<sub>1</sub> = 1

A<sub>0</sub> = 1

A<sub>2</sub> = 0

Write Only

The Control Register, when selected, directs the modem's operation as described below.

Bit	Description	Function	Set = logic '1' (High) Clear = logic '0' (Low)																																																																																					
Bit 0 D <sub>0</sub>	<b>Tx Enable *</b>	<b>Set</b> – D <sub>0</sub> enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. <b>Clear</b> – The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.																																																																																						
Bit 1 D <sub>1</sub>	<b>Tx Parity Enable</b>	<b>Set</b> – D <sub>1</sub> indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. <b>Clear</b> – No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written".																																																																																						
Bit 2 D <sub>2</sub>	<b>Rx Enable *</b>	<b>Set</b> – D <sub>2</sub> enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. <b>Clear</b> – The receiver is disabled and all interrupts caused by the receiver are inhibited.																																																																																						
Bit 3 D <sub>3</sub>	<b>Rx Message Format</b>	<b>Set</b> – D <sub>3</sub> is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. <b>Clear</b> – The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received.																																																																																						
Bit 4 D <sub>4</sub>	<b>Timer LSB</b>	<p>These four bits control the timer as follows :-</p> <table border="1"> <thead> <tr> <th>D<sub>7</sub></th> <th>D<sub>6</sub></th> <th>D<sub>5</sub></th> <th>D<sub>4</sub></th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Reset counter and disable timer interrupts</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Count and interrupt every - 8 bits</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>" " " 16 bits</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>" " " 24 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>" " " 32 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>" " " 40 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>" " " 48 bits</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>" " " 56 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>" " " 64 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>" " " 72 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>" " " 80 bits</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>" " " 88 bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>" " " 96 bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>" " " 104 bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>" " " 112 bits</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>" " " 120 bits</td> </tr> </tbody> </table>		D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>		0	0	0	0	Reset counter and disable timer interrupts	0	0	0	1	Count and interrupt every - 8 bits	0	0	1	0	" " " 16 bits	0	0	1	1	" " " 24 bits	0	1	0	0	" " " 32 bits	0	1	0	1	" " " 40 bits	0	1	1	0	" " " 48 bits	0	1	1	1	" " " 56 bits	1	0	0	0	" " " 64 bits	1	0	0	1	" " " 72 bits	1	0	1	0	" " " 80 bits	1	0	1	1	" " " 88 bits	1	1	0	0	" " " 96 bits	1	1	0	1	" " " 104 bits	1	1	1	0	" " " 112 bits	1	1	1	1	" " " 120 bits
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Bit 5 D <sub>5</sub>	<b>Timer</b>																																																																																							
Bit 6 D <sub>6</sub>	<b>Timer</b>																																																																																							
Bit 7 D <sub>7</sub>	<b>Timer MSB</b>	<p>If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.</p>																																																																																						
<p>* Note –</p> <p><b>Enabling Times</b></p> <p>The time taken to enable one section (receiver or transmitter) when both sections are initially disabled is 16 bit periods. If one section (receiver or transmitter) is already enabled this time is reduced to "one-half" of a bit period.</p>																																																																																								
<p><b>Tx Enable</b></p> <p>If using the internal Tx Preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occasionally produce a Tx Data Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either:</p> <p>(a) Detecting that the Timer interrupt Status Bit is not set and that it is not appropriate to load Tx data at this time. or,</p> <p>(b) Not using the Timer. i.e. immediately after Tx enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.</p>																																																																																								

**Status Register** $A_1 = 1$  $A_0 = 1$  $A_2 = 1$ **Read Only**

When an interrupt is generated the  $\overline{\text{IRQ}}$  Output goes Low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function	Set = logic '1' (High) Clear = logic '0' (Low)
Bit 0 $D_0$	<b>Rx Data Ready</b>	$D_0$ when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. <b>Set</b> – when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. <b>Bit and Interrupt Cleared</b> – (i) by a read of the Status Register followed by a read of the Rx Data Buffer or (ii) by Rx Enable going Low.	
Bit 1 $D_1$	<b>Rx Checksum True</b>	$D_1$ when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit ( $D_0$ ) is set for the second byte of the received checksum, does not cause an interrupt. <b>Set</b> – by a correct comparison between the received and generated checksums. <b>Cleared</b> – (i) by a read of the Status Register followed by a read of the Rx Data Buffer, or (ii) by Rx Enable going Low.	
Bit 2 $D_2$	<b>Rx Carrier Detect</b>	$D_2$ is a "Real Time" indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When FFSK tones are present at the receiver input this bit goes High, for no FFSK input this bit goes Low. When the Rx Enable bit ( $D_2$ – Control Register) is Low Rx Carrier Detect will go Low.	
Bit 3 $D_3$	<b>Tx Data Ready</b>	$D_3$ when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. <b>Set</b> – (i) when the contents of the Tx Data Buffer are transferred to the Tx Data Register, or (ii) when the Tx Enable is set – No interrupt is generated in this case. <b>Bit Cleared</b> – (i) by a read of the Status Register followed by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. <b>Interrupt Cleared</b> – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.	
Bit 4 $D_4$	<b>Tx Idle</b>	$D_4$ causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. <b>Set</b> – one bit period after the last byte is transmitted. This last byte could be either "checksum" or "loaded data" depending upon the Tx Parity Enable state (Control Register $D_1$ ). <b>Bit Cleared</b> – (i) by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. <b>Interrupt Cleared</b> – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.	
Bit 5 $D_5$	<b>Timer Interrupt</b>	$D_5$ , when set, causes an interrupt to indicate that the set timer period has expired. (Control Register $D_4$ – $D_7$ ). <b>Set</b> – by the timer. <b>Bit and Interrupt Cleared</b> – by a read of the Status Register.	
Bit 6 $D_6$	<b>Rx SYNC Detect *</b>	$D_6$ , when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. <b>Set</b> – on receipt of the 16th bit of a 'SYNC' word. <b>Bit and Interrupt Cleared</b> – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.	
Bit 7 $D_7$	<b>Rx SYNT Detect *</b>	$D_7$ , when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000) has been detected in the received bit stream. <b>Set</b> – on receipt of the 16th bit of a 'SYNT' word. <b>Bit and Interrupt Cleared</b> – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.	

\* Note –

*'SYNC' and 'SYNT' Detection is disabled whilst the checksum checker is running.*

**Rx Data Buffer** $A_1 = 1$  $A_0 = 0$  $A_2 = 1$ 

Read Only

These 8 bits are the last byte of data received with bit 7 being received first. *Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other  $\mu$ Processor peripherals.*

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$
LSB	-	-	-	-	-	-	MSB

**Tx Data Buffer** $A_1 = 1$  $A_0 = 0$  $A_2 = 0$ 

Write Only

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. *Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other  $\mu$ Processor peripherals.* If the Tx Parity Enable bit (Control Register  $D_1$ ) is set, a 2-byte checksum will be inserted and transmitted by the modem after every 6 transmitted "message" bytes.

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$
LSB	-	-	-	-	-	-	MSB

**The Syndrome Word**

This 16-bit word (both Low and High bytes) may be used to correct errors.

Bits  $S_1$  to  $S_{15}$  are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of "received message." For a correct message all 15 bits ( $S_1$  to  $S_{15}$ ) will be zero.

The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register  $D_0$ ) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

**Syndrome Low Byte** $A_1 = 0$  $A_0 = 0$  $A_2 = 1$ 

Read Only

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$
$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$	$S_7$	$S_8$

**Syndrome High Byte** $A_1 = 0$  $A_0 = 1$  $A_2 = 1$ 

Read Only

$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$
$S_9$	$S_{10}$	$S_{11}$	$S_{12}$	$S_{13}$	$S_{14}$	$S_{15}$	PARITY ERROR

$D_7$  – This is a "Parity Error Bit" – Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Thus for a correctly received message all 16 bits of the Syndrome Word ( $S_1$  to  $S_{15}$  and Parity Error) will be zero.

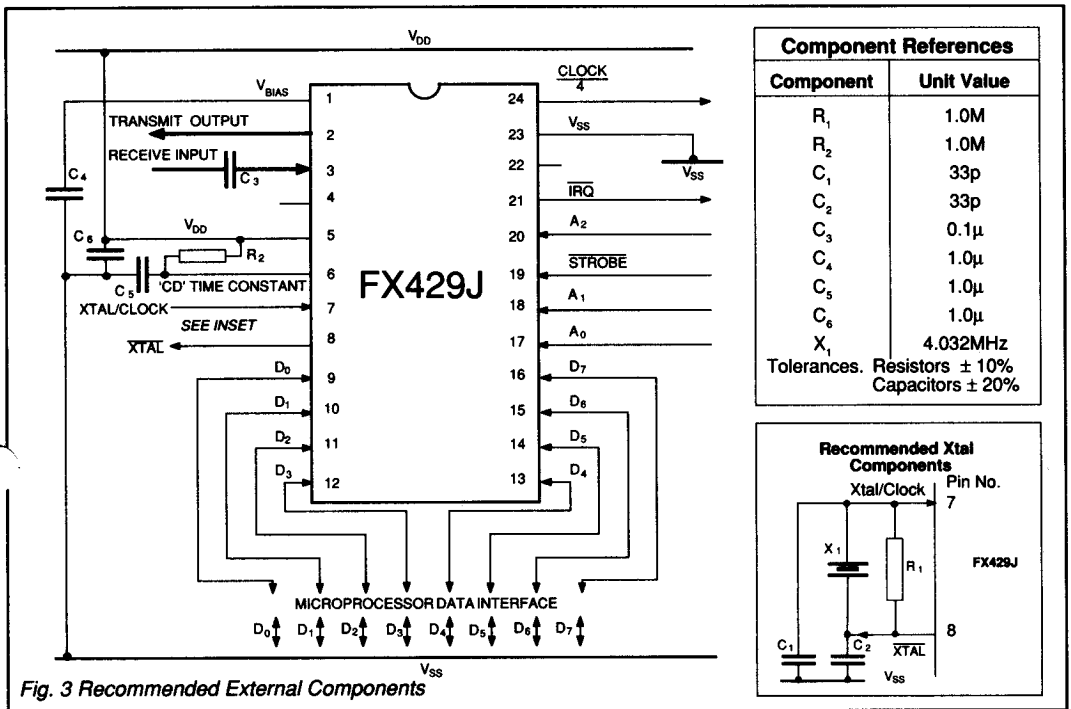


Fig. 3 Recommended External Components

### Carrier Detect Time Constant

The value of the Carrier Detect capacitor,  $C_5$ , determines the carrier detect time constant. A long time constant (larger value  $C_5$ ), results in improved noise immunity but increased response time.  $C_5$  may be varied to optimise noise immunity/reponse time.

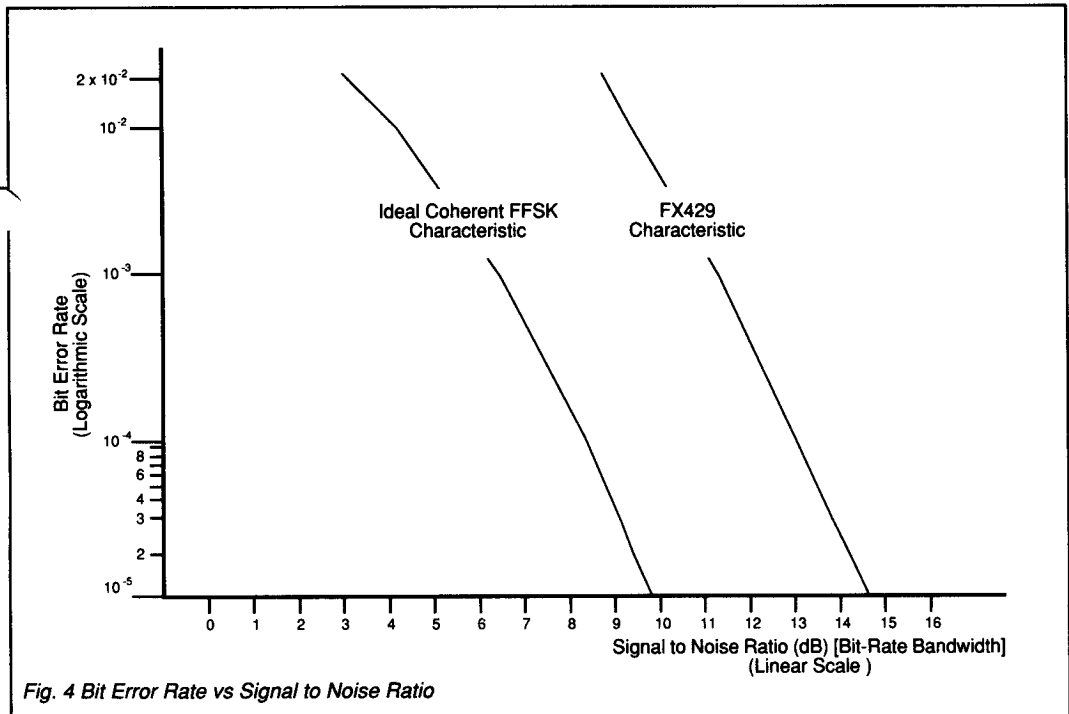
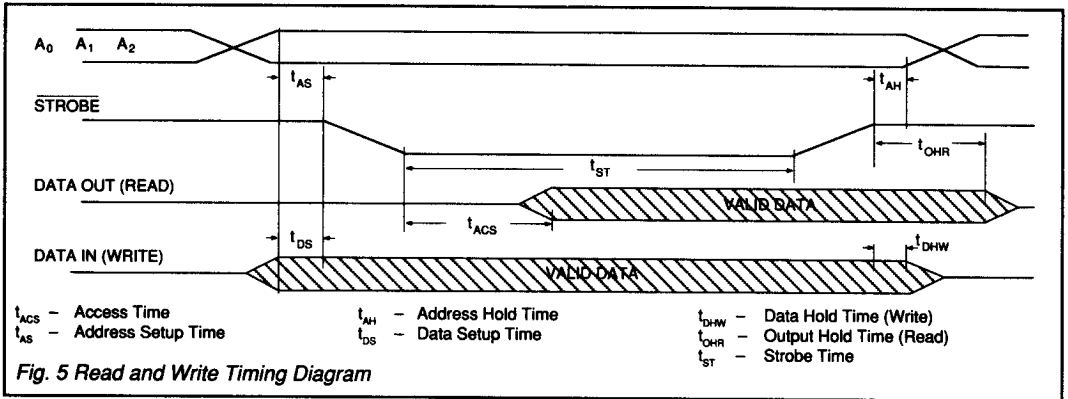
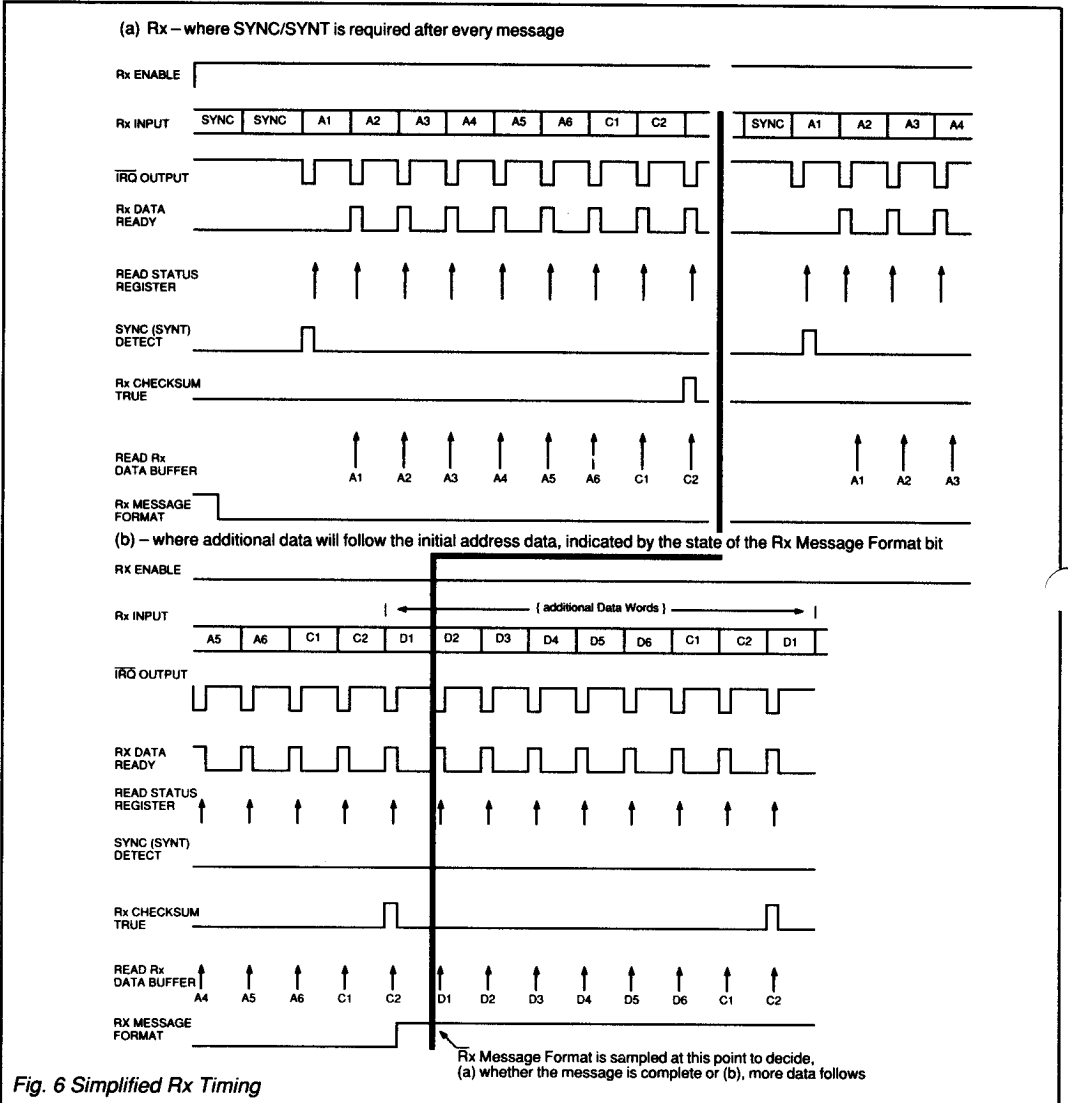


Fig. 4 Bit Error Rate vs Signal to Noise Ratio

# Timing Information



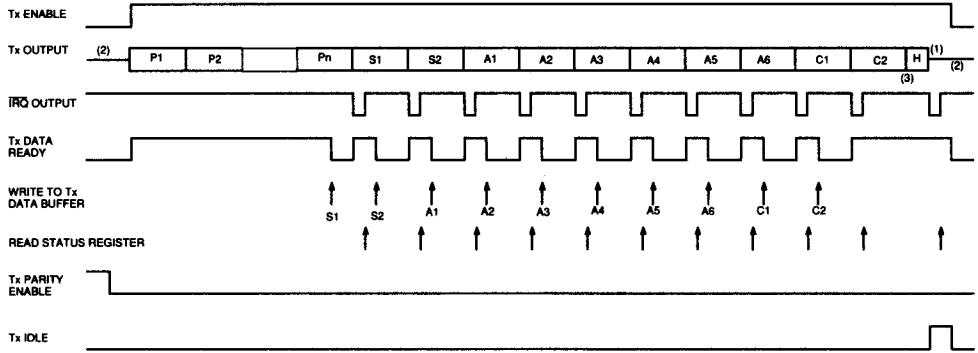
## Operation - Rx



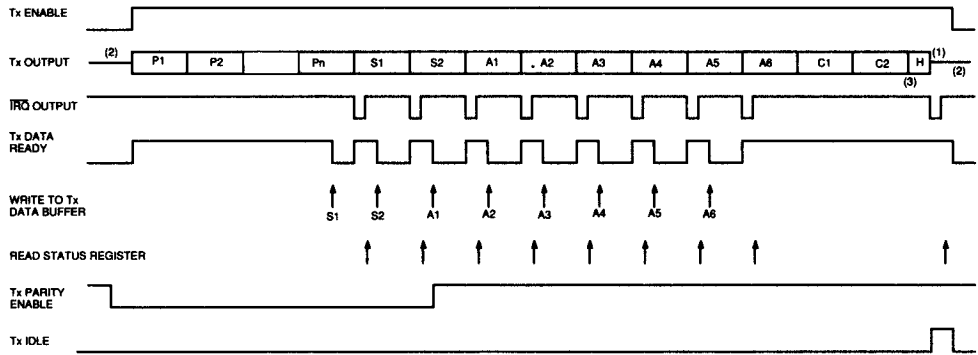


# Operation - Tx

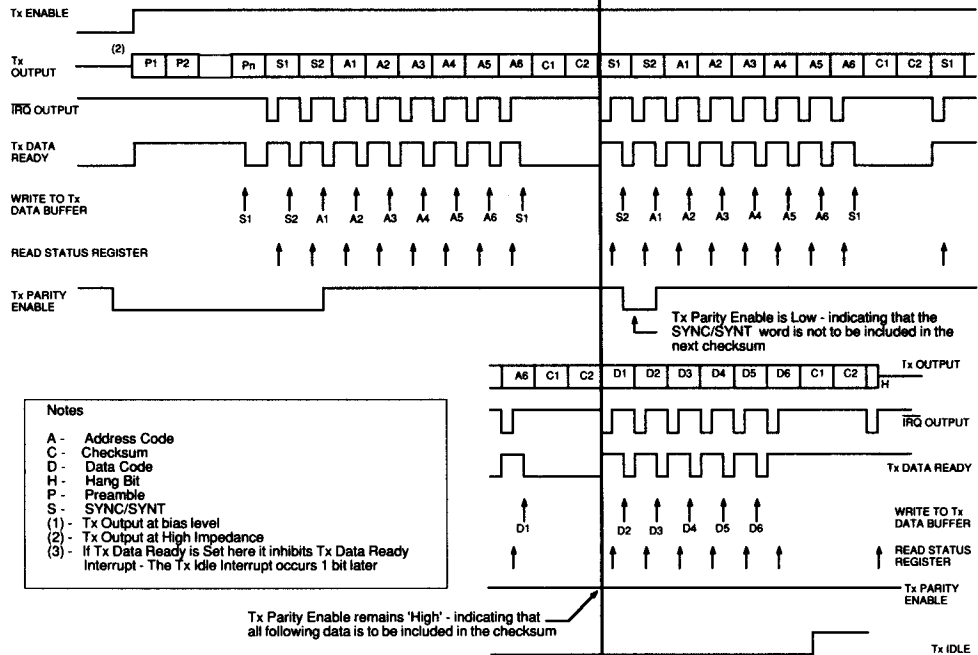
## (a) Tx - one message with checksum supplied by the host



## (b) Tx - one message with checksum generated internally



## (c) Tx - more than one message, with checksum generated internally



### Notes

- A - Address Code
- C - Checksum
- D - Data Code
- H - Hang Bit
- P - Preamble
- S - SYNC/SYNT
- (1) - Tx Output at bias level
- (2) - Tx Output at High Impedance
- (3) - If Tx Data Ready is Set here it inhibits Tx Data Ready Interrupt - The Tx Idle Interrupt occurs 1 bit later

Tx Parity Enable remains 'High' - indicating that all following data is to be included in the checksum

Fig. 7 Simplified Tx Timing

# Basic Power-Up Software

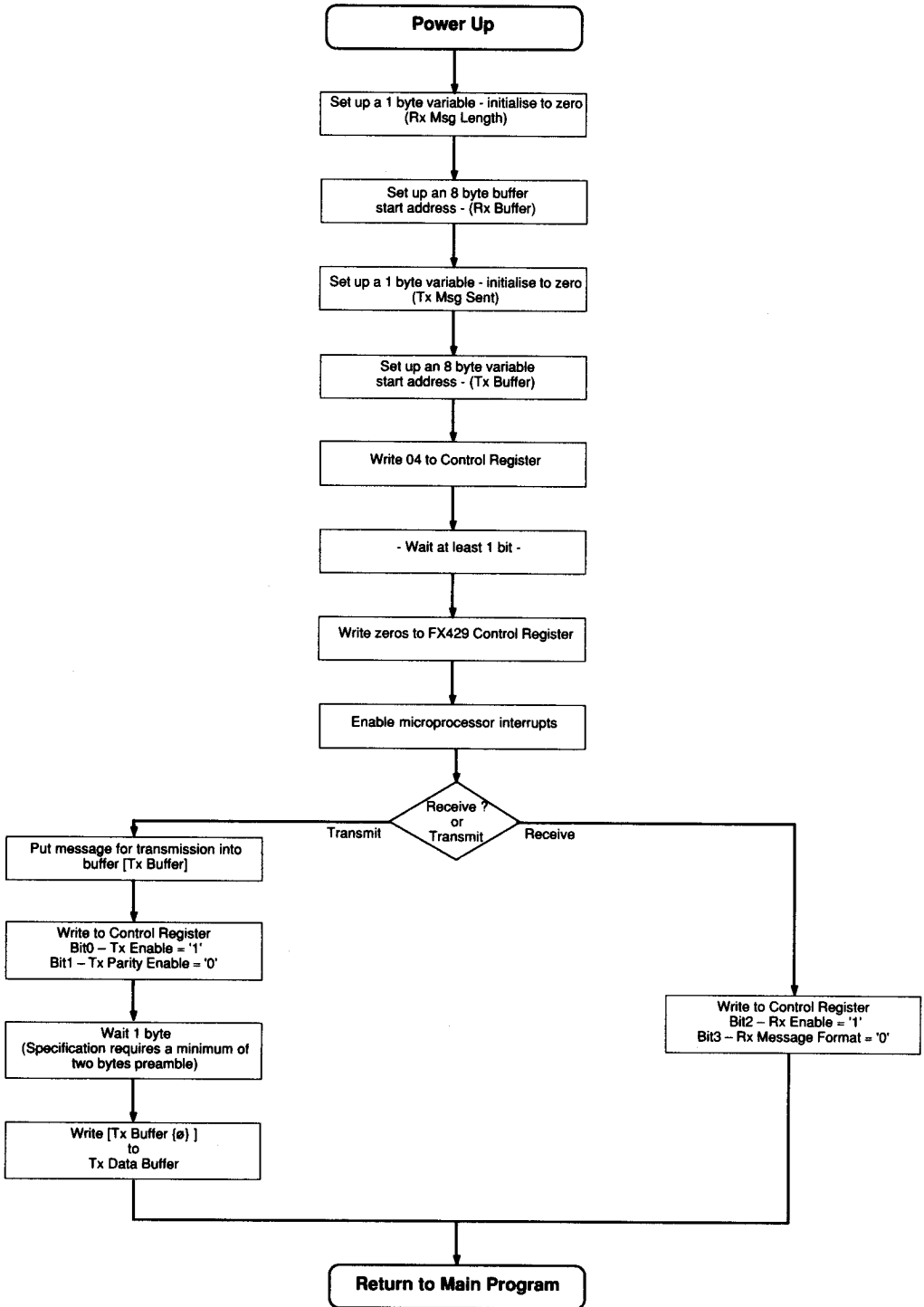


Fig. 8 Power-Up Flow

# Basic Software Interrupt Flow

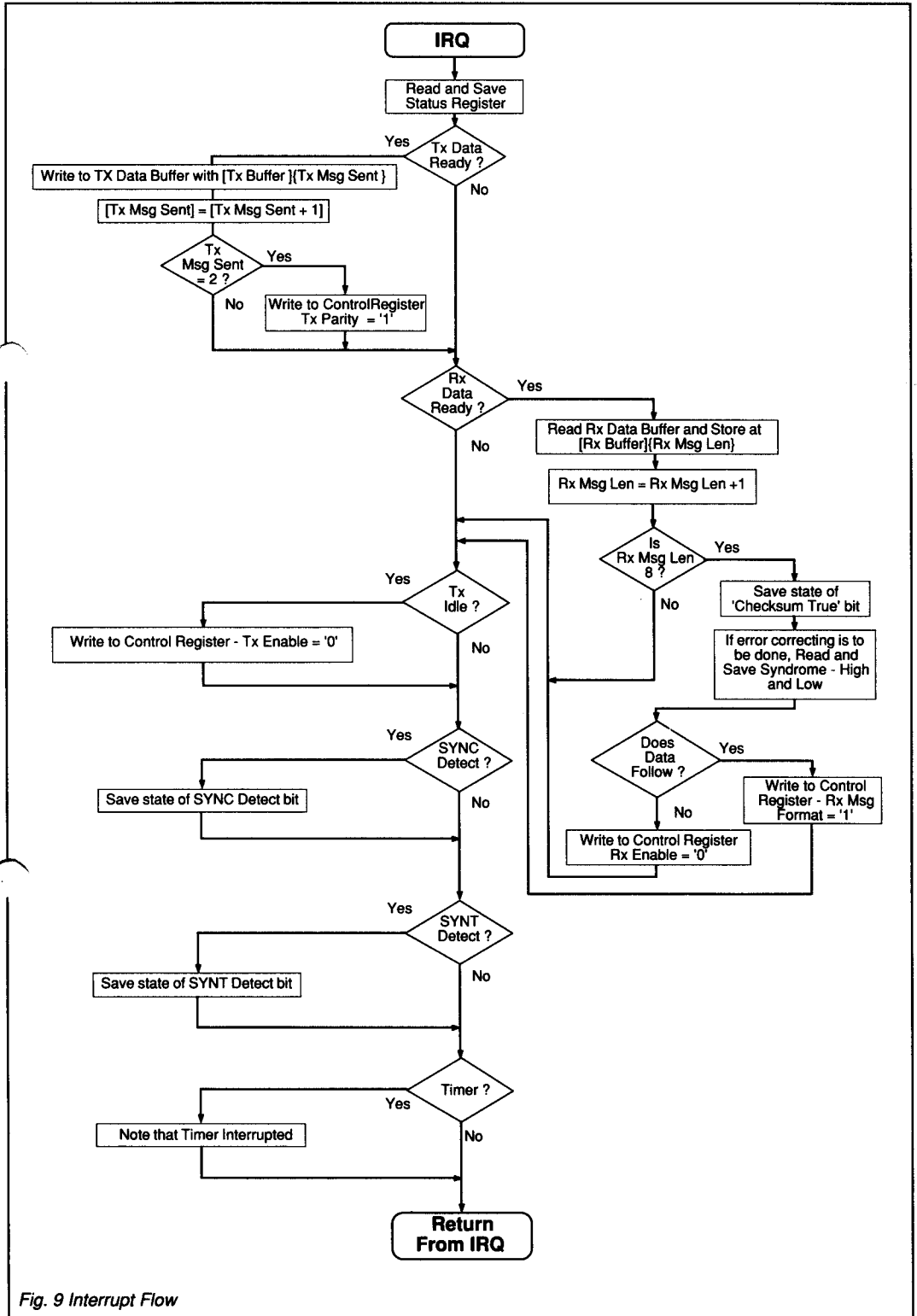


Fig. 9 Interrupt Flow

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$ )		-0.3 to ( $V_{DD} + 0.3V$ )
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ $T_{AMB} = 25^{\circ}C$		800mW Max.
Derating		10mW/ $^{\circ}C$
Operating temperature range:	<b>FX429J</b>	-30 $^{\circ}C$ to +85 $^{\circ}C$ (ceramic)
	<b>FX429LG/LS</b>	-30 $^{\circ}C$ to +70 $^{\circ}C$ (plastic)
Storage temperature range:	<b>FX429J</b>	-55 $^{\circ}C$ to +125 $^{\circ}C$ (ceramic)
	<b>FX429LG/LS</b>	-40 $^{\circ}C$ to +85 $^{\circ}C$ (plastic)

## Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:

$V_{DD} = 5.0V$ ,  $T_{AMB} = 25^{\circ}C$ . Xtal/Clock  $f_0 = 4.032$  MHz. Audio level 0dB ref: = 300mV rms.

Bit Rate Bandwidth = 1200Hz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Values</b>					
Supply Voltage		4.5	-	5.5	V
Supply Current Ranges					
Rx and Tx Enabled		-	-	7.0	mA
Rx Enabled, Tx Disabled		-	4.0	6.0	mA
Rx Disabled, Tx Enabled		-	-	7.0	mA
Rx and Tx Disabled	10	-	1.5	2.5	mA
<b>Dynamic Values</b>					
Modem Internal Delay		-	1.5	-	ms
<b>Interface Levels</b>					
Output Logic '1' Source Current	2	-	-	120	$\mu A$
Output Logic '0' Sink Current	3	-	-	360	$\mu A$
Three State Output Leakage Current		-	-	4.0	$\mu A$
<b>D<sub>0</sub> - D<sub>7</sub>, Data In/Out</b>					
Logic '1' Level	1	3.5	-	-	V
Logic '0' Level		-	-	1.5	V
<b>A<sub>1</sub>, A<sub>0</sub>, A<sub>2</sub>, STROBE, IRQ</b>					
Logic '1' Level	4	4.0	-	-	V
Logic '0' Level		-	-	1.0	V
<b>Analogue Impedances</b>					
Rx Input		100	-	-	k $\Omega$
Tx Output (Enabled)		-	10	-	k $\Omega$
Tx Output (Disabled)		-	5	-	M $\Omega$
<b>On-Chip Xtal Oscillator</b>					
$R_{IN}$		10	-	-	M $\Omega$
$R_{OUT}$	5	5.0	-	15	k $\Omega$
Oscillator Gain		-	15	-	dB
Xtal frequency		-	4.032	-	MHz
<b>Timing - (Fig. 5)</b>					
Access Time	- ( $t_{ACS}$ )	-	-	135	ns
Address Hold Time	- ( $t_{AH}$ )	0	-	-	ns
Address Set-up Time	- ( $t_{AS}$ )	0	-	-	ns
Data Hold Time (Write)	- ( $t_{DHW}$ )	85	-	-	ns
Data Set-up Time (Write)	- ( $t_{DS}$ )	0	-	-	ns
Output Hold Time (Read)	- ( $t_{OHR}$ )	15	-	105	ns
Strobe Time	- ( $t_{ST}$ )	140	-	-	ns

# Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Dynamic Values.....</b>					
<b>Receiver</b>					
Signal Input Levels	6	-9.0	-2.0	+10.5	dB
Bit Error Rate	7				
@ 12dB Signal/Noise Ratio		-	7.0	-	10 <sup>-4</sup>
@ 20dB Signal/Noise Ratio		-	1.0	-	10 <sup>-8</sup>
Synchronization @ 12dB Signal/Noise Ratio	8				
Probability of Bit16 being correct		-	99.5	-	%
Carrier Detect Response Time	8	-	13.0	-	ms
<b>Transmitter</b>					
Output Level		-	8.25	-	dB
Output Level Variation		-1.0	-	+1.0	dB
Output Distortion		-	3.0	5.0	%
3rd Harmonic Distortion		-	2.0	3.0	%
Logic '1' Frequency	9	-	1200	-	Hz
Logic '0' Frequency	9	-	1800	-	Hz
Isochronous Distortion					
1200Hz – 1800Hz		-	25	40	µs
1800Hz – 1200Hz		-	20	40	µs

## Notes

1. With each data line loaded as, C = 50pf and R = 10kΩ.
2. V<sub>OUT</sub> = 4.6V.
3. V<sub>OUT</sub> = 0.4V
4. Sink/Source currents ≤ 0.1mA.
5. Both Xtal and Xtal + 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 3, Bit Error Rate.
8. This Response Time is measured using a 10101010101....01 pattern input signal at a level of 230mV rms (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.
10. Powersave is only active when both Rx and Tx functions are disabled.

## Checksum Generation and Checking

**Generation** – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo-2, by the generating polynomial:-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16-bit word is used as the "Checksum."

**Checking** – The checksum checker does two things:

It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo-2, by the generating polynomial:-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.

Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).

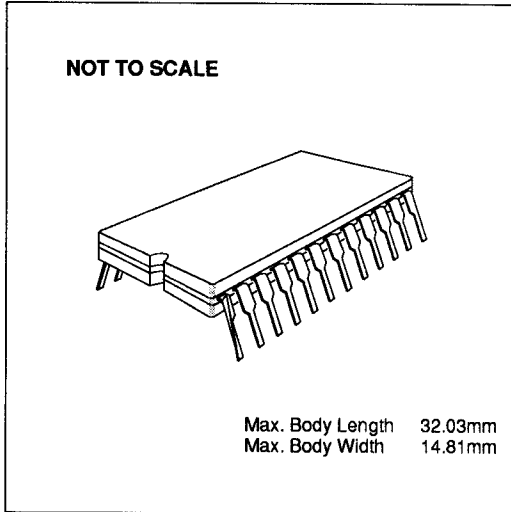
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR D<sub>i</sub>) bit is set.

## Package Outlines

The FX429 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.

Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

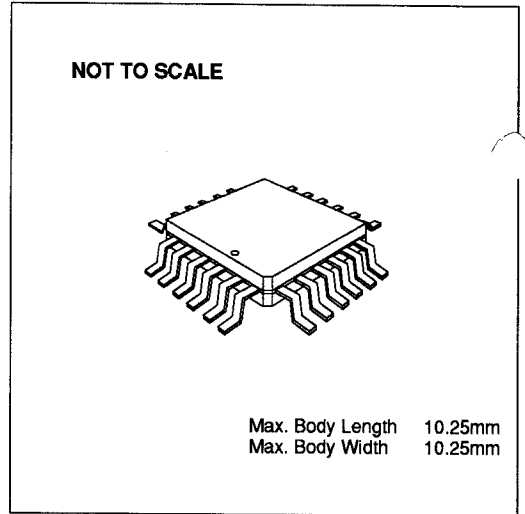
**FX429J** 24-pin cerdip DIL (J4)



## Handling Precautions

The FX429 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

**FX429LG** 24-pin quad plastic encapsulated bent and cropped (L1)



## Ordering Information

**FX429J** 24-pin cerdip DIL (J4)

**FX429LG** 24-pin quad plastic encapsulated bent and cropped (L1)

**FX429LS** 24-lead plastic leaded chip carrier (L2)

**FX429LS** 24-lead plastic leaded chip carrier (L2)

