CMD

G65SC22

Microcircuits

CMOS Versatile Interface Adapter With Interval Timer/Counters

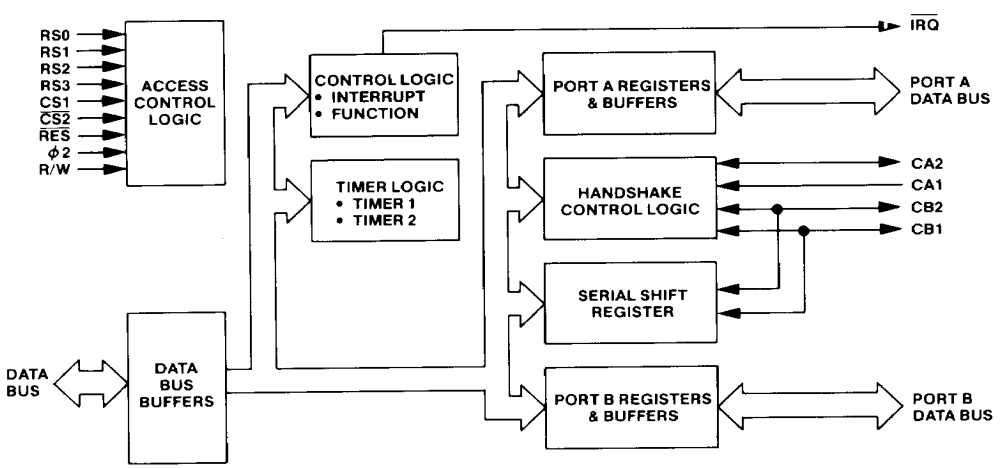
Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6522 devices
- Low power consumption allows battery-powered operation (2 mA at 1 MHz)
- Two 8-bit, bidirectional peripheral I/O Ports
- Two powerful 16-bit programmable Timer/Counters
- Serial bidirectional peripheral I/O Port
- Enhanced "handshake" feature
- Latched Input/Output Registers on both I/O Ports
- Programmable Data Direction Registers
- Six operating frequencies—1, 2, 3, 4, 5 and 6 MHz
- TTL compatible I/O peripheral lines
- Single +5 volts power supply
- Available in 40-pin dual-in-line or 44-pin PLCC package

General Description

The CMD G65SC22 Versatile Interface Adapter (VIA) is a flexible I/O device for use with the CMD G65SCXXX series 8-bit microprocessor family. The G65SC22 includes functions for programmed control of up to two peripheral devices (Ports A and B). Two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capacity. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on a individual line basis. Also provided are two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including — an Interrupt Flag Register, an Interrupt Enable Register and two Function Control Registers.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0-RS3, CS1, $\overline{CS2}$, CA1, ϕ2	I_{IN}		±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IL}		-1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz	I_{DD}		2.0	mA
f = 2 MHz	I_{DD}		4.0	mA
f = 3 MHz	I_{DD}		6.0	mA
f = 4 MHz	I_{DD}		8.0	mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz)	P_D		11.0	mW
Standby (Static)	P_{DSB}		100	μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ±5%, V_{SS} = 0V, T_A = 40° to +85° C Industrial, 0° C to + 70° C Commercial

		G65Sc22-1		G65SC22-2		G65SC22-3		G65SC22-4		C65SC22-5		G65SC22-6		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	200	—	167	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	90	—	80	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	90	—	80	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	—	10	—	10	nS
Read Timing (Figure 2)														
Select, R/$\overline{W}$	t_{ACR}	160	—	90	—	65	—	45	—	40	—	35	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	150	—	130	—	75	—	70	—	65	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	65	—	60	—	nS
Write Timing (Figure 3)														
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	40	—	35	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	75	—	65	—	45	—	40	—	35	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	10	10	5	—	nS
Peripheral Data Delay (Port A)	t_{CPW}	—	1000	—	500	—	330	—	250	—	167	—	125	nS
(Port B)		—	1000	—	500	—	330	—	250	—	167	—	125	nS

AC Characteristics—Peripheral Interface Timing: V_{DD} =5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial.

(See Figures 4 through 12)

Parameter	Symbol	Min	Max	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	tR, tF	—	1.0	μS	—
Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)	tCA2	—	1.0	μS	4,5
Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)	tRS1	—	1.0	μS	4
Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)	tRS2	—	2.0	μS	5
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	tWHS		1.0	μS	6,7
Delay Time, Peripheral Data Valid to CA2 or CB2 Negative Transition	tDS	40	—	nS	6,7
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)	tRS3	—	1.0	μS	6
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)	tRS4	—	2.0	μS	7
Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	t21	400	—	nS	7
Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	tIL	300	—	nS	8
Shift-Out Delay Time—Time from $\phi 2$ Falling Edge to CB2 Data Out	tSR1	—	300	nS	9
Shift-In Set-up Time—Time from CB2 Data In to $\phi 2$ Rising Edge	tSR2	300	—	nS	10
External Shift Clock (CB1) Set-up Time Relative to $\phi 2$ Trailing Edge	tSR3	100	tCYC	nS	10
Pulse Width—PB6 Input Pulse	tIPW	2 x tCYC	—		12
Pulse Width—CB1 Input Clock	tICW	2 x tCYC	—		11
Pulse Spacing—PB6 Input Pulse	tIPS	2 x tCYC	—		12
Pulse Spacing—CB1 Input Pulse	tICS	2 x tCYC	—		11
CA1, CB1 Set Up Prior to Transition to Arm Latch	tAL	300	—	nS	8
Peripheral Data Hold After CA1, CB1 Transition	tPDH	150	—	nS	8

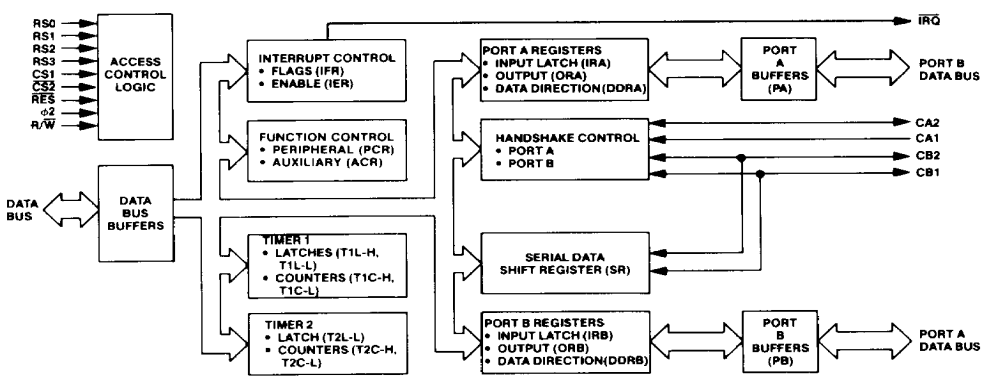


Figure 1. Functional Block Diagram

Timing Diagrams: Measurement points 0.8.V and 2.0V unless otherwise specified.

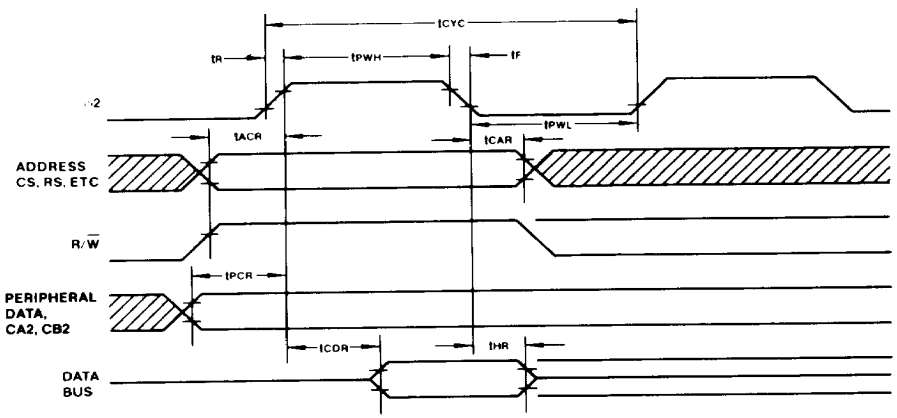


Figure 2. Read Timing

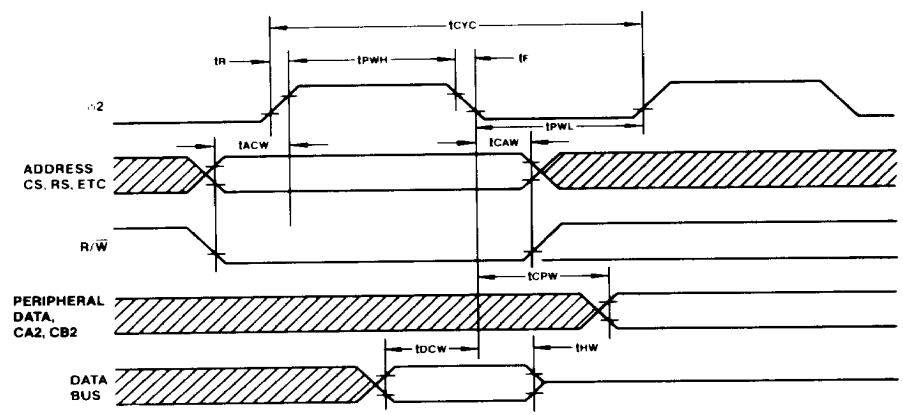


Figure 3. Write Timing

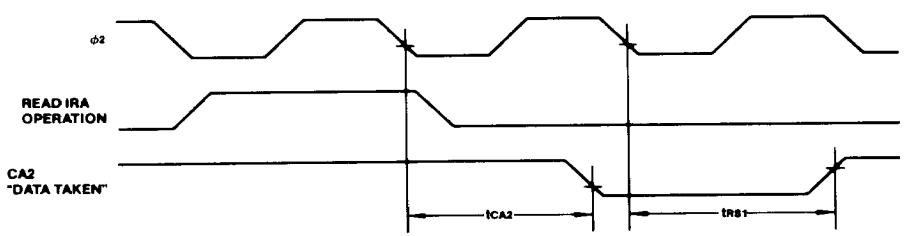


Figure 4. Read Handshake, Pulse Mode Timing (CA2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

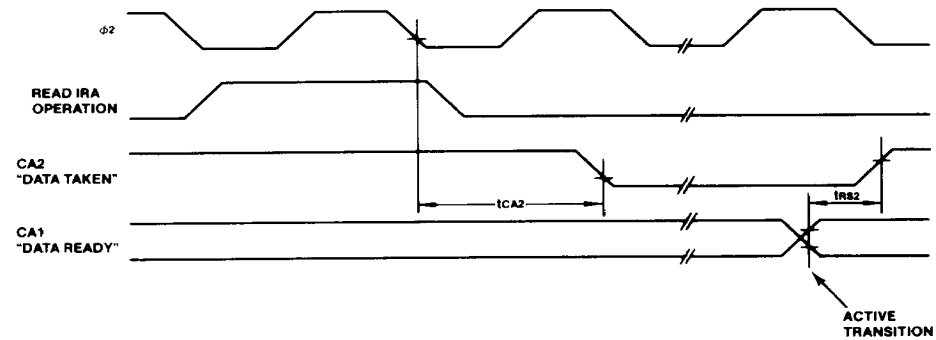


Figure 5. Read Handshake, Handshake Mode Timing (CA2)

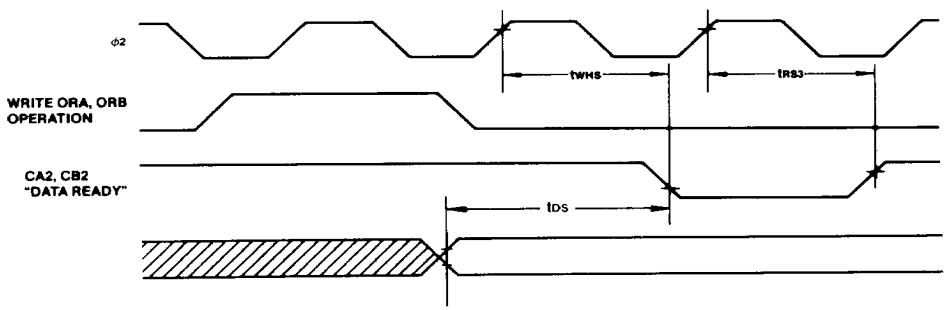


Figure 6. Write Handshake, Pulse Mode Timing (CA2, CB2)

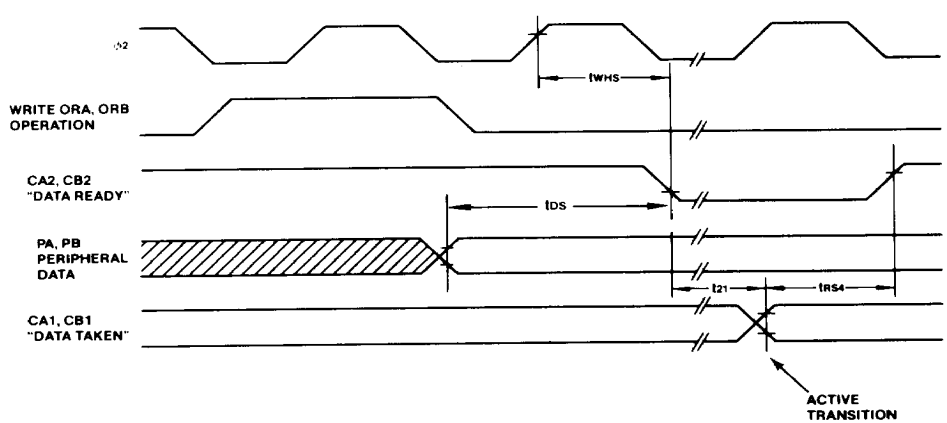


Figure 7. Write Handshake, Handshake Mode Timing (CA2, CB2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

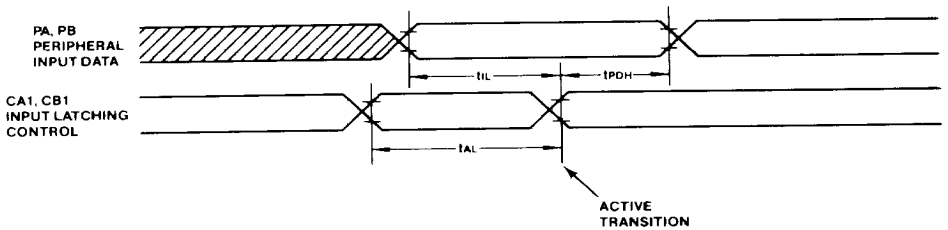


Figure 8. Peripheral Data, Input Latching Timing

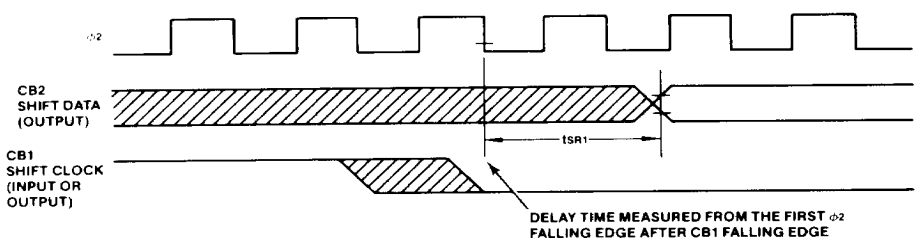


Figure 9. Data Shift Out, Internal or External Shift Clock Timing

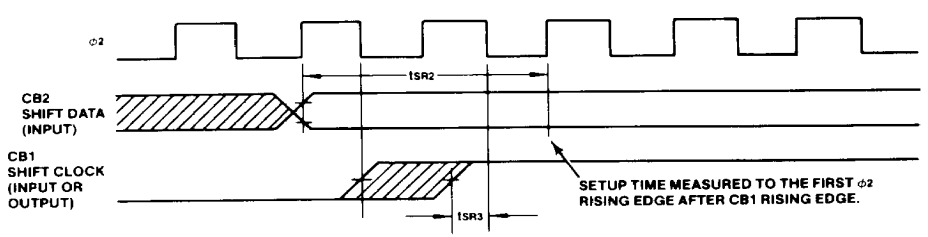


Figure 10. Data Shift In, Internal or External Shift Clock Timing

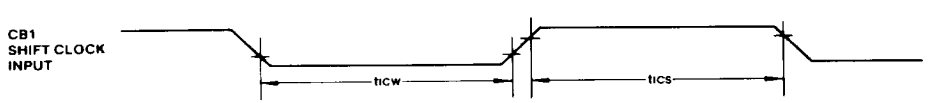


Figure 11. External Shift Clock Timing

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

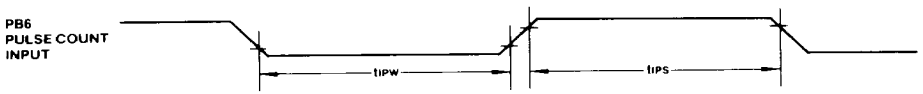


Figure 12. Pulse Count Input Timing

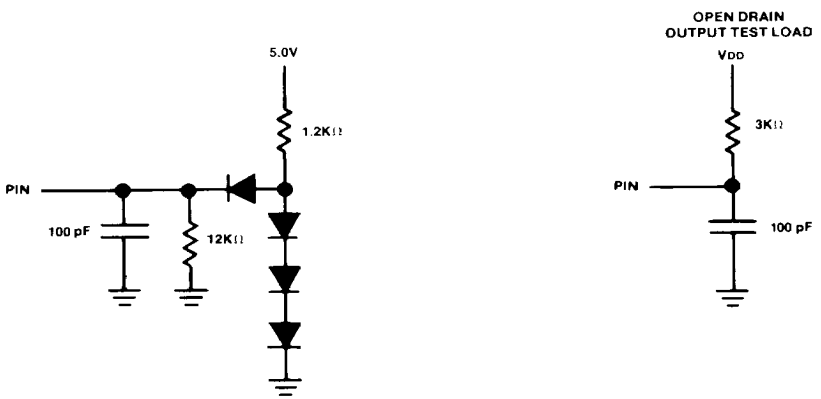


Figure 13. Test Load

Signal Description

Reset ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

Input Clock ($\phi 2$)

The system $\phi 2$ Input Clock controls all data transfers between the G65SC22 and the microprocessor.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the G65SC22 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC22 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC22 register (Write operation). Read/Write must always be preceded by a proper Chip Select (CS1, $\overline{CS2}$).

Data Bus (D0-D7)

The eight bidirectional Data Bus lines are used to transfer data between the G65SC22 and the microprocessor. During a Read operation, the contents of the selected G65SC22 internal register are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected G65SC22 register. The Data Bus lines are in the high impedance state when the G65SC22 is unselected.

Chip Select (CS1, $\overline{CS2}$)

Normally, the two Chip Select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected G65SC22 register, CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0-RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the G65SC22. Refer to Table 1 for Register Select coding and a functional description.

Interrupt Request ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated (Logic 0) whenever an internal Interrupt Flag bit is set (Logic 1) and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Table 1. G65SC22 Internal Registers

Register Number	RS Coding				Register Designation	Description	
	RS3	RS2	RS1	RS0		Write ($R/\overline{W} = 0$)	Read ($R/\overline{W} = 1$)
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same As Reg 1 Except No "Handshake"	

Peripheral Data Port A (PA0-PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the G65SC22's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 14.

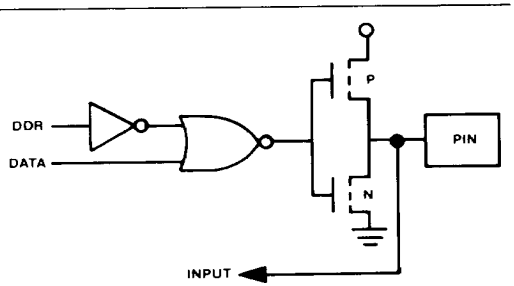


Figure 14. Port A Buffer Circuit (PA0-PA7, CA2)

Peripheral Data Port A Control Lines (CA1, CA2)
Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

Peripheral Data Port B (PB0-PB7)
Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 3.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 15.

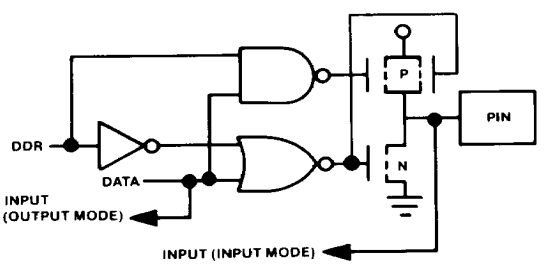


Figure 15. Port B Buffer Circuit (PB0-PB7, CB1, CB2)

Peripheral Data Port B Control Lines (CB1, CB2)
Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.

Functional Description

Peripheral Data Ports (Port A, Port B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA & ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) is transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates similar to Input Register A except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of Input Register A to result in the reading of a Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 16, 17 and 18. It should be noted that the input latching modes are controlled by the Auxiliary Control Register (See Figure 24).

Data Transfer—Handshake Control

A powerful feature of the G65SC22 is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

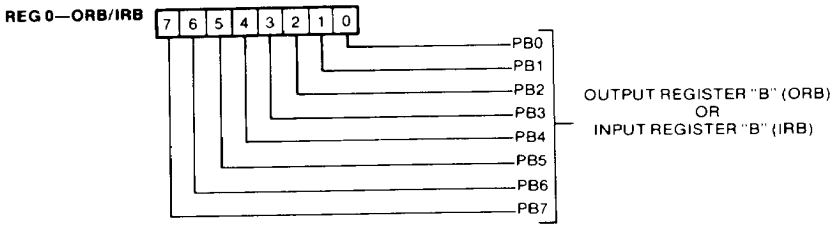
Read Handshake Control

Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the G65SC22 which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figure 19 for Read Handshake timing and operating sequence.

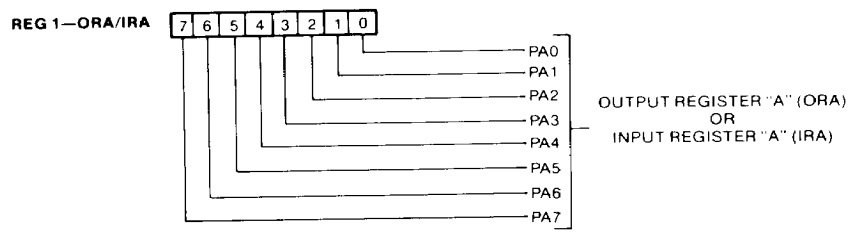
Write Handshake Control

The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the G65SC22 generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Refer to Figure 20 for Write Handshake timing and operating sequence. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1 and CB2) is accomplished by the Peripheral Control Register (PCR). See Figure 21.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect.
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 16. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 17. Output Register A (ORA), Input Register A (IRA)

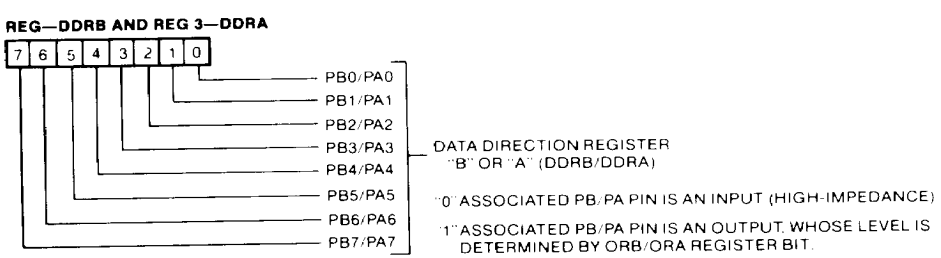


Figure 18. Data Direction Registers (DDRB, DDRA)

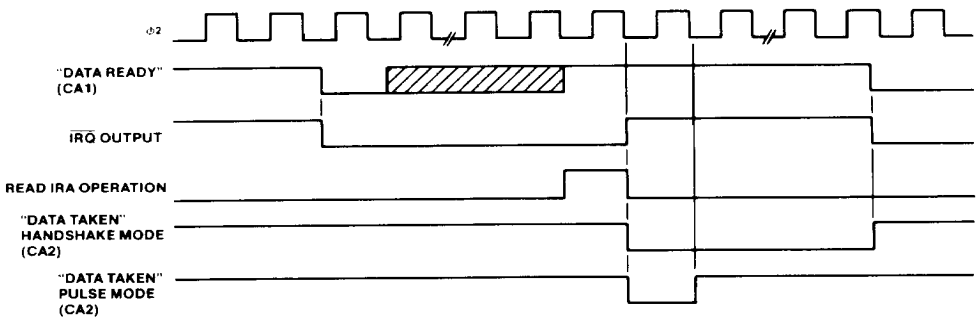


Figure 19. Read Handshake (Port A Only)

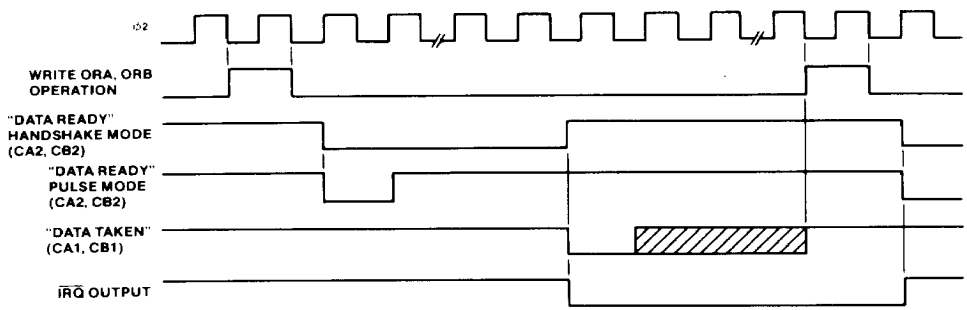


Figure 20. Write Handshake (Ports A and B)

REG 12—PERIPHERAL CONTROL REGISTER

7	6	5	4	3	2	1	0

CB2 CONTROL

7	6	5	Operation
0	0	0	Input-negative active edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

CB1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA2 CONTROL

3	2	1	Operation
0	0	0	Input-negative active edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

*See Note Accompanying Figure 37.

Figure 21. CA1, CA2, CB1, CB2 Control

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 ($\phi 2$) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request ($\overline{IRQ}$) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may also be programmed to invert the output signal on PB7 each time it reaches a count of zero. Each of these counter modes is presented below. The T1 counter format and operation is shown in Figure 22, with corresponding latch format and operation in Figure 23. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer T1 operating modes. The four available modes are shown in Figure 24.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode

Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port line PB7.

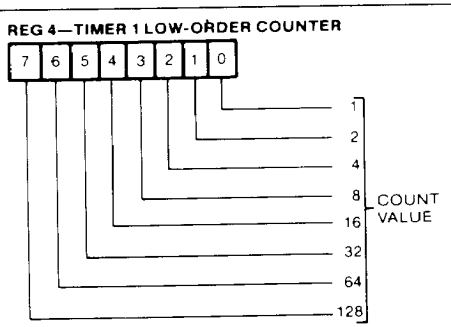
To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next $\phi 2$ clock following the load sequence into T1C-H, and will decrement at the $\phi 2$ clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count.

Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L. Refer to Figure 25 for One-Shot Mode timing information.

Timer 1 Free-Run Mode

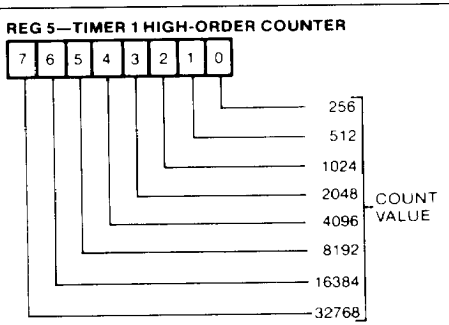
An important advantage within the G65SC22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers to contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated. Refer to Figure 26 for timing information on the Free-Run Mode.



WRITE—8 bits loaded into T1 low-order latches. Latch contents are transferred into low-order counter at the time the high-order counter is loaded (Reg. 5).

READ—8 bits from T1 low-order counter transferred to MPU. In addition, T1 interrupt flag is reset (bit 6 in interrupt flag register)

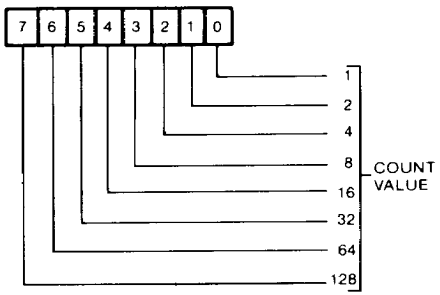


WRITE—8 bits loaded into T1 high-order latches. Also, at this time both high and low-order latches transferred into T1 counter, and initiates countdown. T1 interrupt flag also is reset

READ—8 bits from T1 high-order counter transferred to MPU.

Figure 22. T1 Counter Format and Operation

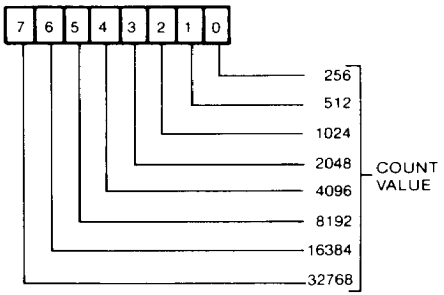
REG 6—TIMER 1 LOW-ORDER LATCHES



WRITE—8 bits loaded into T1 low-order latches. This operation is no different than a write into Reg. 4.

READ—8 bits from T1 low-order latches transferred to MPU. Unlike Reg. 4 operation, this does not cause reset of T1 interrupt flag.

REG 7—TIMER 1 HIGH-ORDER LATCHES

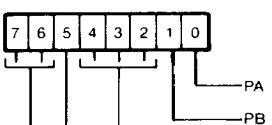


WRITE – 8 bits loaded into T1 high-order latches. Unlike Reg. 4 operation no latch-to-counter transfers take place. T1 interrupt flag is reset.

READ – 8 bits from T1 high-order latches transferred to MPU.

Figure 23. T1 Latch Format and Operation

REG 11—AUXILIARY CONTROL REGISTER



T1 TIMER CONTROL

7	6	Operation	PB7
0	0	Timed interrupt each time T1 is loaded	Disabled
0	1	Continuous interrupts	
1	0	Timed interrupt each time T1 is loaded	One shot output
1	1	Continuous interrupts	Square wave output

T2 TIMER CONTROL

5	Operation
0	Timed interrupt
1	Count down with pulses on PB6

LATCH ENABLE/DISABLE

0 = Disable
1 = Enable Latching

SHIFT REGISTER CONTROL

4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk.
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk.

Figure 24. Auxiliary Control Register Format and Operation

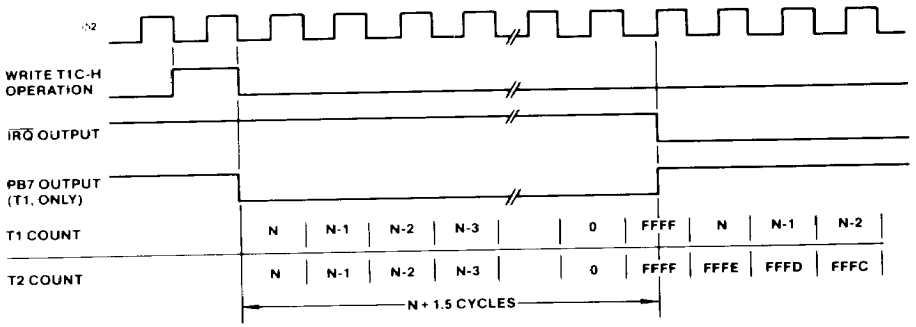
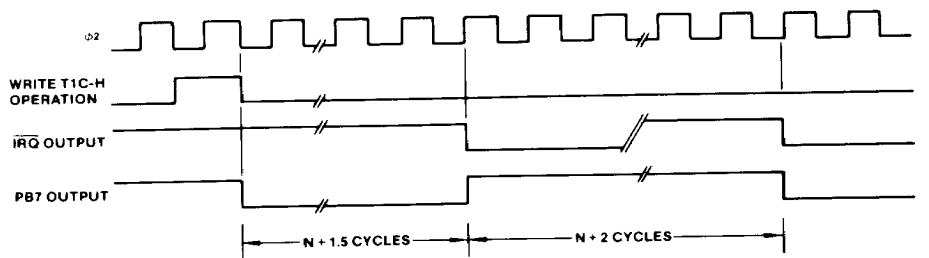


Figure 25. One-Shot Mode (Timer 1 and Timer 2)



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 26. Free-Run Mode (Timer 1)

Timer 2 Operation

Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for counting negative pulses on Data Port line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a $\phi 2$ clock rate. Refer to Figure 27 for T2 counter format and operation.

Timer 2 One-Shot Mode

Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1s ($FFFF_{16}$) and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H. Refer to Figure 25 for timing information on the One-Shot Mode.

Timer 2 Pulse Counting Mode

In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the $\phi 2$ clock. Refer to Figure 28 for timing information.

Shift Register Operation

The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line from an external source, or (with proper mode selection) shift pulses may be generated internally which will appear on the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register. Refer to Figure 29 for format and control bit information. Also refer to Figures 30 through 36 for operation of the various Shift Register modes.

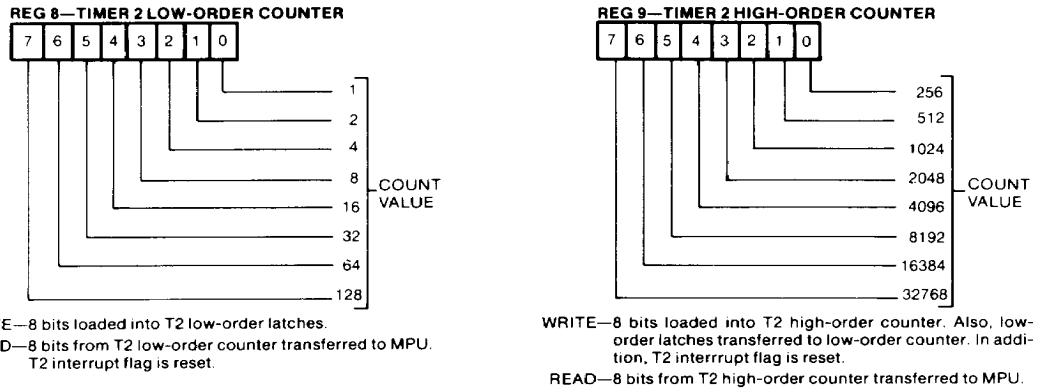


Figure 27. T2 Counter Format and Operation

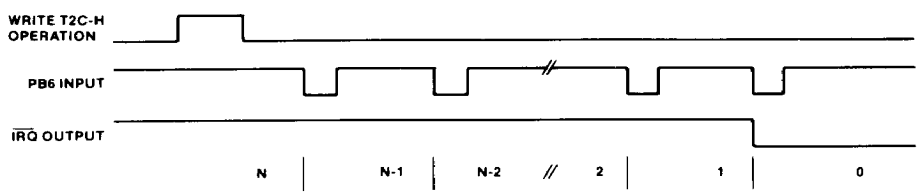


Figure 28. Pulse Counting Mode (Timer 2)

Shift Register Input Modes

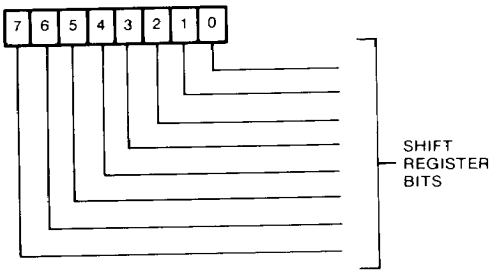
Shift Register Disabled (000)—In the 000 mode, the Shift Register is disabled from all operation. The microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In—Counter T2 Control (001)—In this mode, the shifting rate is controlled by the low order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the $\phi 2$ clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set and $\overline{IRQ}$ will go low (Logic 0). Refer to Figure 30.

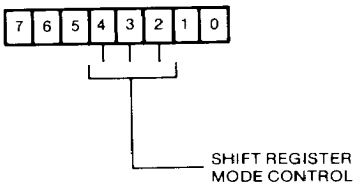
Shift In—$\phi 2$ Clock Control (010)—In this mode, the shift rate is controlled by the $\phi 2$ clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low order bit first, and is then shifted into the next higher order bit on the trailing edge of the $\phi 2$ clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set, and output clock pulses on the CB1 line will stop. Refer to Figure 31.

Shift In—External CB1 Clock Control (011)—In this mode, CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first $\phi 2$ clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Refer to Figure 32.

REG 10—SHIFT REGISTER



REG 11—AUXILIARY CONTROL REGISTER



4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk

Notes:
1. When shifting out, bit 7 is the first bit out and simultaneously is rotated back into bit 0.
2. When shifting in, bits initially enter bit 0 and are shifted towards bit 7.

Figure 29. Shift Register and Auxiliary Control Register Control Bits

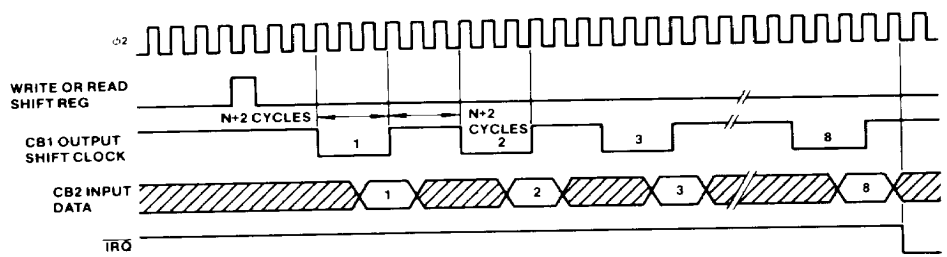


Figure 30. Shift In—Counter T2 Control

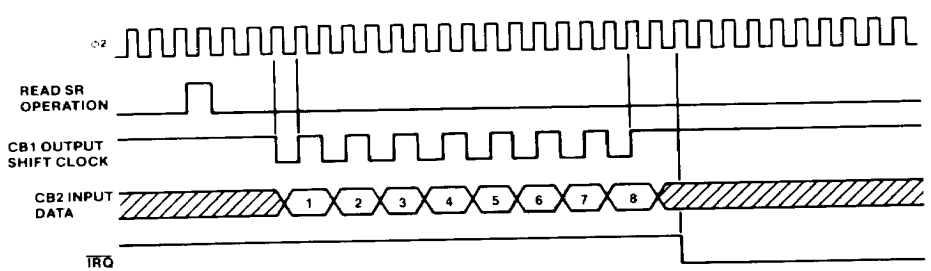


Figure 31. Shift In—$\phi 2$ Clock Control

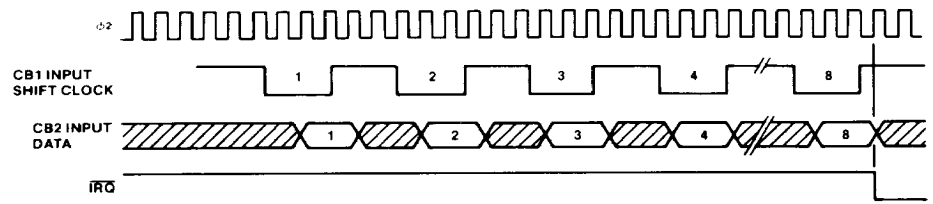


Figure 32. Shift In—External CB1 Clock Control

Shift Register Output Modes

Shift Out—Free Running at T2 Rate (100)—This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CB2 line repetitively. In this mode, the Shift Register Counter is disabled and $\overline{IRQ}$ is never set. Refer to Figure 33.

Shift Out—T2 Control (101)—In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level. Refer to Figure 34.

Shift Out—ϕ2 Clock Control (110)—In this mode, the shift rate is controlled by the system ϕ2 Clock. Refer to Figure 35.

Shift Out—External CB1 Clock Control (111)—In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data. Refer to Figure 36.

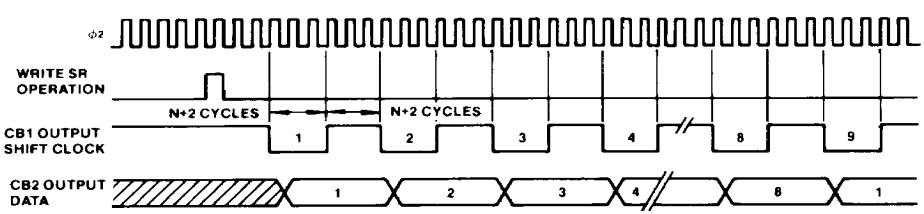


Figure 33. Shift Out—Free Running T2 Rate

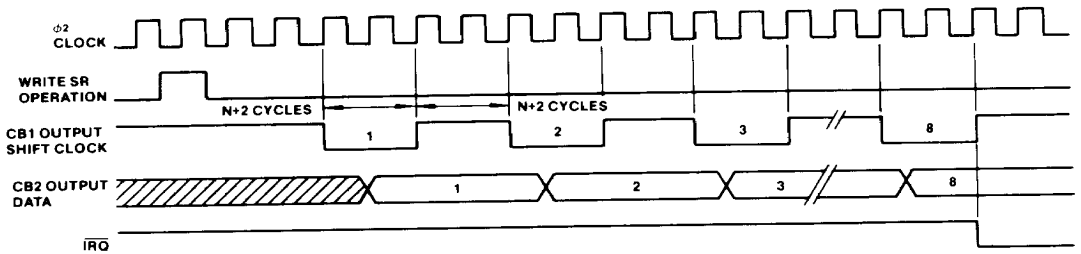


Figure 34. Shift Out—T2 Control

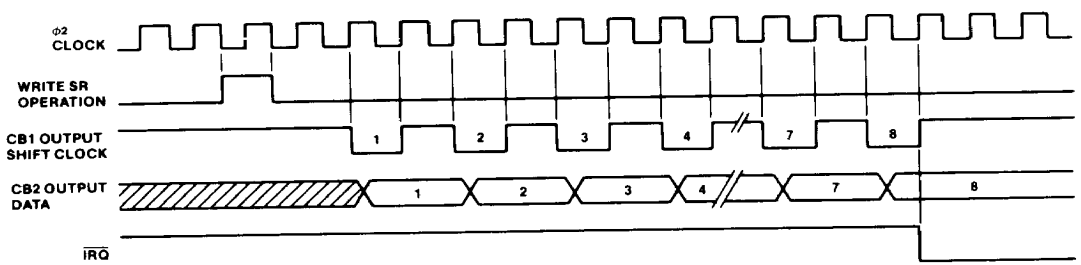


Figure 35. Shift Out—Φ2 Control

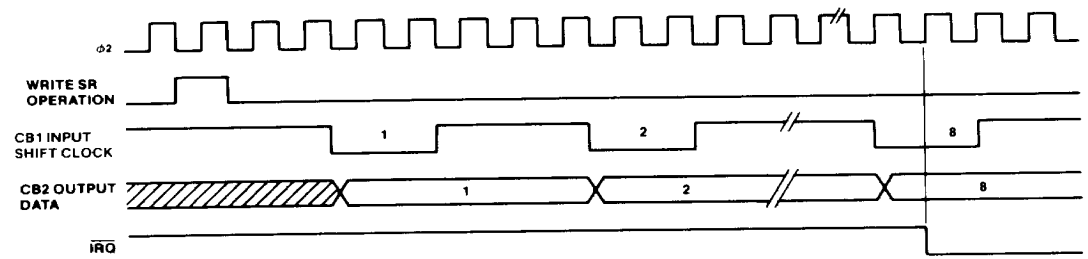


Figure 36. Shift Out—External CB1 Clock Control

Interrupt Operation

There are three basic interrupt operations, including: setting the interrupt flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request ($\overline{IRQ}$). An Interrupt Flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag will remain set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request ($\overline{IRQ}$) will go low (Logic 0). $\overline{IRQ}$ is an open-collector output which can be wire-ORed with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

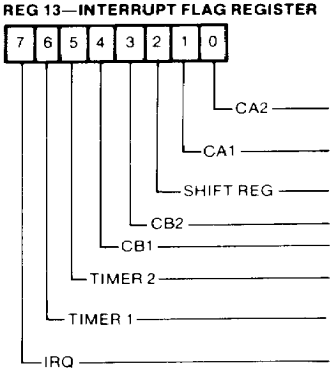
The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 37 and 38 respectively. The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request ($\overline{IRQ}$) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: x = Logic AND, + = Logic OR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts as presented in the next section.

Each Interrupt Flag within the IFR has a corresponding enable bit in the Interrupt Enable Register (IER). The microprocessor can set or clear selected bits within the IER. This allows the control of individual interrupts without affecting others. To set or clear a particular Interrupt Enable bit, the microprocessor must write to address 1110 (IER address). During this write operation, if bit 7 on the Data Bus is a "0", each "1" in bits 6 thru 0 will clear the corresponding bit in the Interrupt Enable Register. For each "0" in bits 6 thru 0, the corresponding bit in the IER will be unaffected.

Setting selected bits in the IER is accomplished by writing to the same address with bit 7 on the Data Bus set to a "1". In this case, each "1" in bits 6 thru 0 will set the corresponding bit to a "1". For each "0", the corresponding bit will be unaffected. This method of controlling the bits in the Interrupt Enable Register allows convenient user control of interrupts during system operation. The microprocessor can also read the contents of the IER by placing the proper address on the Register Select and Chip Select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a "1".

REG 13—INTERRUPT FLAG REGISTER

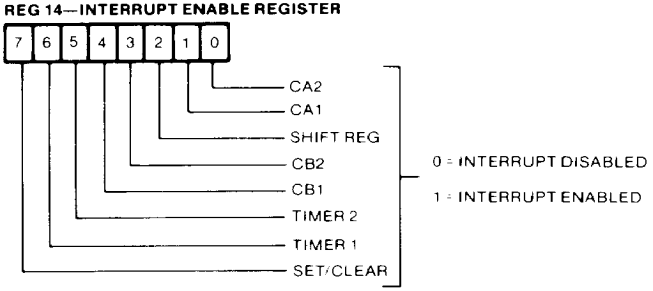


	SET BY	CLEARED BY
CA2	CA2 active edge	Read or write Reg. 1 (ORA)*
CA1	CA1 active edge	Read or write Reg. 1 (ORA)
SHIFT REG	Complete 8 shifts	Read or write Shift Reg.
CB2	CB2 active edge	Read or write ORB*
CB1	CB1 active edge	Read or write ORB
TIMER 2	Time-out of T2	Read T2 low or write T2 high
TIMER 1	Time-out of T1	Read T1 low or write T1 high
IRQ	Any enabled interrupt	Clear all interrupts

*If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

Figure 37. Interrupt Flag Register (IFR)

REG 14—INTERRUPT ENABLE REGISTER



Notes:
1. If bit 7 is a "0", then each "1" in bits 0-6 disables the corresponding interrupt.
2. If bit 7 is a "1", then each "1" in bits 0-6 enables the corresponding interrupt.
3. If a read of this register is done, bit 7 will be "1" and all other bits will reflect their enable/disable state.

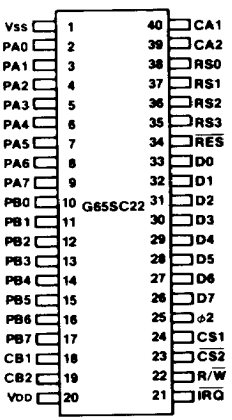
Figure 38. Interrupt Enable Register (IER)

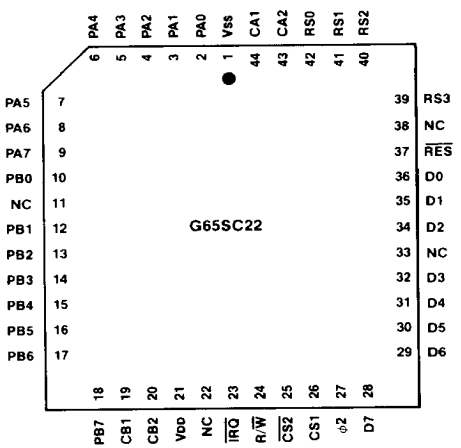
Pin Function Table

Pin	Description
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request

Pin	Description
CS1, $\overline{CS2}$	Chip Select
RS0-RS3	Register Select
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
V_{DD}	Positive Power Supply (+5V)
V_{SS}	Internal Logic Ground

Pin Configuration





Ordering Information