DATA SHEET

GPCE001A

16-bit Sound Controller with 256K x 16 Flash Memory

Oct 01, 2013

Version 1.7

Table of Contents

16-bit SOUND CONTROLLER WITH 256K x 16 FLASH MEMORY

1. GENERAL DESCRIPTION

The GPCE001A, a 16-bit architecture product, equips the newest 16-bit microprocessor, *μ'nSP™ ISA 1.3* developed by Sunplus Technology. This high processing speed ensures the *μ'nSP™ ISA 1.3* is capable of handling sophisticated digital signal processes (DSP) easily and rapidly. Therefore, the GPCE001A is especially targeted to the areas of DSP and Speech/Audio encode/decode. The wide range of CPU speed, from 0.1875MHz to 48MHz, makes the GPCE001A easily to be applied in varieties of applications. The memory capacity contains 256K-word FLASH, and 2K-word working SRAM as well. Other features include 32 programmable multi-functional I/Os, three 16-bit timers/counters, 32768Hz Real Time Clock, Low Voltage Reset/Detection, eight channels of 12-bit ADC (one channel built-in MIC amplifier with Auto Gain Controller), one 16-bit DAC output and two PWM IOs. A power saving mode, halt mode, is designed to only stop CPU clock. To save even more power, a sleep mode is featured to deactivate all of clocks. These two modes can be awakened from the interrupt source triggers.

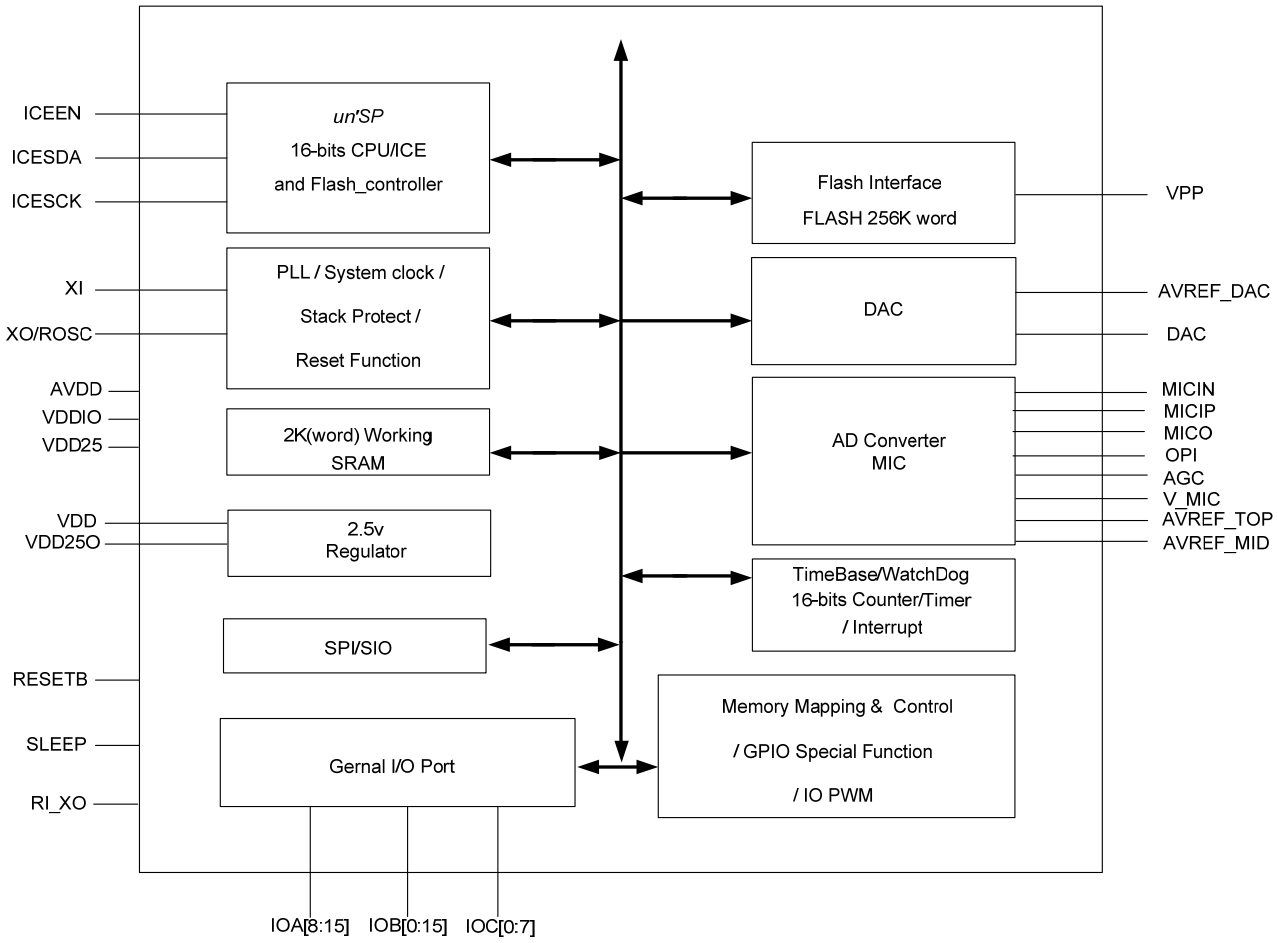
2. APPLICATION FIELD

- Intelligent interactive talking toys
- Advanced educational toys
- General speech synthesizer
- Long duration audio products

3. FEATURES

- 16-bit *μ'nSP™ ISA 1.3* microprocessor
- CPU clock: 0.1875MHz - 48MHz@6MHz crystal
- 256K-word flash memory and 256-word information block
- 2K-word CPU working SRAM
- Chip operating voltage: 2.7V - 3.6V
- IO operating voltage: 2.7V - 5.5V
- Total of 32 programmable IO including IOA(8) & IOB(16) & IOC(8)
- Crystal Resonator & R-oscillator
- Standby mode (Clock Stop mode) for power savings
- Halt mode (only CPU clock stop) for power savings
- Three 16-bit timers/counters
- One 16-bit DAC output
- Wakeup source from IOA key, TIMER/RTC
- 32768Hz Real Time Clock (RTC)
- Eight channels of 12-bit AD converter
- ADC external top reference voltage
- One Generalplus Serial interface I/O
- One SPI serial interface I/O
- Built-in microphone amplifier and AGC function
- Low voltage reset and low voltage detection
- Watchdog enable
- ICE function for development and download into flash memory

4. BLOCK DIAGRAM

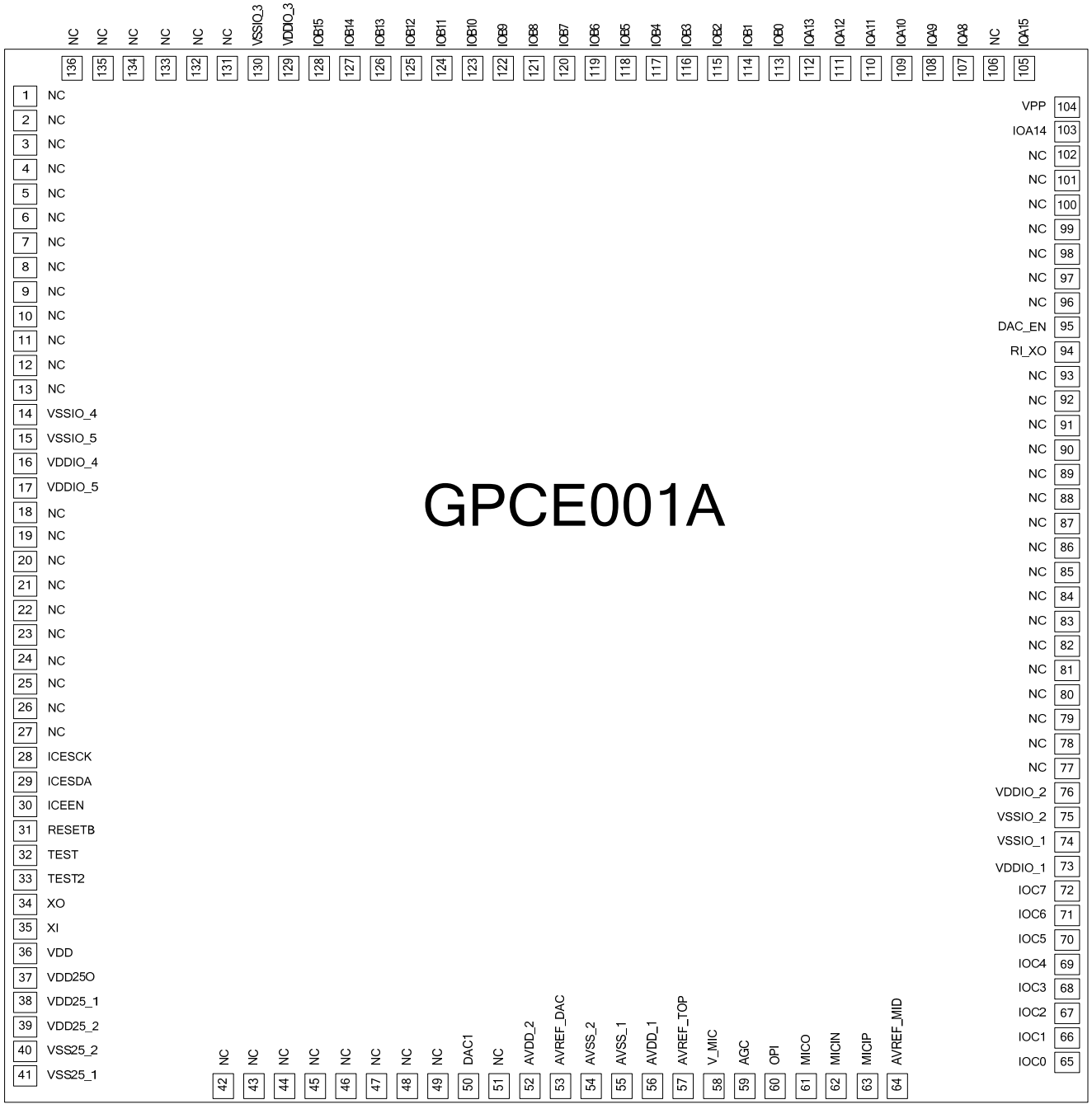


5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	LQFP 128 PIN No.	Type	Description
PORT A, Port B, Port C				
IOA [15:8]	103,105 107-112	97,87,104-99	I/O	IOA [15:8]: bi-directional I/O ports. It can be programmed to wakeup-able I/O pins.
IOB [15:0]	113 - 128	120-105	I/O	IOB [15:0]: bi-directional I/O ports.
IOC [7:0]	65 - 72	72-65	I/O	IOC [7:0]: bi-directional I/O ports.
NC	93	N/A		-
Power & GND				
VDDIO_1	73	73	P	Positive power supply for IOC
VSSIO_1	74	74	G	Ground reference for IOC
VDDIO_2	76	76	P	Positive power supply
VSSIO_2	75	75	G	Ground reference
VDDIO_3	129	121	P	Positive power supply for IOA , IOB
VSSIO_3	130	122	G	Ground reference for IOA , IOB
VDDIO_4, VDDIO_5	16 17	3 4	P	Positive power supply
VSSIO_4, VSSIO_5	14 15	1 2	G	Ground reference
VDD25_1	38	15	P	Positive power supply for core
VSS25_1	41	18	G	Ground reference for core
VDD25_2	39	16	P	Positive power supply for oscillator and PLL
VSS25_2	40	17	G	Ground reference for oscillator and PLL
NC	43	N/A		-
NC	42	N/A		-
AVDD_1	56	47	P	Positive power supply for analog circuit including ADC & MIC
AVSS_1	55	46	G	Ground reference for analog circuit including ADC & MIC
AVDD_2	52	43	P	Positive power supply for analog circuit including DAC
AVSS_2	54	45	G	Ground reference for analog circuit including DAC
VDD	36	13	P	Positive power for regulator and ICESCK, ICESDA, ICEEN, RESETB, TEST, TEST2.
VDD25O	37	14	P	Regulator output for connections to VDD25_1 and VDD25_2.
CLK SYSTEM/ ICE INTERFACE				
ICEEN	30	7	I	ICE (low)/Free run (high) selection pin (floating as H)
ICESDA	29	6	IO	ICE Serial DATA
ICESCK	28	5	I	ICE Clock
XI	35	12	I	Oscillator Crystal input
XO / ROSC	34	11	O	Oscillator Crystal output/ ROSC-input at ROSC mode
OPTION (pin option in both ROM-less and real chip)				
TEST	32	9	I	TEST Mode selection pin
TEST2	33	10	I	TEST Mode for flash
OPTION (mask option in real chip)				
RI_XO	94	78	I	ROSC/Crystal selection pin (No connect as crystal OSC, tie VSS as ROSC)
WDGE	0(info)	N/A	I	Mask option (Flash Information Block) (1: enable watch dog 0: disable)

Mnemonic	PIN No.	LQFP 128 PIN No.	Type	Description
LVR_EN	0(info)	N/A	I	Mask option (Flash Information Block) (1: enable low voltage reset 0: disable)
NC	47-49	N/A		-
DAC				
DAC1	50	41	O	Audio DAC1 output
DAC_EN	95	79	I	DAC enable signal with pull high. We strongly recommend connecting it with power(ex. VDDIO)
ADC				
MICIP	63	54	I	MIC amplifier input positive (Internal Floating)
MICIN	62	53	I	MIC amplifier input negative (Internal Floating)
MICO	61	52	O	MIC amplifier output
OPI	60	51	I	Audio amplifier negative input
AGC	59	50	IO	AGC by pass filter
V_MIC	58	49	O	MIC power output switch to AVDD
AVREF_TOP	57	48	I	AVREF_TOP input
AVREF_MID	64	55	O	AVREF_TOP/2 output with buffer (ADC maximum value voltage)
AVREF_DAC	53	44	O	AVREF_DA reference pin
Other Signal				
RESETB	31	8	I	System reset pin low active (internal 47Kohms pull high resistor)
VPP	104	N/A	P	Flash VPP
NC	1-13,18-27	N/A		-
NC	44-46,47-49	N/A		-
NC	77-92	N/A		-
NC	131-136	N/A		-
Total: 136 pins for chip, 128 pins for LQFP 128 package.				

5.1. PAD Assignment

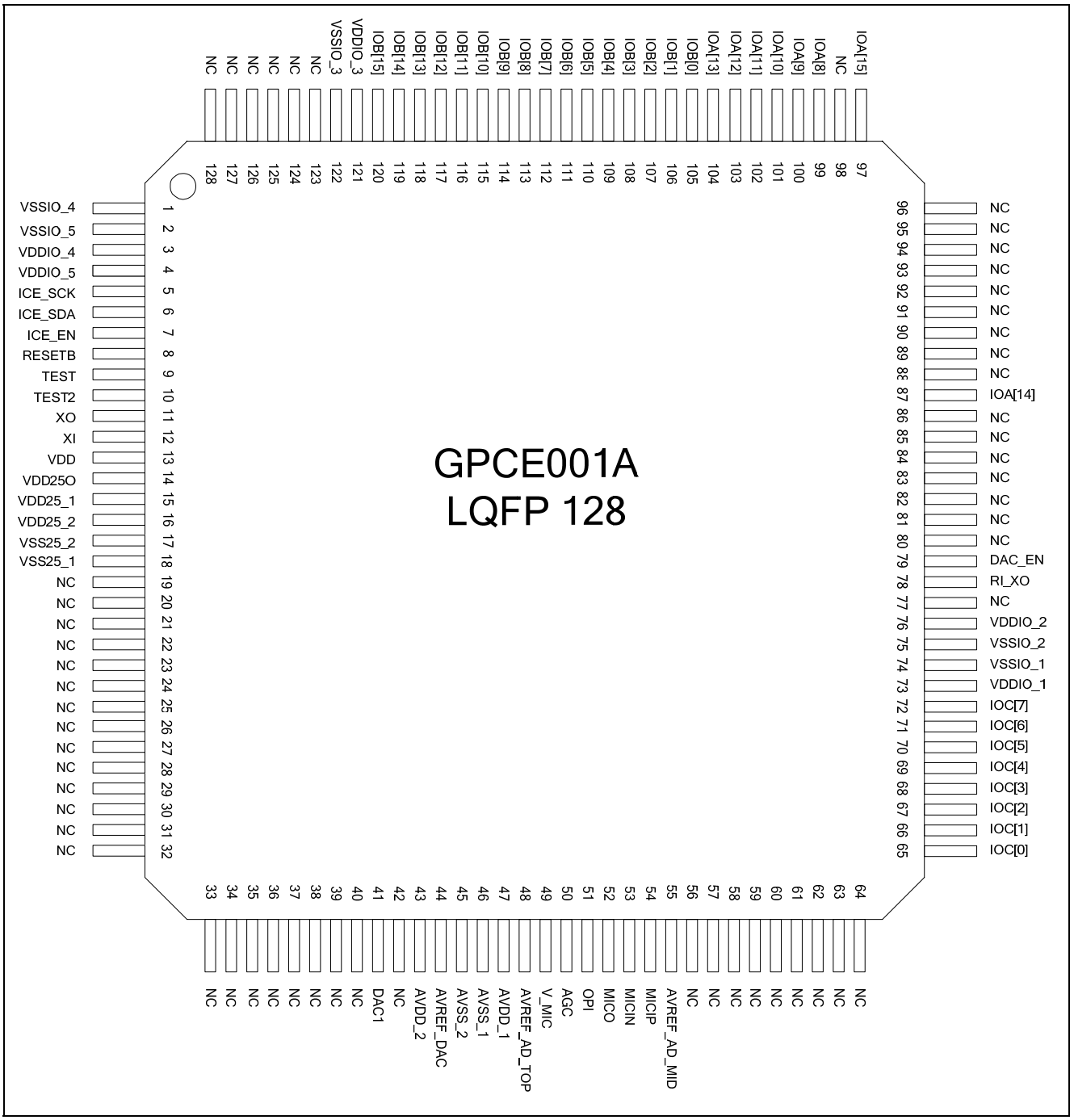


This IC substrate should be connected to VSS

Note1: To ensure the IC functions properly, please bond all VDD and VSS pins.

Note2: The 0.1uF capacitor between VDD and VSS should be placed to IC as close as possible.

5.2. PIN Map


GPCE001A
LQFP 128
1 VSSIO_4
2 VSSIO_5
3 VDDIO_4
4 VDDIO_5
5 ICE_SCK
6 ICE_SDA
7 ICE_EN
8 RESETB
9 TEST
10 TEST2
11 XO
12 XI
13 VDD
14 VDD25O
15 VDD25_1
16 VDD25_2
17 VSS25_2
18 VSS25_1
19 NC
20 NC
21 NC
22 NC
23 NC
24 NC
25 NC
26 NC
27 NC
28 NC
29 NC
30 NC
31 NC
32 NC
33 NC
34 NC
35 NC
36 NC
37 NC
38 NC
39 NC
40 NC
41 DAC1
42 NC
43 AVDD_2
44 AVREF_DAC
45 AVSS_2
46 AVSS_1
47 AVDD_1
48 AVREF_AD_TOP
49 V_MIC
50 AGC
51 OPI
52 MICO
53 MICIN
54 MICIP
55 AVREF_AD_MID
56 NC
57 NC
58 NC
59 NC
60 NC
61 NC
62 NC
63 NC
64 NC
65 IOC[0]
66 IOC[1]
67 IOC[2]
68 IOC[3]
69 IOC[4]
70 IOC[5]
71 IOC[6]
72 IOC[7]
73 VDDIO_1
74 VSSIO_1
75 VSSIO_2
76 VDDIO_2
77 NC
78 RI_XO
79 DAC_EN
80 NC
81 NC
82 NC
83 NC
84 NC
85 NC
86 NC
87 IOA[14]
88 NC
89 NC
90 NC
91 NC
92 NC
93 NC
94 NC
95 NC
96 NC
97 IOA[15]
98 NC
99 IOA[8]
100 IOA[9]
101 IOA[10]
102 IOA[11]
103 IOA[12]
104 IOA[13]
105 IOB[0]
106 IOB[1]
107 IOB[2]
108 IOB[3]
109 IOB[4]
110 IOB[5]
111 IOB[6]
112 IOB[7]
113 IOB[8]
114 IOB[9]
115 IOB[10]
116 IOB[11]
117 IOB[12]
118 IOB[13]
119 IOB[14]
120 IOB[15]
121 VDDIO_3
122 VSSIO_3
123 NC
124 NC
125 NC
126 NC
127 NC
128 NC

6. FUNCTIONAL DESCRIPTION

6.1. CPU

The GPCE001A is equipped with a 16-bit μ'nSP® (read as "micro-n-SP") designed by SUNPLUS. Thirteen registers are available in μ'nSP®: R1 ~ R4 (General-purpose registers), SR1 ~ SR4 (Secondary Bank Registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and FR (Flag Register). It provides interrupts, including fifteen FIQs (Fast Interrupt Request) and sixteen IRQs (Interrupt Request), plus one software-interrupt, BREAK.

Moreover, a high performance hardware multiplier with the capability of FIR filter calculation is also built-in to reduce the software multiplication loading.

6.2. Memory

6.2.1. SRAM

The amount of SRAM is 2K-word (including Stack) ranged from $0000 through $07FF with two CPU-clock cycles access speed.

6.2.2. Flash memory

Flash memory size is 256K words and its address is mapped from $04000 to $043FFF. This flash memory is a high-speed memory, with 50ns access time, containing 256 words information block ranged from $2700 through $27ff as well as containing option information for GPCE001A. The option in information block is described below.

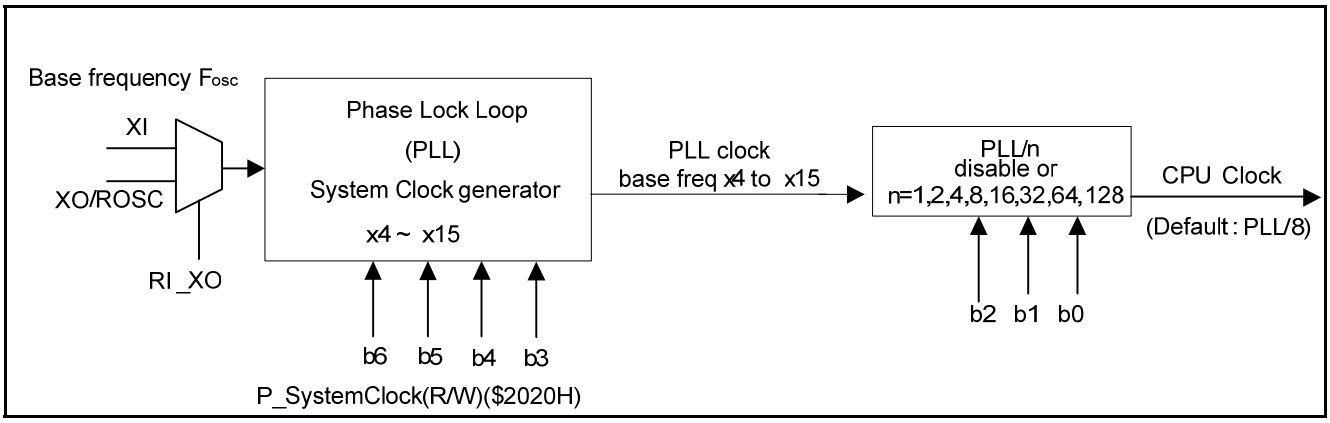
OPTION_SECURITY: enable or disable ICE read.

OPTION_WDOG_EN: enable or disable Watchdog reset.

OPTION_PARA_WP: enable or disable flash write function in address range from $C000 through $FFFF.

OPTION_MAIN_WP: enable or disable flash write function in address range from $10000 through $43FFF.

Writing option into flash information block is done by IDE tool.



6.3. PLL, Clock, Power saving Mode

6.3.1. PLL (Phase Lock Loop)

The purpose of PLL is to provide stable output frequency which takes the base frequency (from crystal) for reference. The PLL frequency gain (output frequency/input frequency) ranges from 4 to 15. Suppose base frequency is 6 MHz and PLL frequency gain selects 8, the output frequency of PLL is 48 MHz.

6.3.1.1. System clock

Basically, the system clock is provided by PLL and determined by programming the P_SystemClock (W). The default PLL clock (PLL) pumps to $6*F_{OSC}$, that is 36MHZ using 6MHZ crystal and CPU clock is 4.5MHZ (with default value: PLL/8).

6.3.1.2. 32768Hz RTC

The Real Time Clock (RTC) is normally used in watch, clock or other timing-based applications. A 2Hz-RTC (0.5 seconds) function is available in GPCE001A. The RTC counts the time as well as to wake CPU up whenever RTC occurs. Time can be traced by the numbers of RTC occurrence. In addition, GPCE001A supports 32768Hz oscillator in strong mode and weak mode for power savings. In strong mode, 32768Hz OSC circuit in GPCE001A always runs at the highest power consumption. On the other hand, 32768Hz OSC in GPCE001A circuit run less power consumption in weak mode, but it must use a high-standard 32768Hz external crystal such as SEIKO SSP_T6 or Microcrystal CC5V-T1A.

6.4. Power Saving Mode

The GPCE001A features a power savings mode (or called standby mode) for low power applications. To enter standby mode, the desired key wakeup port (IOA[15:8]) must be configured to input first. And read the P_IOA_Data to latch the IOA state before entering the standby mode. Also remember to enable the corresponding interrupt source(s) for wakeup. After that, stop the CPU clock by writing $5555 into P_SystemSleep(W) to enter standby mode. In such mode, SRAM and I/Os remain in the previous states until CPU being awakened. The wakeup sources in GPCE001A include KEY wake up (IOA15 - 8), RTC wakeup, and IRQ1 - IRQ7. After GPCE001A is awakened, CPU will continue to execute the program from the location it slept. Programmer can also enable or disable the 32768Hz RTC when CPU is in standby mode.

6.5. CPU Halt Mode

The GPCE001A features a CPU halt mode for power savings. In this mode, the CPU clock is turned off.

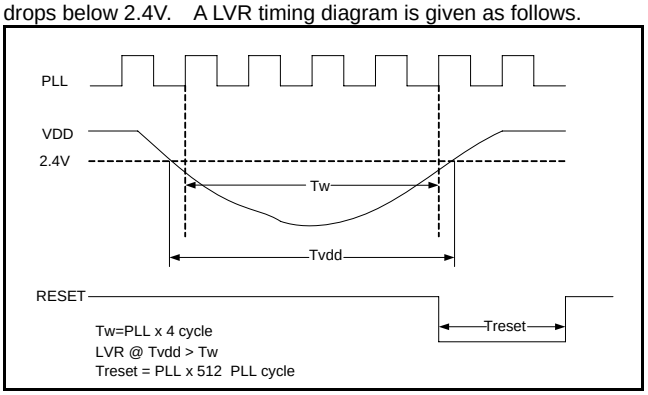
6.6. Low Voltage Detection and Low Voltage Reset

6.6.1. Low Voltage Detection (LVD)

The Low Voltage Detect (LVD) reports the circumstance of present voltage. There are four LVD levels to be selected: 2.6V, 2.8V, 3.0v and 3.2V. Those levels can be programmed via P_LVD_Ctrl. As an example, suppose LVD is given to 2.8V. When the voltage drops below 2.8V, the b12 of P_LVD_Ctrl is read as HIGH. In such state, program can be designed to react this condition.

6.6.2. Low voltage reset

In addition to the LVD, the GPCE001A provides another important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops below 2.4V for 4 consecutive PLL system clock cycles. Without LVR, the CPU becomes unstable and malfunctions when the operating voltage drops below 2.4V. Using LVR, it will reset all functions to the initial operational (stable) states when the voltage drops below 2.4V. A LVR timing diagram is given as follows.



6.6.3. Watchdog reset

The GPCE001A provides another important feature, watchdog reset. With the watchdog function, a reset signal is generated to reset system when watchdog counter is overflow and the option of OPTION_WDOG_EN is enabled.

The purpose of watchdog is to monitor whether the system operates normally. Within a certain period, watchdog register must be cleared. If it is not cleared, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again.

6.6.4. Soft reset protection

Software reset. Writes $5555 into P_System_Reset will reset the whole system like hardware reset(pull low RESETB pin), except a flag will set on in P_System_LVD_Ctrl(R/W).

6.6.5. Stack access protection

GPCE001A will be reset when stack operation (example push or pop) of CPU accesses the SRAM that is not in the defined range. The defined stack range uses stack top (P_Stack_Top) and bottom (P_Stack_Bottom) control register.

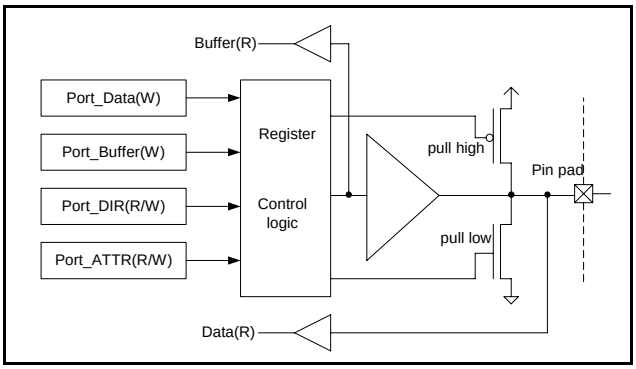
6.7. Interrupt

The GPCE001A has 16 interrupt sources, grouped into two types, FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources.

Interrupt Source	Interrupt Name / FIQ Name	IRQ Priority
Timer A	IRQ0_TMA/FIQ_TMA	1(High)
Timer B	IRQ1_TMB/FIQ_TMB	2
Timer C	IRQ2_TMC/FIQ_TMC	3
SPI	IRQ3_SPI/FIQ_SPI	4
SIO	IRQ3_SI/O	5
Key wakeup	IRQ5_KEY/FIQ_KEY	6
EXT1	IRQ5_EXT1/FIQ_EXT1	7
EXT2	IRQ5_EXT2/FIQ_EXT2	8
4096Hz	IRQ6_4KHz/FIQ_4KHz	9
2048Hz	IRQ6_2KHz/FIQ_2KHz	10
512Hz	IRQ6_512Hz/FIQ_512Hz	11
64Hz	IRQ7_64Hz/FIQ_64Hz	12
16Hz	IRQ7_16Hz_FIQ_16Hz	13
2Hz	IRQ7_2Hz/FIQ_2Hz	14(Low)

6.8. I/O

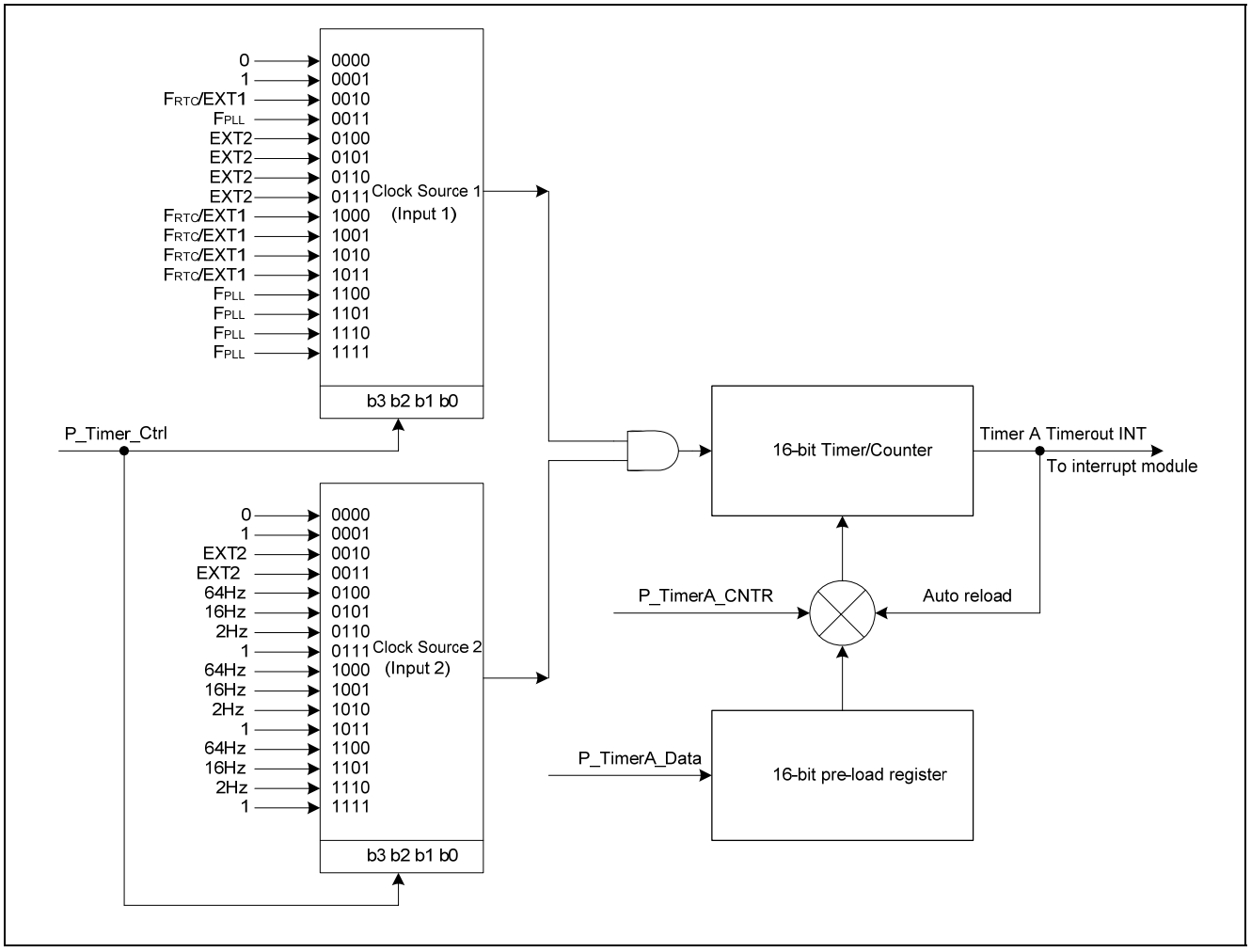
Three I/O ports are built in GPCE001A - PortA, PortB, PortC. The PortA is an general purpose I/O with programmable wakeup capability, i.e. IOA[15:8] is the key wakeup port. User can latch data on P_IOA_Data and enable the key wakeup function. Wakeup is triggered when the PortA state is different from latched data. Furthermore, the I/O ports can be operated at 5V level, higher than the CPU core which is a 2.5V level system. Suppose system operating voltage is running at 2.7V, VDDIO (power for I/O) operates from 2.7V to 5.5V. In such condition, the I/O pad is capable of operating from 0V to VDDIO. The following diagram is an I/O schematic. Although data can be written into the same register through Port_Data and Port_Buffer, they can be read from different places, Buffer(R) and Data(R).



In addition to a general purpose I/O port function, PortA/B/C also shares/carries some special functions. A summary of PortA/B/C special functions is listed as follows:

Port	Special Function	Function Description
IOA8	APWMO1	TimerA PWM output
IOA9	BPWMO1	TimerB PWM output
	IROUT	IR Output
IOA10	Feedback Output2	Work with IOA11 by adding a RC circuit between them to get an OSC to EXT2 interrupts.
IOA11	Feedback Input2	-
	EXT2	External interrupt source 2 (negative edge triggered)
IOA12	Feedback Output1	Work with IOA13 by adding a RC circuit between them to get an OSC to EXT1 interrupts.
IOA13	Feedback Input1	-
	EXT1	External interrupt source 1 (negative edge triggered)

Port	Special Function	Function Description
IOA14	RTCO	Real time clock output
IOA15	RTCI	Real time clock input
IOB6	APWMO2	TimerA PWM output
IOB7	BPWMO2	TimerB PWM output
IOB10	SDA	Serial interface data
IOB11	SCK	Serial interface clock
IOB12	CS	SPI chip select
IOB13	CK	SPI clock
IOB14	DI	SPI data input
IOB15	DO	SPI data output
IOC0	AN0	ADC Channel 0
IOC1	AN1	ADC Channel 1
IOC2	AN2	ADC Channel 2
IOC3	AN3	ADC Channel 3
IOC4	AN4	ADC Channel 4
IOC5	AN5	ADC Channel 5
IOC6	AN6	ADC Channel 6
IOC7	AN7	ADC Channel 7



Refer to the above table, the configuration of IOA10, IOA11, IOA12, IOA13 involves feedback function that an OSC frequency can be obtained from EXT1 (EXT2) by simply adding a RC circuit between IOA10 (IOA12) and IOA11 (IOA13).

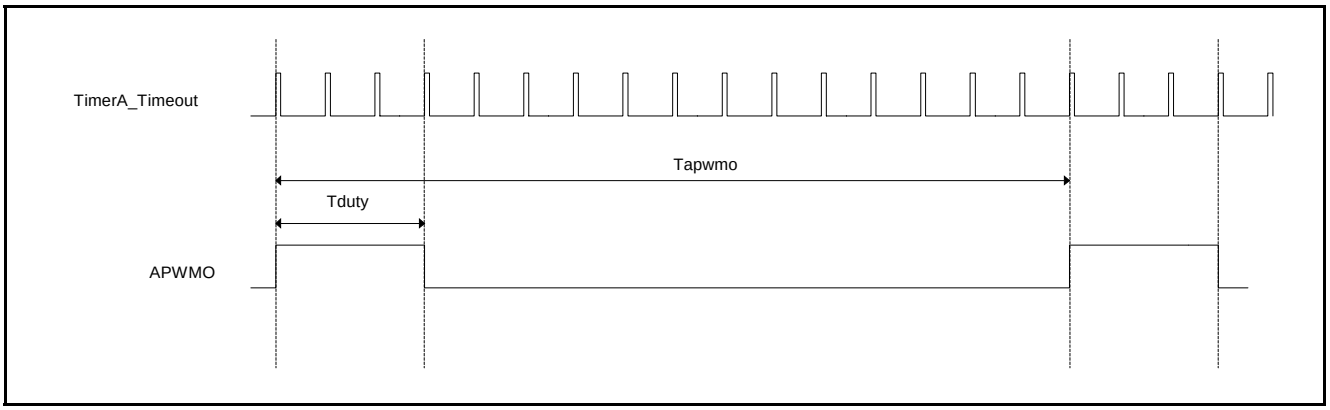
6.9. Timer/Counter

GPCE001A provides three 16-bit timers/counters - TimerA, TimerB and TimerC, or so called universal counters. The clock source of Timer A/B/C are from clock source Input1 and clock source Input2 (as following table) which perform AND operation to form varieties of combinations. When timer overflows, a timeout signal (TAOUT) is sent to CPU interrupt module to generate a timer interrupt signal. In addition, Timer A/B/C hardware interrupt events can be used to latch the DAC audio output and trigger ADC conversion.

Example to Timer A, sending a write signal into TMA_CNT, the value of TMA_DATA (value=N) will reload into TMA_CNT and set an appropriated clock source. Timer will up-count from N, N+1, N+2… 0XFFFF. An INT signal is generated at the moment of timer rolling over from “0xFFFF” to “0x0000”, and an INT signal is processed by INT controller immediately. At the same time, N will be reloaded into TMA_CNT and start counting again.

In Timer A, the clock Input 1 is a high frequency source and clock Input 2 is a low frequency clock source. The combination of clock Input 1 and 2 provides varieties of speeds to TimerA / CounterA - “1” representing pass signal (not gating), and “0” meaning timer deactivated. For instance, if Input 1 =”1”, the clock is depending on Input 2. If Input 1 =”0”, the TimerA is deactivated. The EXT1/EXT2 is the external clock source.

TMXSEL	Input 1	Input 2
0000	‘0’	‘0’
0001	‘1’	‘1’
0010	F_{RTC} / EXT1	EXT2
0011	F_{PLL}	EXT2
0100	EXT2	64Hz
0101	EXT2	16Hz
0110	EXT2	2Hz
0111	EXT2	‘1’
1000	F_{RTC} / EXT1	64Hz
1001	F_{RTC} / EXT1	16Hz
1010	F_{RTC} / EXT1	2Hz
1011	F_{RTC} / EXT1	‘1’
1100	F_{PLL}	64Hz
1101	F_{PLL}	16Hz
1110	F_{PLL}	2Hz
1111	F_{PLL}	‘1’



6.9.1. IO PWM

Two IO PWMs which duty is selected from 1/16 to 14/16. Example in the above figure is a 3/16-duration cycle. The APWMO waveform is made by selecting a pulse width through P_APWM_Ctrl. As a result, each 16 cycles will generate a pulse width defined in control port. These PWM signals can be applied for controlling the speed of motor or other devices.

6.9.2. Timebase

Timebase, generated by 32768Hz crystal oscillator, is a combination of frequency selection. Furthermore, timebase generates 4KHz, 2KHz, 512Hz, 64Hz, 16Hz and 2Hz interrupt sources (IRQ6, IRQ7) for Real-Time-Clock.

6.10. Sleep mode, Wakeup, Halt mode, and Watchdog

6.10.1. Sleep and Wakeup modes

1) Sleep: After power-on reset, IC starts running until a sleep command is issued. When a sleep command is accepted, IC will turn the system clock (PLL) off. After all, it enters sleep mode.
2) Wakeup: CPU awaking from sleep mode requires a wakeup signal to turn the system clock (PLL) on. The FIQ/IRQ signal makes CPU complete the wakeup process and initialization. The CPU wakeup source is given in the following table.
3) Halt mode: Halt mode is for power saving. In this mode, CPU clock is turned off.

Wakeup Source
FIQ source
Timer A interrupt
Timer B interrupt
Timer C interrupt
SPI interrupt
EXT1/EXT2/KEY
RTC

6.11. ADC (Analog to Digital Converter) / DAC

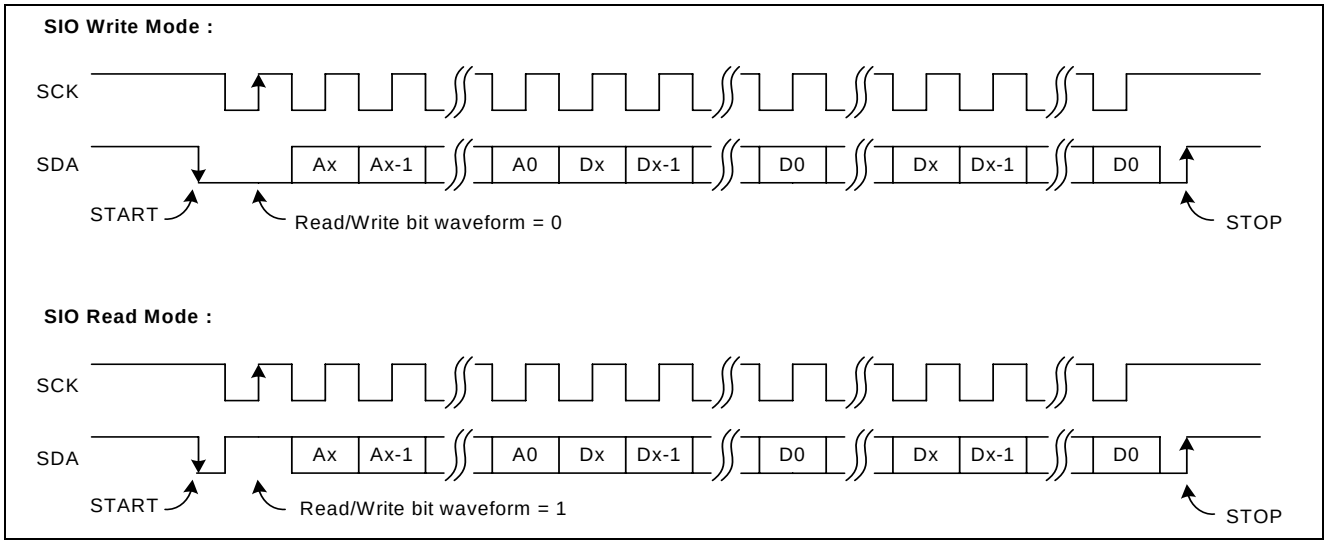
The GPCE001A has eight channels of 12-bit A/D (Analog to Digital Converter). The function of an A/D converter is to convert analog quality signal, e.g. a voltage into a digital word or input source, can be eight channels line-in from IOC[7:0] or one channel microphone input through amplifier and AGC controller. The MIC amplifier circuit is capable of reducing common mode noise by transmitting signals through MIC fully differential Input. Moreover, an external resistor can be applied to adjust microphone gain and time of AGC operating. The ADC needs to select source of line-in before converting.

6.12. 16-bit DAC Audio Driver

The GPCE001A provide one 16-bit DAC for audio output.

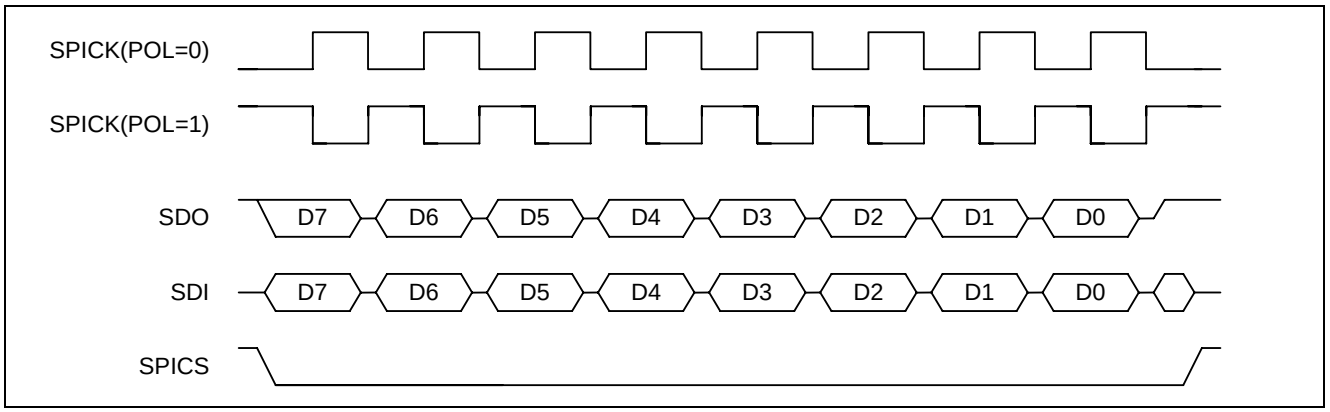
6.13. Serial Interface I/O (SIO)

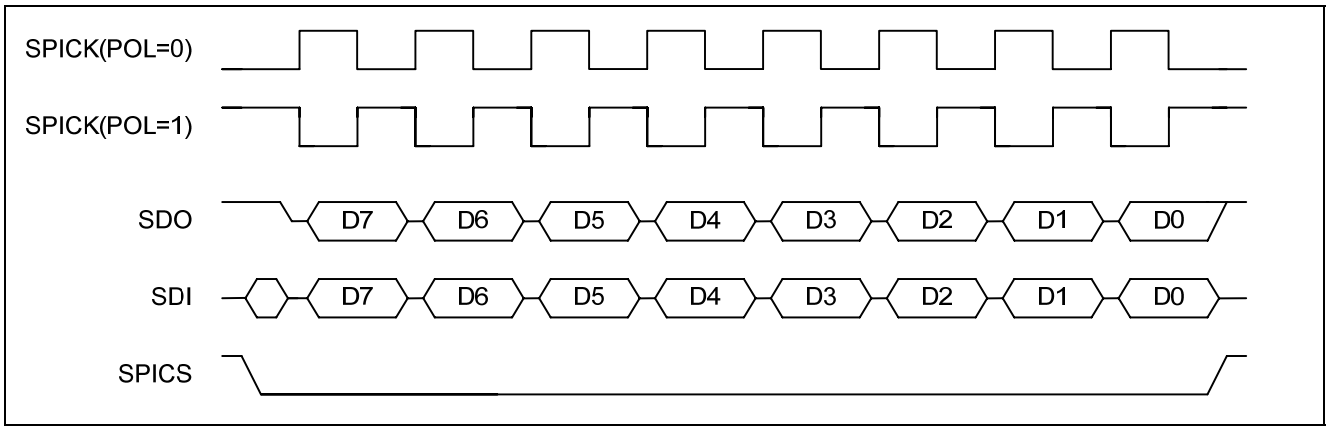
Serial interface I/O offers a one-bit serial interface that communicates with other devices. This serial interface is capable of transmitting or receiving data via two I/O pins, IOB11 (SCK) and IOB10 (SDA).



6.14. SPI

A Serial Peripheral Interface (SPI) controller is built in GPCE001A to facilitate communicating with other devices and components. There are four control signals on SPI - SPICS (IOB12), SPICK (IOB13), SDI (IOB14), and SDO (IOB15).





6.15. Audio Algorithm

The following speech types can be used in GPCE001A: PCM, LOG PCM, SACM_S200 SACM_S480, SACM_S530, SACM_S720, SACM_A1600, SACM_A1601, SACM_A3200, SACM_A3600, SACM_DVR1600 (Digital Voice Recorder), and SACM_DVR4800. For melody synthesis, the GPCE001A provides a SACM_MS01 (FM synthesizer) and SACM_MS02 wave-table synthesizer.

6.16. Security Function

Security function is able to protect code been read or written. When program is downloaded into flash memory, program can be read/write protected by IDE tools for security purpose. By writing security enable option, the IDE function will be disabled except the flash mass erase function in ICE mode. After Mass erase the flash, the security option will be enabled again, to enable the security option cannot limit CPU to read flash content in free run mode.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
Regulator Supply Voltage	VDD	-0.3	4.0	V
IO PAD Supply Voltage	VDDIO	-0.3	6.0	V
Analog Supply Voltage	AVDD	-0.3	4.0	V
Core Supply Voltage	VDD25	-0.3	3.0	V
Input Voltage Range	V_{IN}	-0.3	VDDIO + 0.5	V
ESD Protection(HBM)	V_{ESD}	2K	-	V
Operating Temperature Range	T_A	0	+60	℃
Storage Temperature Range	T_{STO}	-50	+150	℃

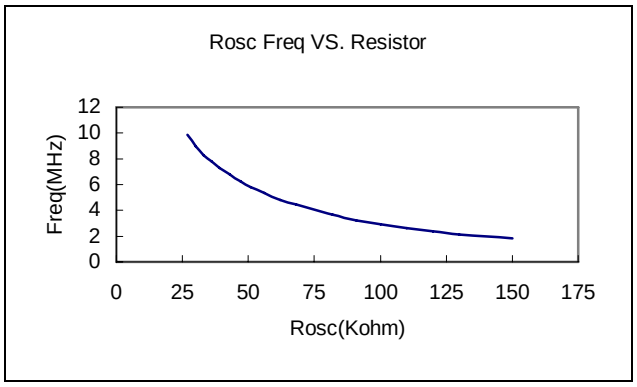
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Electrical Characteristics.

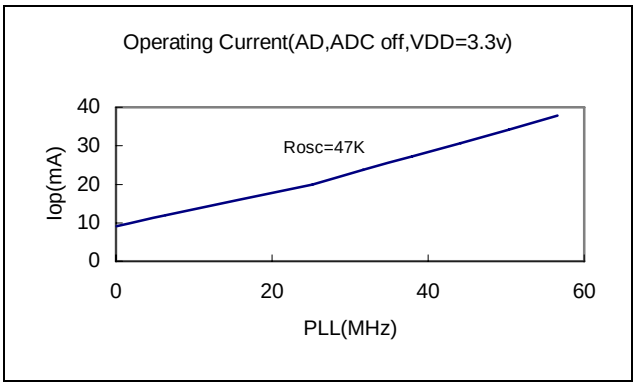
7.2. DC Characteristics (VDD25=2.5V, VDD = 3.3V, VDDIO = 5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage (IO)	VDDIO	2.7	5.0	5.5	V	IO VDD
Operating Voltage (Regulator)	VDD	2.7	3.3	3.6	V	3.3V for regulator power
Operating Voltage (Analog)	AVDD	2.7	3.3	3.6	V	3.3V for analog power
Operating Voltage (Core)	VDD25	2.4	2.5	2.7	V	2.5V for core power
Regulator Max Output Current	I(VDD25O)	-	-	60	mA	VDD = 3.0V, VDD25O= 2.5V, (Regulator output)
Operating Current	I_{OP}	-	40	-	mA	PLL = 48MHz, AD, DAC disable, no loading ; VDD25 = 2.5V; VDD =3.3V; VDDIO = 5.5V
Standby Current	I_{STB}	-	10	30	μA	Disable 32KHz crystal
Input High Level	V_{IH}	0.7 VDDIO	-	-	V	-
Input Low Level	V_{IL}	-	-	0.3 VDDIO	V	-
IO Output High Current	I_{OH}	-	-6.0	-	mA	V_{OH} = 0.9 × VDDIO
IO Output Low Current	I_{OL}	-	12.0	-	mA	V_{OL} = 0.1 × VDDIO
Input Pull-Low Resistor (IOA [8:13], IOB)	R_{PL1}	-	90	-	KΩ	V_{IN} = VDDIO
Input Pull-Low Resistor (IOA [14,15], IOC)	R_{PL2}	-	410	-	KΩ	V_{IN} = VDDIO
Input Pull-High Resistor (IOA, IOB, IOC)	R_{PH}	-	130	-	KΩ	V_{IN} = VSS

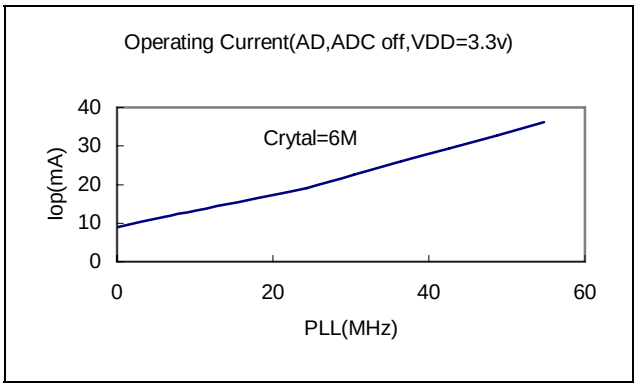
7.2.1. R-OSC Frequency VS Resistor

7.2.1.1. VDD25=2.5V, VDD = 3.3V, VDDIO = 5V, T_A = 25℃





7.2.1.2. Operation current (VDD25=2.5V, VDD = 3.3V, VDDIO = 5V, T_A = 25℃)



7.3. ADC Characteristics (AVDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
ADC Line_In Input Voltage Range from IOC[7:0]	VINL (Note 1)	AVSS-0.3	-	AVDD+0.3	V
ADC Microphone Input Voltage Range	VINM	AVSS-0.3	-	AVDD+0.3	V
External ADC Top Voltage	VEXTREF (Note 2)	2.0	-	AVDD+0.3	V
Resolution of ADC	RESO	-	-	12	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 4)	-	60	-	dB
Effective Number of Bit	ENOB (Note 5)	-	9.6	-	bits
Integral Non-Linearity of ADC	INL	-	±3.0	-	LSB (Note 3)
Differential Non-Linearity of ADC	DNL (Note 6)	-	±1.0	-	LSB
No Missing Code		-	12	-	Bits
Max ADC Clock		-	-	3.375	MHz
AD Conversion Rate	F_{CONV}	-	-	150K	Hz

Note1: Internal protection diodes clamp the analog input to AVDD and AVSS. These diodes allow the analog input to swing from (AVSS-0.3V) to (AVDD+0.3V) without causing damage to the devices.

Note2: The ADC performance is limited by the system's noise level, so the GPCE001A just guarantee with the 8-bit accuracy when AVREF_TOP is 2V.

Note3: LSB means Least Significant Bit. With VINL=3V, 1LSB=3V/2^12= 0.732 mV.

Note4: The SINAD testing condition at VINLp-p=3.1V, F_{CONV} = 48KHz, Fin=0.997KHz Sine waves at AVDD=3.3V from the IOC [7:0] input.

Note5: ENOB=(SINAD-1.76)/6.02.

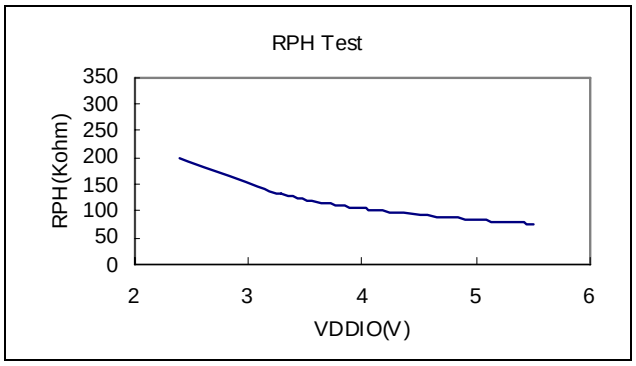
Note6: The ADC of GPCE001A can guarantee no missing code.

7.4. DAC Characteristics (AVDD = 3.3V, T_A = 25℃)

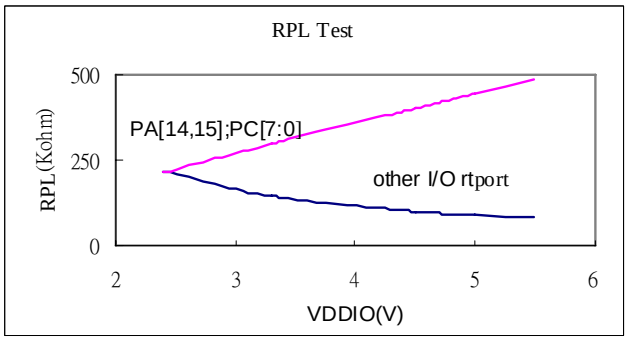
Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Resolution of DAC	RESO	-	16	-	bit
Signal to Noise Ratio of DAC	SNR	-	90	-	dB
Dynamic Range	DR	-	85	-	dB
Sample Rate	F_S	-	200K	-	Hz
THD+N at FS	F_{OUT}=0.997KHz	-	-60	-	db
Output Loading	RL	125	-	-	chm
Output Range	Input=Full Scale	-	60%	-	AVDD

Note1: The THD+N testing condition at AVDD=3.3, F_s=48KHz, Fin=0.997KHz input at RL=125 ohm

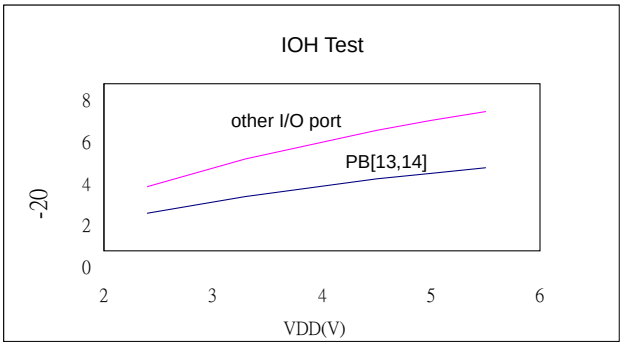
7.4.1. Pull High Resister and VDDIO



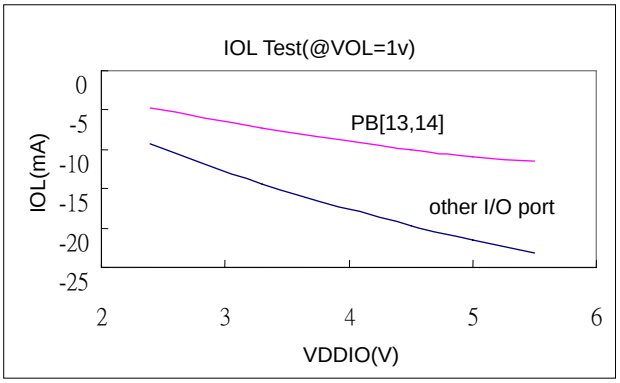
7.4.2. Pull Low Resister and VDDIO



7.4.3. I/O Output High Current I_{OH} and V_{OH}

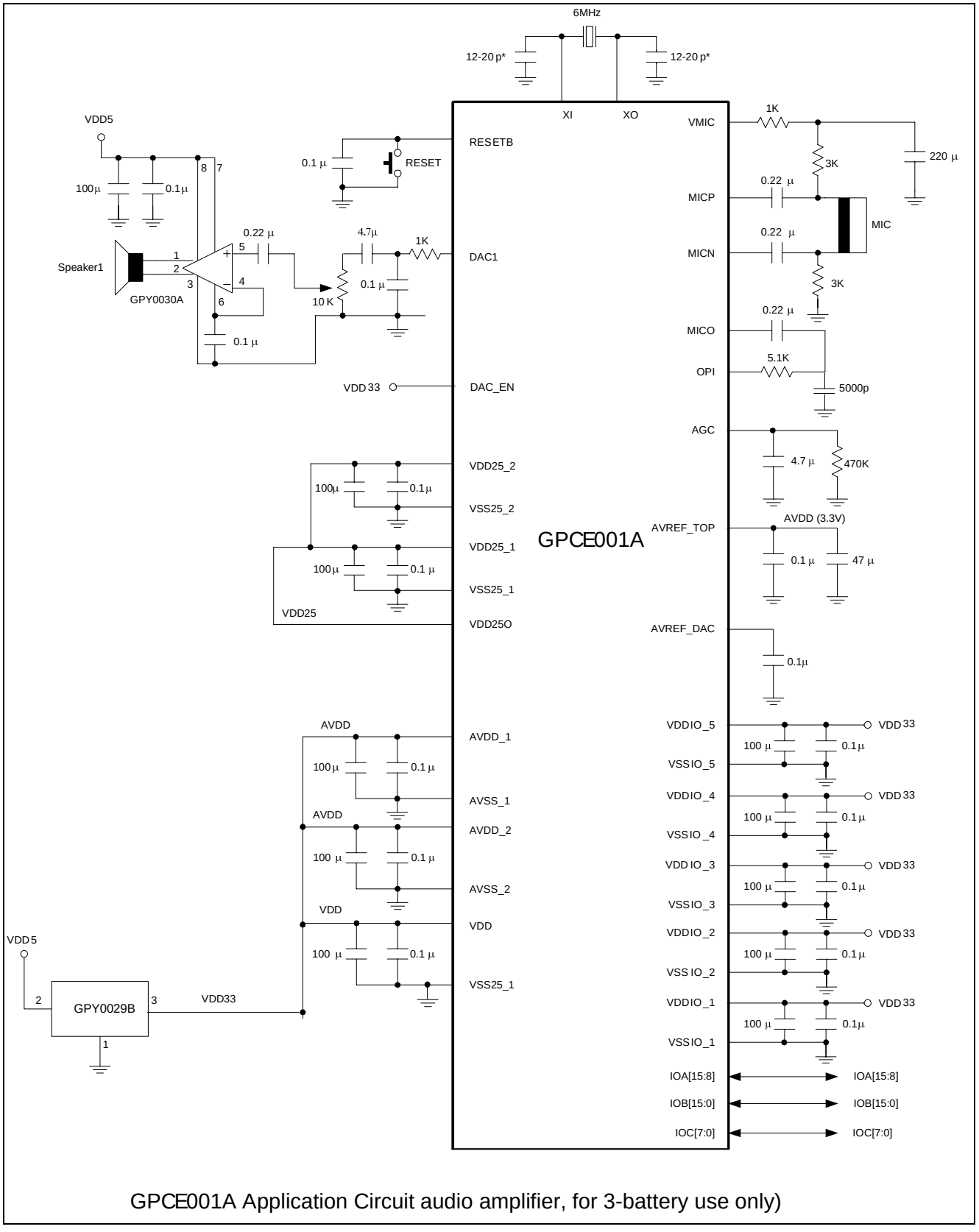


7.4.4. I/O Output Low Current I_{OL} and V_{OL}



8. APPLICATION CIRCUITS

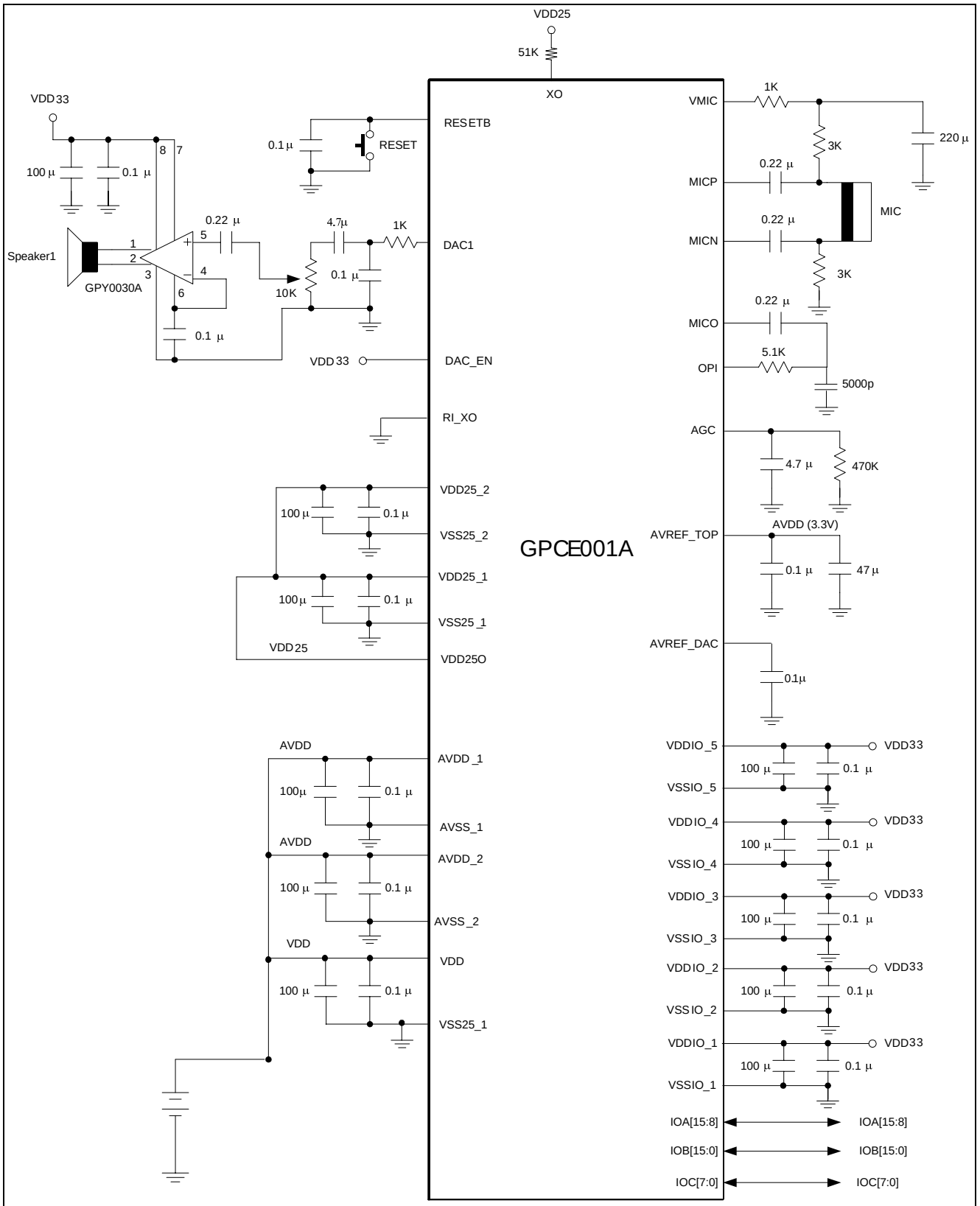
8.1. Application Circuit 1 (with Crystal)



GPCE001A Application Circuit audio amplifier, for 3-battery use only)

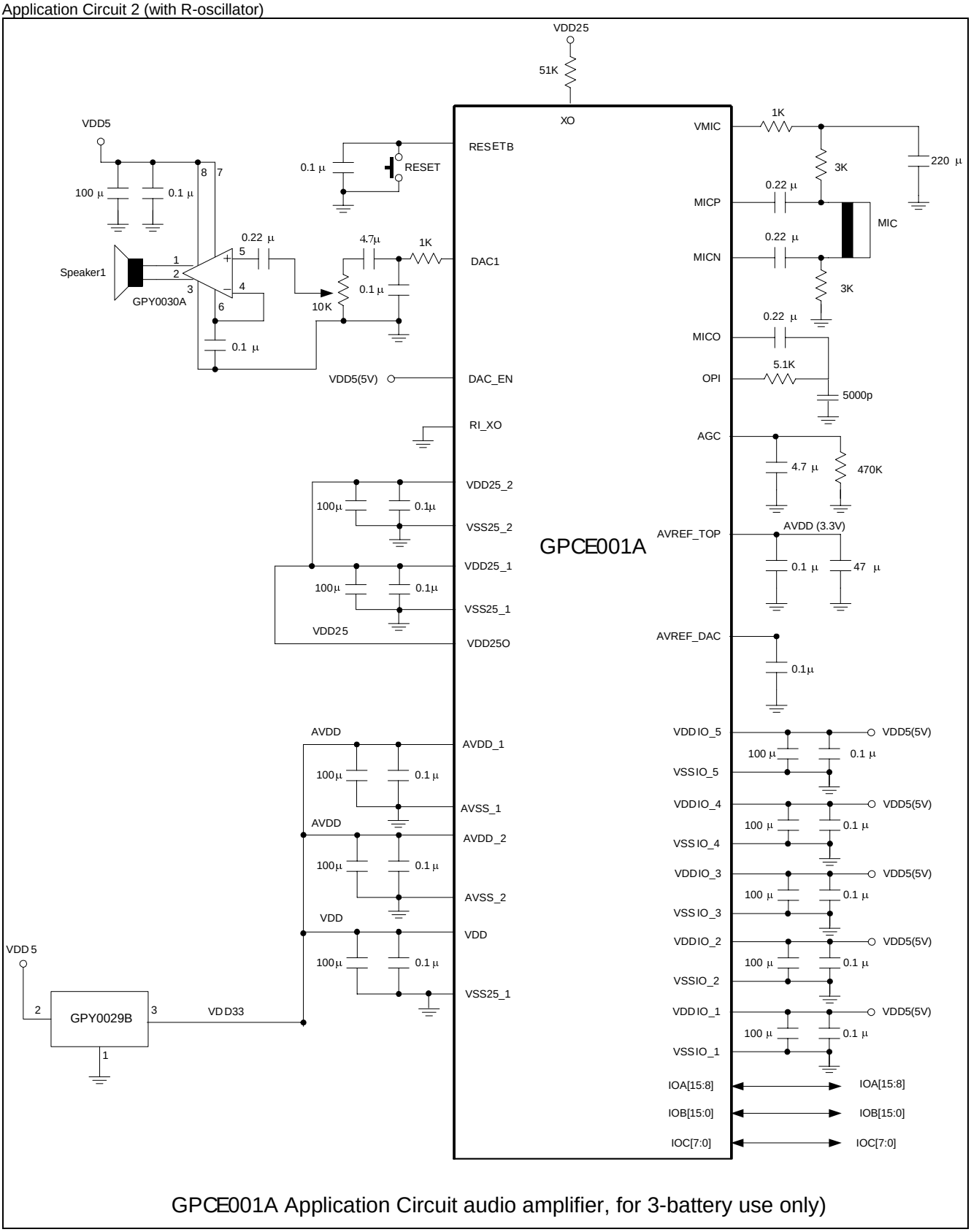
Note*: These capacitor values are for design guidance only. Different capacitor values may be required for different crystal/resonator used.

8.2. Application Circuit (with R-oscillator)



GPCE001A Application Circuit audio amplifier, for 2-battery use only)

Application Circuit 2 (with R-oscillator)



GPCE001A Application Circuit audio amplifier, for 3-battery use only)

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCE001A-NnnV-C	Chip form
GPCE001A-NnnV-QL09x	Halogen Free Package

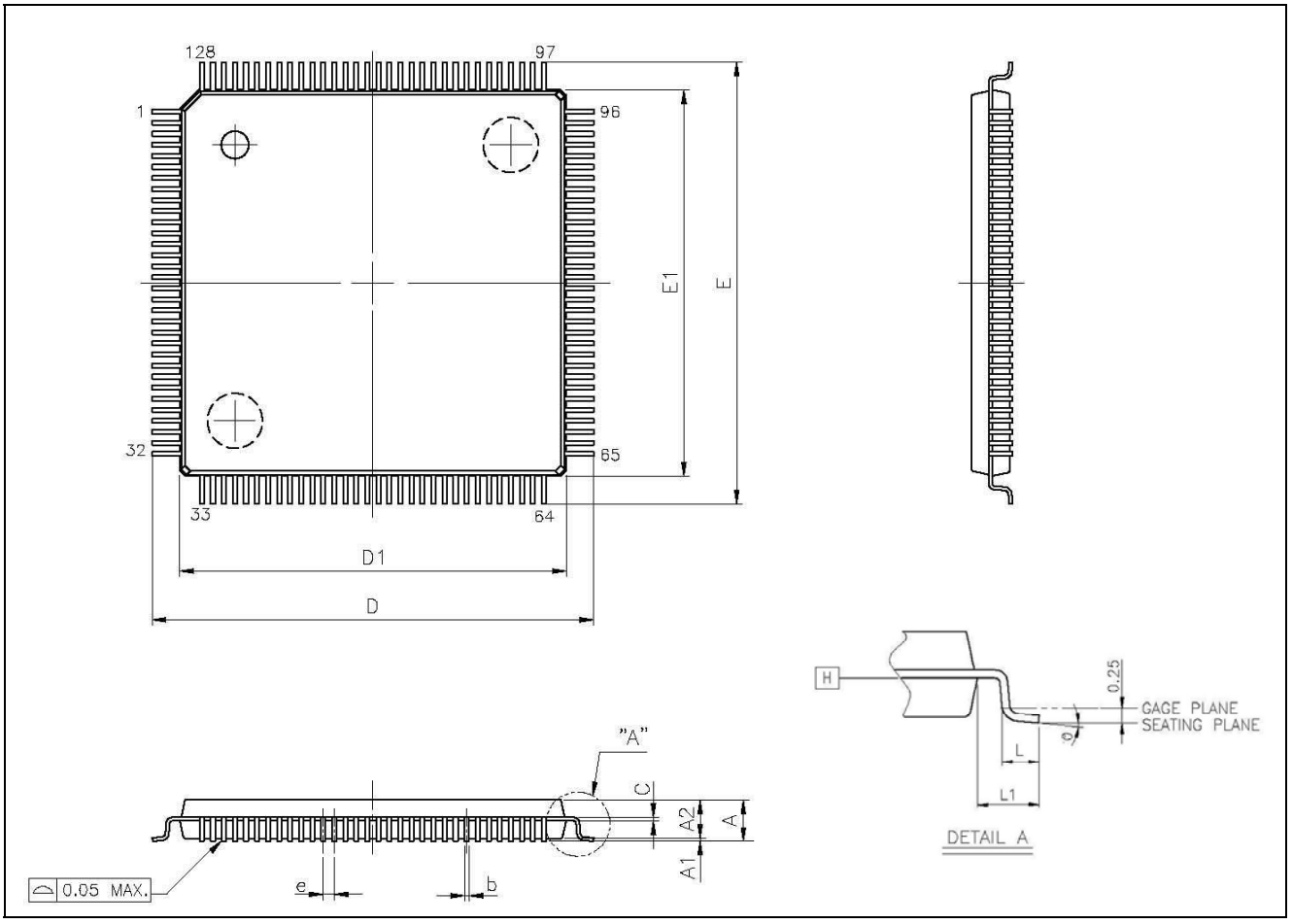
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 0 - 9, serial number).

9.2. Package Information

9.2.1. LQFP 128 outline dimensions



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	-	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
E	16.00 BSC.		

Symbol	Dimension in inch		
	Min.	Typ.	Max.
E1		14.00 BSC.	
e		0.40 BSC.	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

11. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 01, 2013	1.7	Add COMAIR logo to the cover page	
May 09, 2011	1.6	Rename one NC pin to DAC_EN and modify related application circuit.	5,6,7,8, 19,20,21
Sep. 15, 2009	1.5	Modify 7.2 DC Characteristics.	16
Jan. 12, 2009	1.4	1. Modify “SIGNAL DESCRIPTIONS” in section 5. 2. Modify “Application Circuit2” in section 8.3.	5 21
Sep. 09, 2008	1.3	Modify section 8. APPLICATION CIRCUITS.	19-21
Jul. 04, 2007	1.2	1. Modify the “SIGNAL DESCRIPTIONS” in section 5. 2. Modify the “PAD Assignment” in section 9.1. 3. Add the “Package Information” in section 9.3.	5 21 22
Jan. 05, 2007	1.1	Rename to match the real body function.	1
Oct. 05, 2006	1.0	Original	22