DATA SHEET

GPM8F1129A
GPM8F1065A
GPM8F1033A
GPM8F1019A

30/20-pin Microcontroller with 128/64/32/18KB Flash Memory

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Version 1.0

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30/20 PIN 8-BIT MICROCONTROLLER WITH 128/64/32/18KB FLASH

1. GENERAL DESCRIPTION

The GPM8F1129A/GPM8F1065A/GPM8F1033A/GPM8F1019A, a highly integrated microcontroller, integrates a pipelined 1T 8051 CPU, 1.5K-byte XRAM, 256-byte IDM SRAM and 128K/64K/32K/18K-byte program Flash memory. It also contains a maximum of 23 programmable multi-functional I/Os, Timer0/1/2, UART0, SPI (master), I2C, and CMDT for a variety of applications. It operates over a wide voltage range from 1.8V through 5.5V and wide temperature range from -5℃ ~ 70℃. It features two power management modes for power saving purpose. To make development and debug work more easily, an on-chip debug circuit is included to facilitate full speed in-system debug. For more details about GPM8F series, please refer to the feature list in the following section.

2. FEATURES

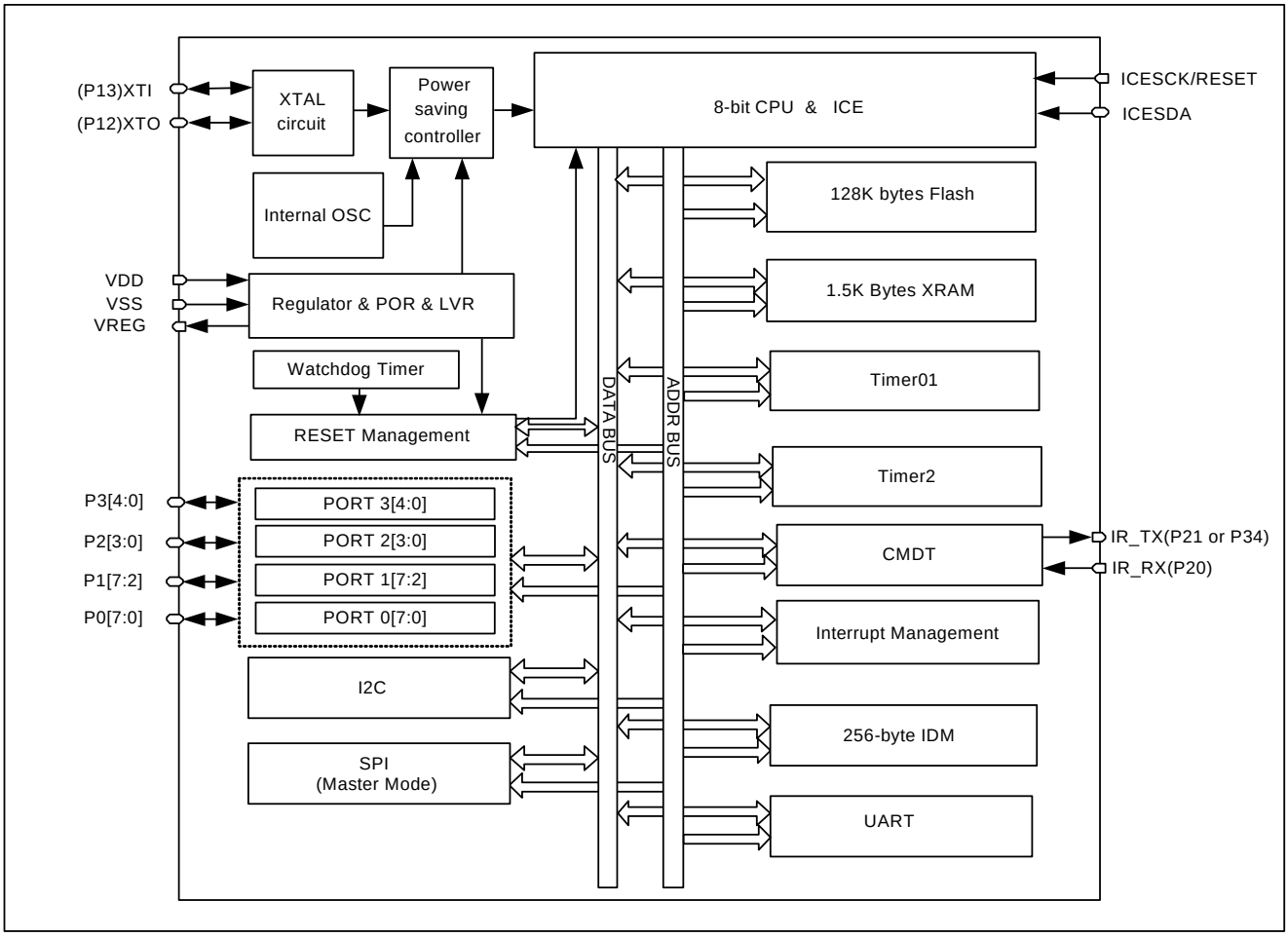
- **CPU**
  - High speed, high performance 1T 8051
    - 100% software compatible with industry standard 8051
    - Pipeline RISC architecture enhances executing instructions 10 times faster than standard 8051
  - Up to 16MHz clock operation
- **Memories**
  - 1.5K bytes XRAM
  - 256 bytes internal Data Memory (IDM) SRAM
  - Up to 128/64/32/18K bytes Flash with high endurance
    - Minimum of 100K progam/erase cycles
    - Minimum of 10 years data retention
    - Page size 1kB
  - Programming lock level for software security
- **Clock Management**
  - Internal oscillator: 16MHz±1.5% @ 2.0V~5.5V
  - Crystal input with 1MHz~16MHz
- **Slow Clock**
  - Internal oscillator: 4KHz
- **Power Management**
  - One STOP mode for power saving
  - One IDLE mode for only peripheral operation
- **Interrupt Management**
  - Up to 9 internal interrupt sources
  - Up to 5 external interrupt sources
  - Up to 8 keyboard Interrupt sources
- **Reset Management**
  - Power On Reset (POR)
  - Low Voltage Reset (LVR)
  - Pad Reset (PAD_RST)
  - Watchdog Reset (WDT_RST)
  - Software Reset (S/W_RST)
  - Stop mode Reset (STOP_RST)
  - Miss Clock Reset (MISS_CLK_RST)
  - Flash Related Error Reset (FLASH_ERR_RST)
- **Programmable Watchdog Timer**
  - A time-base generator
  - An event timer
  - System supervisor
- **I/O Ports**
  - Max. 23 multifunction bi-directional I/Os
    - Each incorporate with pull-up resistor, pull-down resistor, output high, output low or floating input, depending on the settings in the corresponding registers
    - I/O ports with 12mA current sink
    - I/O ports with 12mA current drive
- **Two 16-bit Timer/Counter (Timer 0/1)**
  - Timer mode with clock source selectable
  - Auto reload 8-bit timers
- **One Powerful Timer2 with 16-bit Compare/Capture Unit**
  - Timer mode with clock source selectable
  - Auto reload 16-bit timers
  - Event capturing
  - Digital signals generator
  - Pulse width modulation and measurement
- **UART0**
  - One synchronous mode
  - Three asynchronous modes
- **SPI (master mode)**
  - Programmable phase and polarity of master clock
  - Programmable master clock frequency
  - Auto read/write function
  - Max SPI clock: 4MHz (F_{OSC} /4) @16MHz
- **I2C (master/slave mode)**
- **Carrier Modulator/Demodulator Timer (CMDT)**
  - One 8-bit Timer A for carrier generation and detection
  - One 16-bit Timer B for envelop generation and detection
  - Drives IR_TX pin for remote control communication
  - Receive IR signal from IR_RX pin
- **Built-in Low Voltage Reset**
  - Trigger level: 1.9V
- **Built-in low Voltage Detect**
  - Programmable level: 2.3V, 2.5V, 3.3V, 3.5V

- **On-chip Debug Unit**
- **C compatible Development Tools**

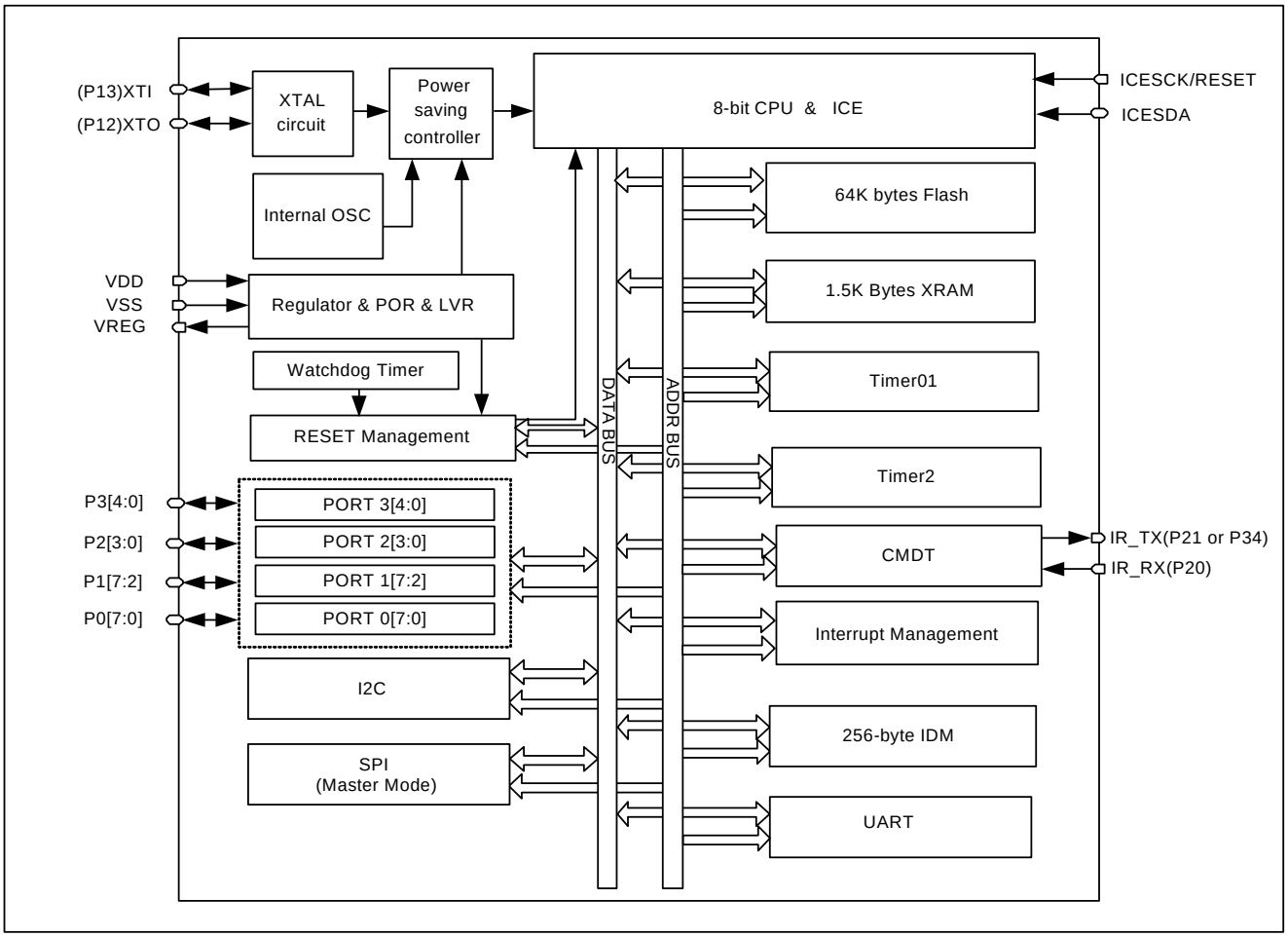
Part NO.	Voltage(V)	Speed (MHz)	Flash (Byte)	IDM (Byte)	XDM (Byte)	CMDT	IR Tx/Rx	CPU OSC.		IO No.	PKG
								INT	XTAL		
GPM8F1129A	1.8~5.5	16	128K	256	1.5k	•	Tx/Rx	•	•	23/15	SSOP30/SSOP20
GPM8F1065A	1.8~5.5	16	64K	256	1.5k	•	Tx/Rx	•	•	23/15	SSOP30/SSOP20
GPM8F1033A	1.8~5.5	16	32K	256	1.5k	•	Tx/Rx	•	•	23/15	SSOP30/SSOP20
GPM8F1019A	1.8~5.5	16	18K	256	1.5k	•	Tx/Rx	•	•	23/15	SSOP30/SSOP20

3. BLOCK DIAGRAM

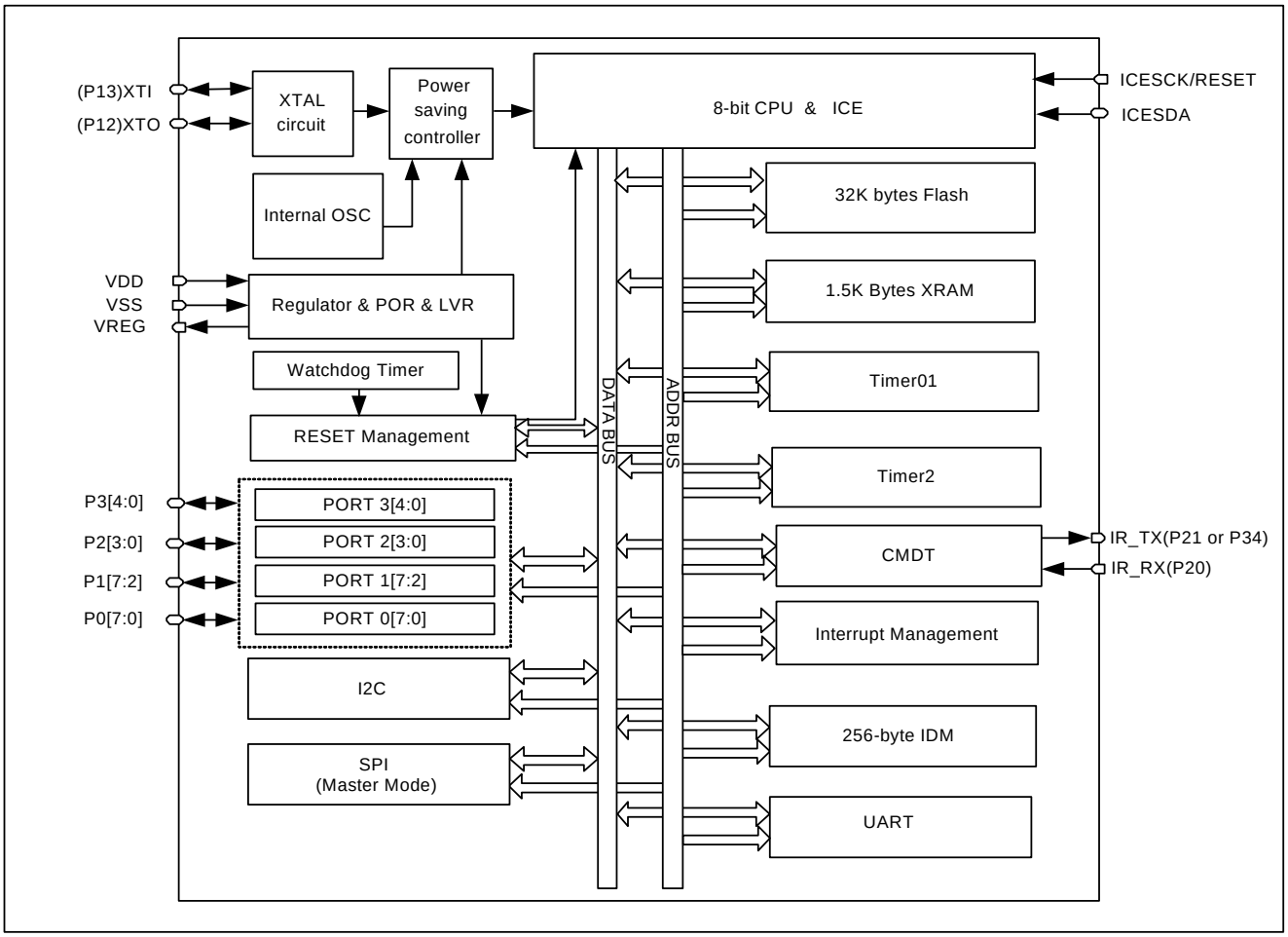
3.1. GPM8F1129A



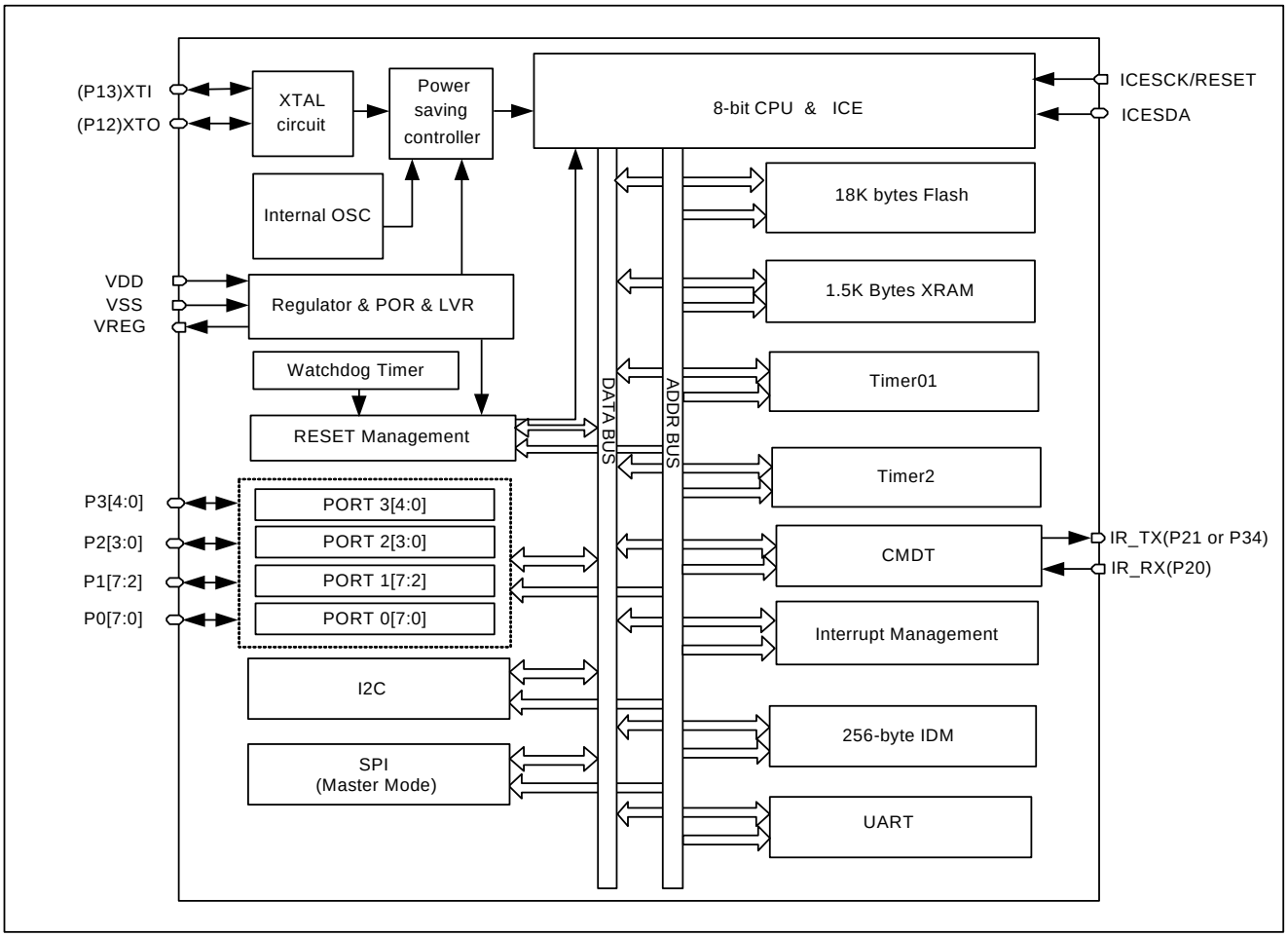
3.2. GPM8F1065A



3.3. GPM8F1033A



3.4. GPM8F1019A



4. SIGNAL DESCRIPTIONS

SSOP30:

Type: I = Input, O = Output, S = Supply

Pin Name	SSOP30	Type	Description
NC	1	NA	Not connected
P23	2	I/O	Port 2's bit 3/ I2CSDA
VREG	3	S	Regulator output
ICESDA	4	I/O	ICE data input/output
ICESCK	5	I/O	ICE clock input/ RESET
P12	6	I/O	Port 1's bit 2/ XTO
VSS	7	S	Ground
P13	8	I/O	Port 1's bit 3/ XTI
VDD	9	S	Power 5V input
P14	10	I/O	Port 1's bit 4/ MOSI
P15	11	I/O	Port 1's bit 5/ SPSCK
P16	12	I/O	Port 1's bit 6/ MISO
P17	13	I/O	Port 1's bit 7/ SPCSB
P30	14	I/O	Port 3's bit 0/ RXD/ INT3
P31	15	I/O	Port 3's bit 1/ TXD/ INT4
P32	16	I/O	Port 3's bit 2/ INT0
P00	17	I/O	Port 0's bit 0/ KBI_0
P01	18	I/O	Port 0's bit 1/ KBI_1
P02	19	I/O	Port 0's bit 2/ KBI_2
P03	20	I/O	Port 0's bit 3/ KBI_3
P04	21	I/O	Port 0's bit 6/ KBI_4
P05	22	I/O	Port 0's bit 7/ KBI_5
P06	23	I/O	Port 0's bit 6/ KBI_6
P07	24	I/O	Port 0's bit 7/ KBI_7
P33	25	I/O	Port 3's bit 3/ INT1
P34	26	I/O	Port 3's bit 4/ INT2/ CMPO/ IR_TX
P20	27	I/O	Port 2's bit 0/ IR_RX
P21	28	I/O	Port 2's bit 1/ IR_TX
P22	29	I/O	Port 2's bit 2/ I2CSCK
NC	30	NA	Not connected

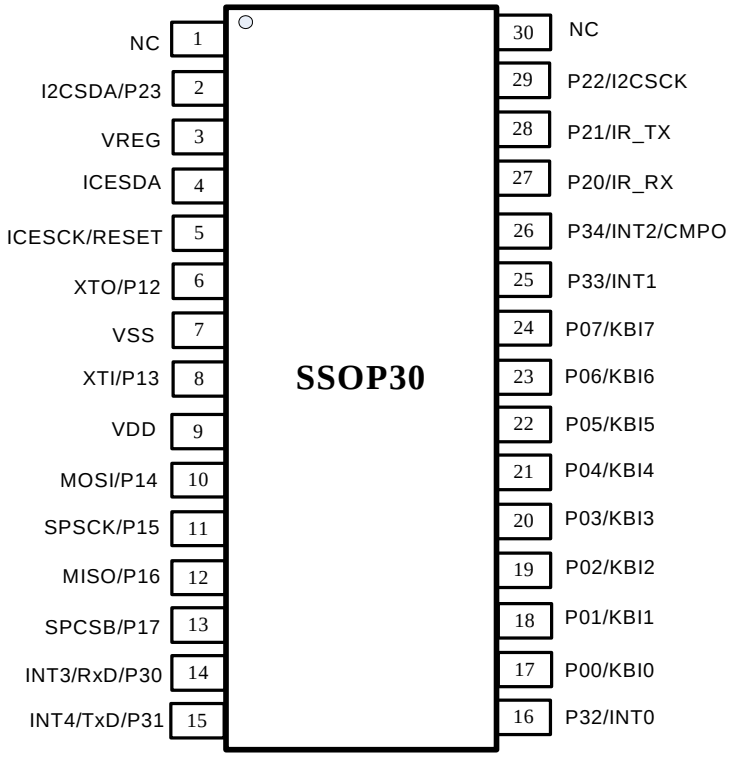
SSOP20:

Type: I = Input, O = Output, S = Supply

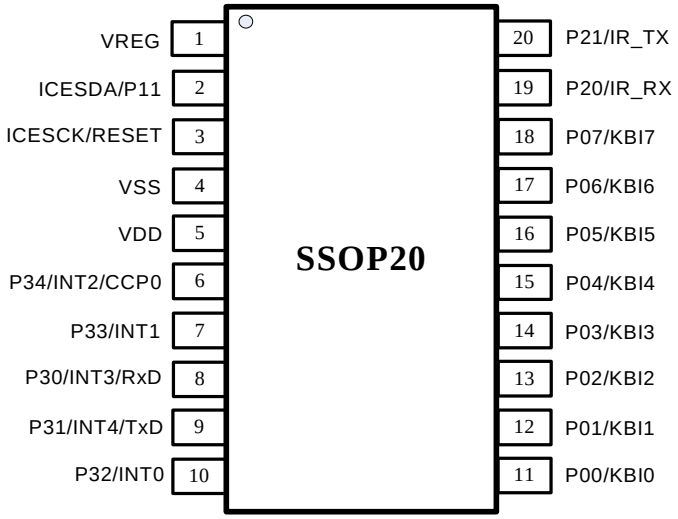
Pin Name	SSOP20	Type	Description
VREG	1	S	Regulator output
ICESDA	2	I/O	ICE data input/output
ICESCK	3	I/O	ICE clock input/ RESET
VSS	4	S	Ground
VDD	5	S	Power 5V input
P34	6	I/O	Port 3's bit 4/ INT2/ CMPO/ IR_TX
P33	7	I/O	Port 3's bit 3/ INT1
P30	8	I/O	Port 3's bit 0/ RXD/ INT3
P31	9	I/O	Port 3's bit 1/ TXD/ INT4
P32	10	I/O	Port 3's bit 2/ INT0
P00	11	I/O	Port 0's bit 0/ KBI_0
P01	12	I/O	Port 0's bit 1/ KBI_1
P02	13	I/O	Port 0's bit 2/ KBI_2
P03	14	I/O	Port 0's bit 3/ KBI_3
P04	15	I/O	Port 0's bit 6/ KBI_4
P05	16	I/O	Port 0's bit 7/ KBI_5
P06	17	I/O	Port 0's bit 6/ KBI_6
P07	18	I/O	Port 0's bit 7/ KBI_7
P20	19	I/O	Port 2's bit 0/ IR_RX
P21	20	I/O	Port 2's bit 1/ IR_TX

4.1. PIN Map

SSOP30:



SSOP20:



Note:

The pins which are not used is SSOP20 must be configured to avoid current leakage.

5. FUNCTION DESCRIPTION

5.1. CPU

The CPU is an ultra-high performance, high speed embedded microcontroller. Pipelined architecture enables the CPU 10 times faster than standard architecture. This performance can also be exploited to great advantage in low power application where the core can be clocked over ten times slower than original implementation for no performance penalty.

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions execution with high performance and high speed.

5.1.1. CPU Features

- ❑ 100 % software compatible with industry 8051
- ❑ 24 times faster multiplication operation
- ❑ 12 times faster addition operation

The CPU is fully compatible with industry standard 8051 microcontroller, maintaining all instruction mnemonics and binary compatibility. It incorporates some great architectural enhancements, allowing the CPU instructions execution with high performance and high speed.

The arithmetic section of the processor performs extensive data manipulation and is comprised of an 8-bit arithmetic logic unit (ALU), an ACC(0xE0) register, B(0xF0) register and PSW(0xD0) register.

5.1.2. Arithmetic Logic Unit (ALU)

The ALU performs the arithmetic and logic operations during one instruction execution. Typical arithmetic operations are addition, subtraction, multiplication and division. Additional operations are such as increment, decrement, BCD-decimal-add-adjust and compare. Within logic unit, operation such as AND, OR, Exclusive OR, complement and rotation are performed. The Boolean processor performs the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry.

5.1.3. Accumulator A register

The accumulation is the 8-bit general-purpose register, which can be operated with data transfer, temporary saving, condition judgment, etc.

5.1.4. B Register

The B register is used during multiplying and dividing operations. In other cases, it may be used as normal SFR.

5.1.5. Program Status Word (PSW)

The PSW contains several bits that reflect the current state of the CPU which is similar to the flag-register of general CPU.

5.1.6. Program Counter (PC)

The program counter is a 16-bit wide register. It consists of two 8-bit registers which are PCH and PCL. This register indicates the address of next instruction to be executed. In Reset state, the content of 0x0000 is stored into program counter.

The GPM8F1129A supports both LARGE mode and FLAT mode. The program counter is a 16-bit register in LARGE mode, but 23-bit register in FLAT mode. Switching between LARGE and FLAT modes is performed by appropriate writing into AM bit of ACON (0x9D) register.

ACC			**Address: 0xE0**		**Accumulator A Register**			
Bit	7	6	5	4	3	2	1	0
Function	ACC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	**Function**	**Type**	**Description**	**Condition**
7:0	ACC[7:0]	R/W	Accumulator A	

Table 5-1 The ACC register

B			Address: 0xF0		B Register			
Bit	7	6	5	4	3	2	1	0
Function	B[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	B[7:0]	R/W	B	

Table 5-2 The B register

PSW			Address: 0xD0		Program Status Word Register			
Bit	7	6	5	4	3	2	1	0
Function	CY	AC	F0	RS1	RS0	OV	F1	P
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CY	R/W	Carry flag	
6	AC	R/W	Auxiliary carry flag	
5	--	R	Reserved	
4:3	RS[1:0]	R/W	Register bank select bits RS[1:0] / Function description 00 / Bank 0, data address 0x00-0x07 01 / Bank 1, data address 0x08-0x0F 10 / Bank 2, data address 0x10-0x17 11 / Bank 3, data address 0x18-0x1F	
2	OV	R/W	Overflow flag	
1	--	R	Reserved	
0	P	R/W	Parity flag	

Table 5-3 The PSW register

ACON			Address: 0x9D		Address Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	AM	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	AM	R/W	Addressing Mode 0: 16-bit Addressing Mode - LARGE 1: 23-bit Contiguous Addressing Mode - FLAT	
0	--	R/W	Reserved	

Table 5-4 The ACON register (GPM8F1129A only)

5.2. Memory

5.2.1. Introduction

The GPM8F1129/1065/1033/1019A has three separated address spaces for program memory and data memory. The program memory is on-chip, re-programmable Flash memory and contains up to 128/ 64/ 32/ 18K bytes spaces. The data memory is divided into 1.5K bytes of external RAM, 256 bytes IDM SRAM with 128 bytes of SFR which can be read and written. The upper IDM and SFR use the same access address in different access ways, described in Figure 5-2.

5.2.2. Program Memory Allocation

The GPM8F1129/ 1065/ 1033/ 1019A implement 128/ 64/ 32/ 18KB program memory size. The program memory allocation is divided into four parts, including first page, normal page, data flash and loader zone. The address space between 0x00000 and 0x03FF is called FIRST_PAGE. It is used for reset vector, IRQ vectors, passwords and CONFIG_BYTE. The CONFIG_BYTE is located in 0x008F of program memory. The content of CONFIG_BYTE also can be read from CONFIG_BYTE register (0xB7) of SFR. The definition of CONFIG_BYTE is shown in Table 5-5. The address space between 0x88 and 0x8b is used for passwords (i.e. PASSWD0~PASSWD3). If CONFIG_BYTE[0] is programmed to be '0', the whole chip memory is protected and any page erase or program by two wire serial interface is not allowed. The only thing user can do is to erase the entire chip. A user can choose to allow or disallow the read operation of whole chip memory in code lock state by setting CONFIG_BYTE[3] to "0". If CONFIG_BYTE[3] is set to "0" and user-entered passwords match contents of PASSWD0~PASSWD3, the whole chip memory can be read even in code lock state. The address space between 0x0400 and 0x01CFFF/0xCFFF/0x4FFF/0x17FF is used for user code area. The last 12K bytes are used for data flash and loader zone.

After each reset, CPU starts execution in the program memory at location 0x0000 or loader zone based on the value of 0x8E in Flash or 0xCF in SFR. The value of JMP_LZ is 0xFF in default, and CPU will jump to loader zone after reset. Each interrupt has its own start address for service routine. The Flash memory can be programmed in-system, through the SCK/SDA interface or by software using the MOVX instruction when PWE= 1. Flash data cannot be programmed from a '0' to a '1', and can only be recognized by erase operation. Therefore, flash data will typically be erased (set to 0xFF) before being programmed. The write and erase operations are executed using PSIDLE (Pseudo-idle) mode to be automatically timed by hardware without data polling to determine the end of the write and erase operation.

For software security consideration, user can set the programmable Flash level by FL_LEVEL register to limit the code area that avoids inadvertently erased or written by software; the protected region is called READONLY_PAGE.

The GPM8F1129/ 1065/ 1033/ 1019A implements three control bytes for boot loader applications (i.e. JMP_LZ, LZ_SEL and DF_SEL). The JMP_LZ/LZ_SEL/DF_SEL is allocated in 0x8E/0x8D/0x8C of program memory. The reset vector of GPM8F1129/ 1065/ 1033/ 1019A can be changed to 0x1FC00/ 0xFC00/ 0x7C00/ 0x4400 by writing #0xFF to JMP_LZ (0x8E of program memory). The LZ_SEL is used to protect the content of loader zone. The DF_SEL is used to protect the content of data flash when CPU is executing loader code. CPU should execute "JLMP 0x1FC00(GMP8F1129A) / 0xFC00(GMP8F1065A) / 0x7C00(GMP8F1033A) / 0x4400(GMP8F1019A)" instruction or write #0xFF to JMP_LZ before executing loader code. The FIRST_PAGE can be programmed or erased, when the loader code is in progress, Table 5-8, Table 5-9 and Table 5-10 show the definition of JMP_LZ, LZ_SEL and DF_SEL respectively.

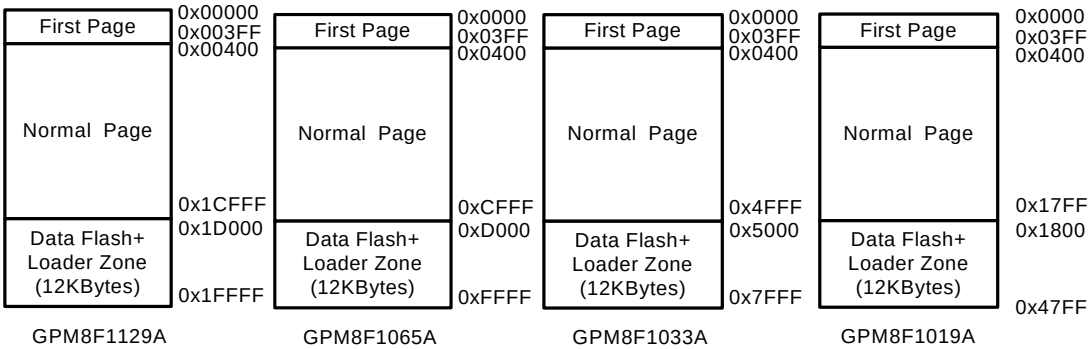


Figure 5-1 Program memory organization

CONFIG_BYTE			Address: 0xB7		CONFIG_BYTE Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	PWENB	--	IOSEL	CODE_UNLOCK
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:4	--	R	Reserved	
3	PWENB	R/W	Password mechanism enable bit 0: Passwords mechanism enable 1: Passwords mechanism disable	
2	--	R	Reserved	
1	IOSEL	R/W	IO initial state selection bit 0: Input pull high 1: floating	
0	CODE_UNLOCK	R/W	Program memory protection enable bits 0: CODE is locked 1: CODE is unlocked	

Note: default value of CONFIG_BYTE = 0xFF

Table 5-5 CONFIG_BYTE description

FL_LEVEL			Address: 0xED		Flash Level Register			
Bit	7	6	5	4	3	2	1	0
Function		FLASH_LEVEL[6:0]						
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	FLASH_LEVEL[6:0]	R/W	FLASH_LEVEL, it determines the number of 1K page is read only, shown in the following table. Note 1. Only FLASH_LEVEL[4:0] is useful in GPM8F1019A Note 2. Only FLASH_LEVEL[4:0] is useful in GPM8F1033A Note 3. Only FLASH_LEVEL[5:0] is useful in GPM8F1065A Note 4. Only FLASH_LEVEL[6:0] is useful in GPM8F1129A	

Table 5-6 The FL_LEVEL register

FLASH_LEVEL	Note	FLASH_LEVEL	Note
0x00	no page is read only	0x40	address < 0x10400 is read only
0x01	address < 0x800 is read only	0x41	address < 0x10800 is read only
0x02	address < 0xC00 is read only	0x42	address < 0x10C00 is read only
0x03	address < 0x1000 is read only	0x43	address < 0x11000 is read only
0x04	address < 0x1400 is read only	0x44	address < 0x11400 is read only
0x05	address < 0x1800 is read only	0x45	address < 0x11800 is read only
0x06	address < 0x1C00 is read only	0x46	address < 0x11C00 is read only
0x07	address < 0x2000 is read only	0x47	address < 0x12000 is read only
0x08	address < 0x2400 is read only	0x48	address < 0x12400 is read only
0x09	address < 0x2800 is read only	0x49	address < 0x12800 is read only

FLASH_LEVEL	Note	FLASH_LEVEL	Note
0x0A	address < 0x2C00 is read only	0x4A	address < 0x12C00 is read only
0x0B	address < 0x3000 is read only	0x4B	address < 0x13000 is read only
0x0C	address < 0x3400 is read only	0x4C	address < 0x13400 is read only
0x0D	address < 0x3800 is read only	0x4D	address < 0x13800 is read only
0x0E	address < 0x3C00 is read only	0x4E	address < 0x13C00 is read only
0x0F	address < 0x4000 is read only	0x4F	address < 0x14000 is read only
0x10	address < 0x4400 is read only	0x50	address < 0x14400 is read only
0x11	address < 0x4800 is read only	0x51	address < 0x14800 is read only
0x12	address < 0x4C00 is read only	0x52	address < 0x14C0 is read only
0x13	address < 0x5000 is read only	0x53	address < 0x15000 is read only
0x14	address < 0x5400 is read only	0x54	address < 0x15400 is read only
0x15	address < 0x5800 is read only	0x55	address < 0x15800 is read only
0x16	address < 0x5C00 is read only	0x56	address < 0x15C00 is read only
0x17	address < 0x6000 is read only	0x57	address < 0x16000 is read only
0x18	address < 0x6400 is read only	0x58	address < 0x16400 is read only
0x19	address < 0x6800 is read only	0x59	address < 0x16800 is read only
0x1A	address < 0x6C00 is read only	0x5A	address < 0x16C00 is read only
0x1B	address < 0x7000 is read only	0x5B	address < 0x17000 is read only
0x1C	address < 0x7400 is read only	0x5C	address < 0x17400 is read only
0x1D	address < 0x7800 is read only	0x5D	address < 0x17800 is read only
0x1E	address < 0x7C00 is read only	0x5E	address < 0x17C00 is read only
0x1F	address < 0x8000 is read only	0x5F	address < 0x18000 is read only
0x20	address < 0x8400 is read only	0x60	address < 0x18400 is read only
0x21	address < 0x8800 is read only	0x61	address < 0x18800 is read only
0x22	address < 0x8C00 is read only	0x62	address < 0x18C00 is read only
0x23	address < 0x9000 is read only	0x63	address < 0x19000 is read only
0x24	address < 0x9400 is read only	0x64	address < 0x19400 is read only
0x25	address < 0x9800 is read only	0x65	address < 0x19800 is read only
0x26	address < 0x9C00 is read only	0x66	address < 0x19C00 is read only
0x27	address < 0xA000 is read only	0x67	address < 0x1A000 is read only
0x28	address < 0xA400 is read only	0x68	address < 0x1A400 is read only
0x29	address < 0xA800 is read only	0x69	address < 0x1A800 is read only
0x2A	address < 0xAC00 is read only	0x6A	address < 0x1AC00 is read only
0x2B	address < 0xB000 is read only	0x6B	address < 0x1B000 is read only
0x2C	address < 0xB400 is read only	0x6C	address < 0x1B400 is read only
0x2D	address < 0xB800 is read only	0x6D	address < 0x1B800 is read only
0x2E	address < 0xBC00 is read only	0x6E	address < 0x1BC00 is read only
0x2F	address < 0xC000 is read only	0x6F	address < 0x1C000 is read only
0x30	address < 0xC400 is read only	0x70	address < 0x1C400 is read only
0x31	address < 0xC800 is read only	0x71	address < 0x1C800 is read only
0x32	address < 0xCC00 is read only	0x72	address < 0x1CC00 is read only
0x33	address < 0xD000 is read only	0x73	address < 0x1D000 is read only
0x34	address < 0xD400 is read only	0x74	address < 0x1D400 is read only
0x35	address < 0xD800 is read only	0x75	address < 0x1D800 is read only
0x36	address < 0xDC00 is read only	0x76	address < 0x1DC00 is read only

FLASH_LEVEL	Note	FLASH_LEVEL	Note
0x37	address < 0xE000 is read only	0x77	address < 0x1E000 is read only
0x38	address < 0xE400 is read only	0x78	address < 0x1E400 is read only
0x39	address < 0xE800 is read only	0x79	address < 0x1E800 is read only
0x3A	address < 0xEC00 is read only	0x7A	address < 0x1EC00 is read only
0x3B	address < 0xF000 is read only	0x7B	address < 0x1F000 is read only
0x3C	address < 0xF400 is read only	0x7C	address < 0x1F400 is read only
0x3D	address < 0xF800 is read only	0x7D	address < 0x1F800 is read only
0x3E	address < 0xFC00 is read only	0x7E	address < 0x1FC00 is read only
0x3F	address < 0x10000 is read only	0x7F	address < 0x20000 is read only

Table 5-7 The description of FL_LEVEL register

JMP_LZ			Address: 0x008E (Program Memory)		Jump to Loader Zone Control Register			
Bit	7	6	5	4	3	2	1	0
Function	JMP_LZ[7:0]							
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	JMP_LZ[7:0]	R/W	CPU jumps to loader zone control bits #0x55: After each reset, CPU starts execution in the program memory at location 0x0000 #0xFF: After each reset, CPU starts execution in the program memory at location 0x1FC00 (GPM8F1129A)/ 0xFC00(GPM8F1065A)/ 0x7C00(GPM8F1033A)/ 0x4400(GPM8F1019A)	

Table 5-8 The JMP_LZ register

LZ_SEL			Address: 0x008D (Program Memory)		Loader Zone Area Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	LZ_SEL[2:0]		
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:3	--	R	Reserved	
2:0	LZ_SEL[2:0]	R/W	Loader zone area control bits GPM8F1129A: 000 No loader zone selected 001 The size of loader zone is 1K bytes (0x1FC00~0x1FFFF) and it cannot be programmed by software. 010 The size of loader zone is 2K bytes (0x1F800~0x1FFFF) and it cannot be programmed by software. 011 The size of loader zone is 3K bytes (0x1F400~0x1FFFF) and it cannot be programmed by software.	

Bit	Function	Type	Description	Condition
			100 The size of loader zone is 4K bytes (0x1F000~0x1FFFF) and it cannot be programmed by software.	
			GPM8F1065A:	
			000 No loader zone selected	
			001 The size of loader zone is 1K bytes (0xFC00~0xFFFF) and it cannot be programmed by software.	
			010 The size of loader zone is 2K bytes (0xF800~0xFFFF) and it cannot be programmed by software.	
			011 The size of loader zone is 3K bytes (0xF400~0xFFFF) and it cannot be programmed by software.	
			100 The size of loader zone is 4K bytes (0xF000~0xFFFF) and it cannot be programmed by software.	
			GPM8F1033A:	
			000 No loader zone selected	
			001 The size of loader zone is 1K bytes (0x7C00~0x7FFF) and it cannot be programmed by software.	
			010 The size of loader zone is 2K bytes (0x7800~0x7FFF) and it cannot be programmed by software.	
			011 The size of loader zone is 3K bytes (0x7400~0x7FFF) and it cannot be programmed by software.	
			100 The size of loader zone is 4K bytes (0x7000~0x7FFF) and it cannot be programmed by software.	
			GPM8F1019A:	
			000 No loader zone selected	
			001 The size of loader zone is 1K bytes (0x4400~0x47FF) and it cannot be programmed by software.	
			010 The size of loader zone is 2K bytes (0x4000~0x47FF) and it cannot be programmed by software.	
			011 The size of loader zone is 3K bytes (0x3C00~0x47FF) and it cannot be programmed by software.	
			100 The size of loader zone is 4K bytes (0x3800~0x47FF) and it cannot be programmed by software.	

Table 5-9 The LZ_SEL register

DF_SEL			Address: 0x008C (Program Memory)		Data Flash Area Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	DF_SEL[3:0]			
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:4	--	R	Reserved	
3:0	DF_SEL[2:0]	R/W	Data flash area control bits. The data flash cannot be programmed when loader code is in progress. GPM8F1129A: 0000 No loader zone and data flash selected	

Bit	Function	Type	Description	Condition
			0001 The size of loader zone + data flash is 1K bytes (0x1FC00~0x1FFFF). 0010 The size of loader zone + data flash is 2K bytes (0x1F800~0x1FFFF). 0011 The size of loader zone + data flash is 3K bytes (0x1F400~0x1FFFF). 0100 The size of loader zone + data flash is 4K bytes (0x1F000~0x1FFFF). 0101 The size of loader zone + data flash is 5K bytes (0x1EC00~0x1FFFF). 0110 The size of loader zone + data flash is 6K bytes (0x1E800~0x1FFFF). 0111 The size of loader zone + data flash is 7K bytes (0x1E400~0x1FFFF). 1000 The size of loader zone + data flash is 8K bytes (0x1E000~0x1FFFF). 1001 The size of loader zone + data flash is 9K bytes (0x1DC00~0x1FFFF). 1010 The size of loader zone + data flash is 10K bytes (0x1D800~0x1FFFF). 1011 The size of loader zone + data flash is 11K bytes (0x1D400~0x1FFFF). 1100 The size of loader zone + data flash is 12K bytes (0x1D000~0x1FFFF). GPM8F1065A: 0000 No loader zone and data flash selected 0001 The size of loader zone + data flash is 1K bytes (0xFC00~0xFFFF). 0010 The size of loader zone + data flash is 2K bytes (0xF800~0xFFFF). 0011 The size of loader zone + data flash is 3K bytes (0xF400~0xFFFF). 0100 The size of loader zone + data flash is 4K bytes (0xF000~0xFFFF). 0101 The size of loader zone + data flash is 5K bytes (0xEC00~0xFFFF). 0110 The size of loader zone + data flash is 6K bytes (0xE800~0xFFFF). 0111 The size of loader zone + data flash is 7K bytes (0xE400~0xFFFF). 1000 The size of loader zone + data flash is 8K bytes (0xE000~0xFFFF). 1001 The size of loader zone + data flash is 9K bytes (0xDC00~0xFFFF). 1010 The size of loader zone + data flash is 10K bytes (0xD800~0xFFFF).	

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>1011</td><td>The size of loader zone + data flash is 11K bytes (0xD400~0xFFFF).</td></tr>
<tr><td>1100</td><td>The size of loader zone + data flash is 12K bytes (0xD000~0xFFFF).</td></tr>
</table>
GPM8F1033A:
<table>
<tr><td>0000</td><td>No loader zone and data flash selected</td></tr>
<tr><td>0001</td><td>The size of loader zone + data flash is 1K bytes (0x7C00~0x7FFF).</td></tr>
<tr><td>0010</td><td>The size of loader zone + data flash is 2K bytes (0x7800~0x7FFF).</td></tr>
<tr><td>0011</td><td>The size of loader zone + data flash is 3K bytes (0x7400~0x7FFF).</td></tr>
<tr><td>0100</td><td>The size of loader zone + data flash is 4K bytes (0x7000~0x7FFF).</td></tr>
<tr><td>0101</td><td>The size of loader zone + data flash is 5K bytes (0x6C00~0x7FFF).</td></tr>
<tr><td>0110</td><td>The size of loader zone + data flash is 6K bytes (0x6800~0x7FFF).</td></tr>
<tr><td>0111</td><td>The size of loader zone + data flash is 7K bytes (0x6400~0x7FFF).</td></tr>
<tr><td>1000</td><td>The size of loader zone + data flash is 8K bytes (0x6000~0x7FFF).</td></tr>
<tr><td>1001</td><td>The size of loader zone + data flash is 9K bytes (0x5C00~0x7FFF).</td></tr>
<tr><td>1010</td><td>The size of loader zone + data flash is 10K bytes (0x5800~0x7FFF).</td></tr>
<tr><td>1011</td><td>The size of loader zone + data flash is 11K bytes (0x5400~0x7FFF).</td></tr>
<tr><td>1100</td><td>The size of loader zone + data flash is 12K bytes (0x5000~0x7FFF).</td></tr>
</table>
GPM8F1019A:
<table>
<tr><td>0000</td><td>No loader zone and data flash selected</td></tr>
<tr><td>0001</td><td>The size of loader zone + data flash is 1K bytes (0x4400~0x47FF).</td></tr>
<tr><td>0010</td><td>The size of loader zone + data flash is 2K bytes (0x4000~0x47FF).</td></tr>
<tr><td>0011</td><td>The size of loader zone + data flash is 3K bytes (0x3C00~0x47FF).</td></tr>
<tr><td>0100</td><td>The size of loader zone + data flash is 4K bytes (0x3800~0x47FF).</td></tr>
<tr><td>0101</td><td>The size of loader zone + data flash is 5K bytes (0x3400~0x47FF).</td></tr>
<tr><td>0110</td><td>The size of loader zone + data flash is 6K bytes (0x3000~0x47FF).</td></tr>
<tr><td>0111</td><td>The size of loader zone + data flash is 7K bytes (0x2C00~0x47FF).</td></tr>
</table>
</td><td></td></tr>
</table>

Bit	Function	Type	Description		Condition
			1000	The size of loader zone + data flash is 8K bytes (0x2800~0x47FF).	
			1001	The size of loader zone + data flash is 9K bytes (0x2400~0x47FF).	
			1010	The size of loader zone + data flash is 10K bytes (0x2000~0x47FF).	
			1011	The size of loader zone + data flash is 11K bytes (0x1C00~0x47FF).	
			1100	The size of loader zone + data flash is 12K bytes (0x1800~0x47FF).	

Table 5-10 The DF_SEL register

FLASHCON			Address: 0xB7		Flash Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	P_ERASE	PROG
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1	P_ERASE	R/W	Flash page erase enable bit 0: Flash page erase is disabled 1: Flash page erase is enabled	
0	PROG	R/W	Flash program enable bit 0: Flash program is disabled 1: Flash program is enabled	

Table 5-11 The FLASHCON register

5.2.3. Data Memory Allocation

Data memory address allocations on the GPM8F1129/ 1065/ 1033/ 1019A are divided into two parts. The first part is 1.5K bytes of external RAM and the second one is 256 byte IDM shown in Figure 5-2. The lowest internal data memory (IDM) consists of four register banks with eight registers each. A bit addressable segment with 128 bits (16 bytes) begins at 0x20. The address from 0x30 to 0x7F is not defined and can be utilized freely by user.

The last 128 bytes of data memory can be used by different addressing modes. With the indirect addressing mode, address from 0x80 to 0xFF shared with stack space is addressed. With the direct addressing mode, the SFR addressing from 0x80 to 0xFF is accessed. The SFR memory map is shown in Table 5-12.

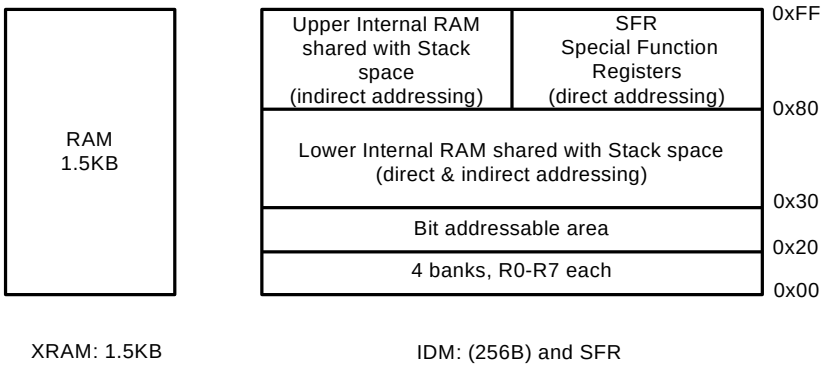


Figure 5-2 Data memory organization

Note1: Black: standard 8051 register; gray: additional register;

0xF8	EIP	IOSCCON	IOSCT0	IOSCT1	SPICON	SPITXD	SPIRXD	BODYID
0xF0	B							
0xE8	EIE	EXIPOL	EXIMOD	KEYCODE	FLASHCON	FL_LEVEL		
0xE0	ACC	P0_SC	P3_SC	P0_TKEY	P3_TKEY	TKEY_XOR		
0xD8	WDCON		I2CCON	I2CSTS	I2CADR	I2CDAT	I2CDEB	
0xD0	PSW							
0xC8	T2CON	T2IF	CRCL	CRCH	TL2	TH2	CCEN	JMP_LZ
0xC0	CCL	CCH						
0xB8	IP	CMPO_INV	TMBIF	MARKL	MARKH	SPACEL	SPACEH	RXCON
0xB0	P3	CMDTCON	CAPCON	TMAIF	PERIOD	DUTY	WKUEN	CONFIG_BYTE
0xA8	IE	KBIEN	P0_PU	P0_PD	P1_PU	P1_PD	SYSCON0	SYSCON1
0xA0	P2		P3_PU	P3_PD		SRCON	FLASHERRF	
0x98	SCON0	SBUF0				ACON	P2_PU	P2_PD
0x90	P1	EIF		DPX0	RSTSTS	DPX1	BIP	BIF
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	RSTCON
0x80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F

Table 5-12 SFR memory map

5.2.4. Memory Related SFR

The following sub-sections describe program, external and internal memories related SFRs of 8051 core and their functionality. For other information about standard SFRs, please refer to appropriate peripheral section.

5.2.4.1. Program write enable bit

The Program Write Enable (PWE) bit, located in PCON register bit 4, is used during MOVX instructions. When PWE bit is set to logic 1, the MOVX @DPTR, an instruction writes data located in accumulator register into program memory addressed by DPTR register. Program memory can only be read by MOVC regardless of PWE bit.

5.2.4.2. Data pointer registers

Dual data pointer registers are implemented to speed up data block copy. DPTR0 and DPTR1 are located in four SFR addresses. Active DPTR register is selected by SEL bit (DPS[0]). If SEL=0, DPTR0 is selected, else DPTR1.

5.2.4.3. Stack pointer

The 8051 has 8-bit stack pointer called SP (0x81) located in the internal RAM space. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution. In the other words, it always points to the last valid stack byte. The SP is accessed as any other SFRs. Figure 5-3 shows an example when PUSH A is executed and Figure 5-4 shows an example when POP PSW is executed.

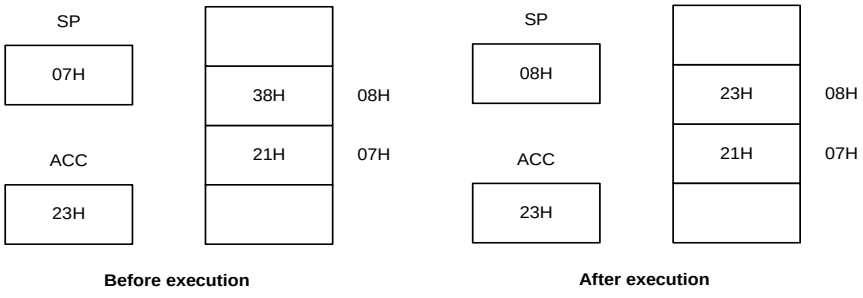


Figure 5-3 Stack byte order for PUSH A instruction

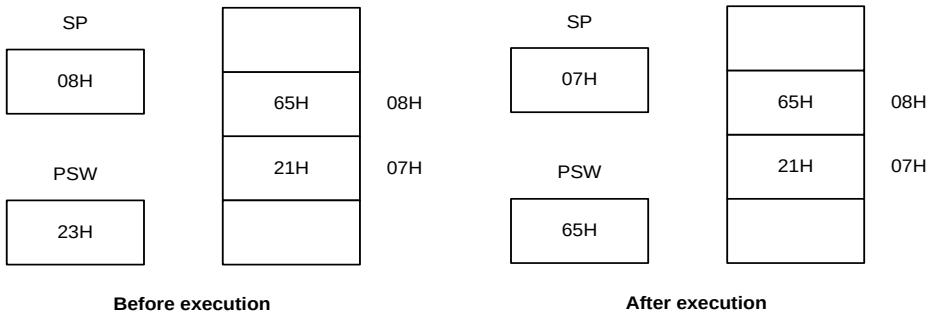


Figure 5-4 Stack byte order for POP PSW instruction

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-13 The PCON register

DPH0			Address: 0x83		Data Pointer Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[15:8]	R/W	Data pointer register DPTR0 - high byte	

Table 5-14 The DPH0 register

DPL0			Address: 0x82		Data Pointer Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[7:0]	R/W	Data pointer register DPTR0 - low byte	

Table 5-15 The DPL0 register

DPX0			Address: 0x93		Data Pointer Extended Register			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[23:16] (GPM8F1129/1065A only)							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR0[23:16]	R/W	Data pointer extended register	

Table 5-16 The DPX0 register

DPH1			Address: 0x85		Data Pointer 1 Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[15:8]	R/W	Data pointer 1 register DPTR1 - high byte	

Table 5-17 The DPH1 register

DPL1			Address: 0x84		Data Pointer 1 Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	DPTR0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[7:0]	R/W	Data pointer 1 register DPTR1 - low byte	

Table 5-18 The DPL1 register

DPX1			Address: 0x95		Data Pointer Extended 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	DPTR1[23:16] (GPM8F1129/1065A only)							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DPTR1[23:16]	R/W	Data pointer extended 1 register	

Table 5-19 The DPX1 register

DPS			Address: 0x86		Data Pointer Select Register			
Bit	7	6	5	4	3	2	1	0
Function	ID1	ID0	TSL	-	-	-	-	SEL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	ID[1:0]	R/W	Increment/decrement function selection. See Table 5-21	
5	TSL	R/W	Toggle select enable bit 0: DPTR related instructions do not affect state of SEL bit 1: DPTR related instructions to toggle the SEL bit	
4:1	--	R/W	Reserved	
0	SEL	R/W	Active data pointer select bit See Table 5-21	

Table 5-20 The DPS register

ID1	ID0	SEL=0	SEL=1
0	0	INC DPTR0	INC DPTR1
0	1	DEC DPTR0	INC DPTR1
1	0	INC DPTR0	DEC DPTR1
1	1	DEC DPTR0	DEC DPTR1

Table 5-21 DPTR0/DPTR1 operations

SP			Address: 0x81		Stack Pointer Register			
Bit	7	6	5	4	3	2	1	0
Function	SP[7:0]							
Default	0	0	0	0	0	1	1	1

Bit	Function	Type	Description	Condition
7:0	SP[7:0]	R/W	Stack pointer	

Table 5-22 The SP register

5.3. Special Function Registers (SFR)

GPM8F1129/1065/1033/1019A has up to 94 control registers for special function registers. All of the SFRs are used by MCU and peripheral function block for controlling the desired operation. Some of the SFRs contain control and status bits for peripheral module such as Timer unit, Interrupt control unit, etc. Some of bits in SFRs are read only, so writing to those bits will not have any effect on corresponding bits. Some SFRs have key code design that KEYCODE register must be written with correct key codes, in sequence, before writing a value to it for software security reason. The following table shows the summary of the SFRs. The detailed information of each SFRs are explained in each peripheral section.

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0x80	P0		0xFF	Port 0							
0x81	SP		0x07	Stack Pointer							
0x82	DPL0		0x00	Data pointer register DPTR0 — low byte							
0x83	DPH0		0x00	Data pointer register DPTR0 — high byte							
0x84	DPL1		0x00	Data pointer register DPTR1 — low byte							
0x85	DPH1		0x00	Data pointer register DPTR1 — high byte							
0x86	DPS		0x00	ID1	ID0	TSL	--	--	--	--	SEL
0x87	PCON		0x00	SMOD0	SMOD1	CPU_ IDLE	PWE	STOP_RST _EN	--	STOP	--
0x88	TCON		0x00	TF1	TR1	TF0	TR0	IE1	--	IE0	--
0x89	TMOD		0x00	--	--	M11	M10	--	--	M01	M00
0x8A	TL0		0x00	Timer 0 Load value – low byte							
0x8B	TL1		0x00	Timer 1 Load value – low byte							
0x8C	TH0		0x00	Timer 0 Load value – high byte							
0x8D	TH1		0x00	Timer 1 Load value – high byte							
0x8E	CKCON		0x01	WD1	WD0	WDFM	T1M	T0M	--	--	--
0x8F	RSTCON	4F,72,7A	0x10	DF_EP_ ENB	LZ_EP_ ENB	FLASH_FLOW _ ENB	XADDR_ENB	FP_EP_ENB	CHIP_E_ ENB	MISS_CLK_ ENB	FLASH_ERR _ ENB
0x90	P1		0xff	P17	P16	P15	P14	P13	P12	--	--
0x91	EIF		0x00	KBIF	--	--	--	LVDF	INT4F	INT3F	INT2F
0x93	DPX0		0x00	Data pointer extended register(GPM8F1129/1065A only)							
0x94	RSTSTS		0x00	--	MISS_CLK _RST	STOP_ RST	FLASH_ ERR_RST	S/W_RST	WDT_RST	LVR_RST	RAD_RST
0x95	DPX1		0x00	Data pointer extended 1 register(GPM8F1129/1065A only)							
0x96	BIP		0x00	--	--	--	--	--	PTMB	PTMA	PI2C
0x97	BIF		0x00	--	--	--	--	--	TMBIF	TMAIF	--
0x98	SCON0		0x00	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
0x99	SBUF0		0x00	UART 0 buffer							
0x9D	ACON	AA,55	0x00	--	--	--	--	--	--	AM	--
0x9E	P2_PU		0x00	--	--	--	--	P23_PU	P22_PU	P21_PU	P20_PU
0x9F	P2_PD		0x00	--	--	--	--	P23_PD	P22_PD	P21_PD	P20_PD
0xA0	P2		0xFF	--	--	--	--	P223	P22	P21	P20
0xA2	P3_PU		0x00	--	--	--	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
0xA3	P3_PD		0x00	--	--	--	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
0xA5	SRCON		0x0F	--	--	--	--	P3_SR	P2_SR	P1_SR	P0_SR
0xA6	FLASHERRF		0x00	DF_EP_ F	LZ_EP_ F	FLASH_ FLOW_F	XADDR_F	FP_EP_F	CHIP_E_F	--	--

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xA8	IE		0x00	EA	ECCP	ET2	ES0	ET1	EX1	ET0	EX0
0xA9	KBIEN		0x00	KBIEN[7:0]							
0xAA	P0_PU		0x00	P07_PU	P06_PU	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
0xAB	P0_PD		0x00	P07_PD	P06_PD	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD
0xAC	P1_PU		0x00	P17_PU	P16_PU	P15_PU	P14_PU	P13_PU	P12_PU	--	--
0xAD	P1_PD		0x00	P17_PD	P16_PD	P15_PD	P14_PD	P13_PD	P12_PD	--	--
0xAE	SYSCON0	FF,00	0x00	LVD_STATUS	LVDENB	LVDSEL1	LVDSEL0	LVRENB	CLKOUT_EN	--	--
0xAF	SYSCON1		0x00	--	--	ADorDA	SPI_EN	I2CEN	I2C_AUTO_RW	IRTX_SW	--
0xB0	P3		0xFF	--	--	--	P34	P33	P32	P31	P30
0xB1	CMDTCON		0x00	IRTX_EN	TX_STATE	ENVDET	EXSPC	PWM_MODE	POLARITY	TMBEN	TMAEN
0xB2	CAPCON		0x00	CAPB_MODE	CAPB_EN	TMB_DIV[1:0]		RXOUT_INV	CAPA_MODE	TMA_DIV[1:0]	
0xB3	TMAIF		0x00	--	--	--	CAPAIF	TMAOIF	FALLIF	RISEIF	TMAIE
0xB4	PERIOD		0x00	PERIOD[7:0]							
0xB5	DUTY		0x00	DUTY[7:0]							
0XB6	WKUEN	AF,50	0x9F	KB_WKUEN	WD_WKUEN	--	INT4_WKUEN	INT3_WKUEN	INT2_WKUEN	INT1_WKUEN	INT0_WKUEN
0xB7	CONFIG_BYTE		0xFF	--	--	--	--	PWENB	--	IOSEL	CODE_UNLOCK
0xB8	IP		0x00	--	--	PT2	PS0	PT1	PX1	PT0	PX0
0xB9	CMPO_INV		0x00	--	--	--	--	--	--	--	CC_INVEN
0xBA	TMBIF		0x00	ENVDETIF	MASK_oe	FCAPBIF	RCAPBIF	TMBOIF	SPACEIF	MARKIF	TMBIE
0xBB	MARKL		0x00	MARK[7:0]							
0xBC	MARKH		0x00	MARK[15:8]							
0xBD	SPACEL		0x00	SPACE[7:0]							
0xBE	SPACEH		0x00	SPACE[15:8]							
0XBF	RXCON		0x00	--	RXOUT	FILTER_SEL[1:0]		--	--	--	--
0xC0	CCL		0x00	Timer2cc capture low byte							
0xC1	CCH		0x00	Timer2cc capture high byte							
0xC8	T2CON		0x00	T2PS	I3FR	--	T2R	--	T2CM	--	T2I
0xC9	T2IF		0x00	--	--	--	CCF	--	--	--	TF2
0xCA	CRCL		0x00	CRC register – Low byte							
0xCB	CRCH		0x00	CRC register – High Byte							
0xCC	TL2		0x00	Timer 2 Load value – low byte							
0xCD	TH2		0x00	Timer 2 Load value – high byte							
0xCE	CCEN		0x01	--	--	--	--	--	--	CM	--
0xCF	JMP_LZ		0xFF	JMP_LZ[7:0]							
0xD0	PSW		0x00	CY	AC	--	RS1	RS0	OV	--	P
0xD8	WDCON	AA,55	0x00	--	--	--	--	WDIF	--	EWT	RWT
0xDA	I2CCON		0x00	ACKEN	CLKSEL	I2CIE	I2CIF	TXCLK[3:0]			
0xDB	I2CSTS		0x00	MODE[1:0]		BUSY	DataEN	ArbS	SS	GC	ACK
0xDC	I2CADR		0x00	Addr[7:1]							--
0xDD	I2CDAT		0x00	Data[7:0]							
0xDE	I2CDEB		0x00	DEBCLK[7:0]							
0xE0	ACC		0x00	ACC register							
0xE1	P0_SC		0x00	P0_SC[7:0]							
0xE2	P3_SC		0x00	--	--	--	P3_SC[4:0]				

Addr	Function	Key Code	Reset Value	7	6	5	4	3	2	1	0
0xE3	P0_TKEY			P0_TKEY[7:0]							
0xE4	P3_TKEY			--	--	--	P3_TKEY[4:0]				
0xE5	TKEY_XOR			--	--	--	--	--	--	--	TKEY_XOR
0xE8	EIE		0x00	EKBI	--	EWDI		ELVD	EINT4	EINT3	EINT2
0xE9	EXIPOL		0x00	--	--	--	INT4POL	INT3POL	INT2POL	INT1POL	INT0POL
0xEA	EXIMOD		0x00	--	--	--	INT4MOD	INT3MOD	INT2MOD	INT1MOD	INT0MOD
0xEB	KEYCODE		0x00	KEYCODE[7:0]							
0xEC	FLASHCON		0x00	--	--	--	--	--	--	P_ERASE	PROG
0xED	FL_LEVEL		0xFF	--	FLASH_LEVEL[6:0]						
0xF0	B		0x00	B register							
0xF8	EIP		0x00	PKBI	--	PWDI	--	PLVD	PINT4	PINT3	PINT2
0xF9	IOSCCON		0x00	--	--	XTAL_PAD_EN	--	OSC_SEL	--	CLKDIV[1:0]	
0xFA	IOSCT0		0x00	--	--	--	--	--		XFCN[1:0]	
0xFB	IOSCT1			--	--	OSC_TRIM[6:0]					
0xFC	SPICON		0x00	PO_LARITY	PHASE	SPI_CLK_SEL[1:0]		CSB_KEEP	--	SPI_RD	SPI_START
0xFD	SPITXD		0x00	SPI TX Data[7:0]							
0xFE	SPIRXD		0x00	SPI RX Data[7:0]							
0xFF	BODYID										

5.4. Power Saving Mode

5.4.1. Introduction

Although GPM8F1129/1065/1033/1019A is a high-speed microcontrollers designed for maximum performance, it also provide Power Management Unit (PMU) with two advanced power conservation modes. These modes are IDLE mode, and STOP mode. In order to reduce the current consumption when system does not need to be active, STOP mode can be utilized. For more information about these two modes, please see the following two sections.

5.4.2. IDLE mode

The IDLE mode reduces power consumption by turning off the clock provided to the microcontroller, causing MCU to stop to execute following instruction. IDLE mode is entered by setting the CPU_IDLE bit (PCON[5]). In this mode, peripheral clock is not turned off, so peripheral device can still work normally.

5.4.3. STOP mode

STOP mode is the lowest power states that the microcontroller can enter. It is achieved by cutting-off frequency provided to SYSCLK, resulting in a fully static condition. No processing is possible, timers are stopped, and no serial communication is executed. Processor operation will be postponed on the instruction that sets the STOP bit. STOP mode can be exited in the following ways:

A non-clocked interrupt such as the external interrupts INT0-INT4 and keyboard/key-scan IO can be used. Except for watchdog timer, other clocked interrupts such as internal timers, and serial ports do not operate in STOP mode. Processor operation will resume with the fetching of the interrupt vector associated with the interrupt that causes the exit from STOP mode. When the interrupt service routine is completed, RETI returns the program to the instruction immediately following the one that invoked the STOP mode. When INT0-INT4 and keyboard/key-scan IO are used for wakeup source, WKUEN register must be set which tabled in Table 5-25. There are two selections of the place of instruction execution after wakeup when entering STOP mode and the control bit is in PCON[3]. If STOP_RST_EN is set to '1', reset state will take place after wakeup, otherwise, next instruction will be executed.

	System Clock	Peripheral clock	Wakeup source	After wakeup
RUN Mode	Register setting	Register setting	--	--
IDLE Mode	OFF	ON	1. All wakeup sources 2. All interrupt sources	Next instruction state
STOP Mode	OFF	OFF	1. All wakeup sources	Reset state or next instruction state base on PCON[3]

Table 5-23 Three operation modes for GPM8F1129/1065/1033/1019A

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-24 The PCON register

WKUEN			Address: 0xB6		Wake Up Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	KB_WKUEN	WD_WKUEN	--	INT4_WKUEN	INT3_WKUEN	INT2_WKUEN	INT1_WKUEN	INT0_WKUEN
Default	1	0	0	1	1	1	1	1
Key Code	0xAF, 0x50							

Bit	Function	Type	Description	Condition
7	KB_WKUEN	R/W	Keyboard / key-scan pin wake up enable control	
6	WD_WKUEN	R/W	Watchdog wakeup enable control	
5	--	R/W	Reserved	
4	INT4_WKUEN	R/W	INT4 PAD wakeup enable control, active high	
3	INT3_WKUEN	R/W	INT3 PAD wakeup enable control, active high	
2	INT2_WKUEN	R/W	INT2 PAD wakeup enable control, active high	
1	INT1_WKUEN	R/W	INT1 PAD wakeup enable control, active high	
0	INT0_WKUEN	R/W	INT0 PAD wakeup enable control, active high	

Table 5-25 The WKUEN register

5.5. Interrupt System

The GPM8F1129/1065/1033/1019A provides up to five external interrupt sources, nine internal interrupt sources and eight keyboard change interrupt sources. Each external interrupt pin can be set enable/disable, edge/level and polarity trigger and individually. The keyboard change interrupt is activated at any transition on keyboard inputs which user selects in KBIEN (0xA9). User should read P0 for latching P0 status before setting EKBI bit of EIE(0xE8). GPM8F1129/1065/1033/1019A also equips two levels of interrupt priority control. Interrupt requests are sampled each system clock at the rising edge of clock control. Each interrupt vector can be individually enabled or disabled by setting or clearing a corresponding bit in the special function registers (SFRs). The IE contains global interrupt system disable(0) / enable(1) bit called EA. In general, once an interrupt event occurs, the corresponding flag bit will be set. The related registers of interrupt flag are described as below.

If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and then CPU executes service routine. If the related interrupt control bit is disabled, programmer can still observe the corresponding flag bit, but no interrupt request signal will be generated. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine. With any instruction, interrupts pending during the previous instruction is served. Before entering interrupt service routine, the system saves the current PC address into top of stack pointer and jumps to corresponding vector to execute the interrupt service. After finishing the interrupt service, the system abstract the return PC address from the top of the stack to execute the following instruction. For more details, please refer to related block.

Interrupt flag	Function	Active level/edge	Flag resets	Vector	Vector number	Priority
IE0	Device pin INT 0	Falling/Rising/Low/High	Hardware	0x03	0	1
TF0	Internal Timer 0	-	Hardware	0x0B	1	2
IE1	Device pin INT 1	Falling/Rising/Low/High	Hardware	0x13	2	3
TF1	Internal Timer 1	-	Hardware	0x1B	3	4
TI0 & RI0	Internal UART0	-	Software(cleared by 0)	0x23	4	5
TMAOIF	Internal Timer A	-	Software(cleared by 0)	0x2B	5	6
TMBOIF	Internal Timer B	-	Software(cleared by 0)	0x33	6	7
T2IF	Internal Timer 2	-	Software(cleared by 0)	0x3B	7	8
KBIF	Keyboard pin Key-scan pin	-	Software(cleared by 0) Software(cleared by 0)	0x43	8	9
INT2F	Device pin INT 2	Falling/Rising/Low/High	Software(cleared by 0)	0x4B	9	10
I2CIF	Internal I2C	-	Software(cleared by 0)	0x53	10	11
LVDF	Low Voltage Detection	-	Software(cleared by 0)	0x5B	11	12
INT3F	Device pin INT 3	Falling/Rising/Low/High	Software(cleared by 0)	0x63	12	13
INT4F	Device pin INT 4	Falling/Rising/Low/High	Software(cleared by 0)	0x6B	13	14
WDIF	Internal Watchdog	-	Software(cleared by 0)	0x73	14	15

IP			Address: 0xB8		Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	PT2	PS0	PT1	PX1	PT0	PX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5	PT2	R/W	Timer 2 priority level control (1: high level)	
4	PS0	R/W	UART0 priority level control (1: high level)	
3	PT1	R/W	Timer 1 priority level control (1: high level)	
2	PX1	R/W	INT1 priority level control (1: high level)	

Bit	Function	Type	Description	Condition
1	PT0	R/W	Timer 0 priority level control (1: high level)	
0	PX0	R/W	INT0 priority level control (1: high level)	

Table 5-26 IP register

EIP			Address: 0xF8		Extended Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	PKBI	--	PWDI	--	PLVD	PINT4	PINT3	PINT2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	PKBI	R/W	Keyboard interrupt level control (1: high level)	
6	--	R/W	Reserved	
5	PWDI	R/W	Watchdog priority level control (1: high level)	
4	--	R/W	Reserved	
3	PLVD	R/W	LVD priority level control (1: high level)	
2	PINT4	R/W	INT4 priority level control (1: high level)	
1	PINT3	R/W	INT3 priority level control (1: high level)	
0	PINT2	R/W	INT2 priority level control (1: high level)	

Table 5-27 EIP register

BIP			Address: 0x96		Additional Interrupt Priority Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	PTMB	PTMA	PI2C
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	PTMB	R/W	Timer B priority level control (1: high level)	
1	PTMA	R/W	Timer A priority level control (1: high level)	
0	PI2C	R/W	IC2 priority level control (1: high level)	

Table 5-28 BIP register

IE			Address: 0xA8		Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EA	ECCP	ET2	ES0	ET1	EX1	ET0	EX0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EA	R/W	Enable global interrupts	
6	ECCP	R/W	Enable Timer2 compare/capture interrupts	
5	ET2	R/W	Enable Timer2 interrupt	
4	ES0	R/W	Enable UART0 interrupt	
3	ET1	R/W	Enable Timer 1 interrupt	
2	EX1	R/W	Enable INT1 interrupt	
1	ET0	R/W	Enable Timer 0 interrupt	

Bit	Function	Type	Description	Condition
0	EX0	R/W	Enable INT0 interrupt	

Table 5-29 IE register

EIE			Address: 0xE8		Extended Interrupt Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	EKBI	-	EWDI	--	ELVD	EINT4	EINT3	EINT2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	EKBI	R/W	Enable keyboard/key-scan pin interrupt	
6	--	R/W	Reserved	
5	EWDI	R/W	Enable watchdog interrupt	
4	--	R/W	Reserved	
3	ELVD	R/W	Enable LVD interrupts	
2	EINT4	R/W	Enable INT4 interrupts	
1	EINT3	R/W	Enable INT3 interrupts	
0	EINT2	R/W	Enable INT2 interrupts	

Table 5-30 EIE register

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	--	IE0	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled ; 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled ; 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	--	R/W	Reserved	
1	IE0	R/W	INT0 interrupt flag	
0	--	R/W	Reserved	

Table 5-31 TCON register

TMAIF			Address: 0xB3		Timer A Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	CAPAIF	TMAOIF	FALLIF	RISEIF	TMAIE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	CAPAIF	R/W	Timer A capture flag	

Bit	Function	Type	Description	Condition
3	TMAOIF	R/W	Timer A overflow flag	
2	FALLIF	R/W	Falling edge flag of carrier output	
1	RISEIF	R/W	Rising edge flag of carrier output	
0	TMAIE	R/W	Timer A interrupt enable bit	

Table 5-32 TMAIF register

TMBIF			Address: 0xBA		Timer B Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	ENVDETIF	MASK_oe	FCAPBIF	RCAPBIF	TMBOIF	SPACEIF	MARKIF	TMBIE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ENVDETIF	R/W	ENVDET rising and falling flag	
6	MASK_oe	R/W	Timer B capture flag masking enable bit 0: RCAPBIF, FCAPBIF is not masked 1: RCAPBIF, FCAPBIF is masked	
5	FCAPBIF	R/W	Timer B falling capture flag	
4	RCAPBIF	R/W	Timer B rising capture flag	
3	TMBOIF	R/W	Timer B overflow flag	
2	SPACEIF	R/W	Space flag when count of timer B is matched to space register	
1	MARKIF	R/W	Mark flag when count of timer B is matched to mark register	
0	TMBIE	R/W	Timer B interrupt enable bit	

Table 5-33 TMBIF register

EIF			Address: 0x91		Extended Interrupt Flag			
Bit	7	6	5	4	3	2	1	0
Function	KBIF	--	--	--	LVDF	INT4F	INT3F	INT2F
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	KBIF	R/W	Keyboard pin (P00~P07) change/ key-scan pin interrupt flag	
6:4	--	R/W	Reserved	
3	LVDF	R/W	LVD interrupt flag	
2	INT4F	R/W	INT4 interrupt flag	
1	INT3F	R/W	INT3 interrupt flag	
0	INT2F	R/W	INT2 interrupt flag	

Table 5-34 EIF register

BIF			Address: 0x97		Additional interrupt flag			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	TMBIF	TMAIF	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:3	--	R/W	Reserved	
2	TMBIF	R	Timer B interrupt flag, cleared by 0 in TMBIF register	
1	TMAIF	R	Timer A interrupt flag, cleared by 0 in TMAIF register	
0	--	R/W	Reserved	

Table 5-35 BIF register

EXIPOL			Address: 0xE9		External Interrupt Polarity Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	INT4POL	INT3POL	INT2POL	INT1POL	INT0POL
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	INT4POL	R/W	INT4 polarity select 0: Falling edges/ low level 1: Rising edges/ high level	
3	INT3POL	R/W	INT3 polarity select 0: Falling edges/ low level 1: Rising edges/ high level	
2	INT2POL	R/W	INT2 polarity select 0: Falling edges/ low level 1: Rising edges/ high level	
1	INT1POL	R/W	INT1 polarity select 0: Falling edges/ low level 1: Rising edges/ high level	
0	INT0POL	R/W	INT0 polarity select 0: Falling edges/ low level 1: Rising edges/ high level	

Table 5-36 EXIPOL register

EXIMODE			Address: 0xEA		External Interrupt Mode Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	INT4MOD	INT3MOD	INT2MOD	INT1MOD	INT0MOD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	INT4MOD	R/W	INT4 detection mode 0: Edge-only detection. 1: Edge-and-level detection.	
3	INT3MOD	R/W	INT3 detection mode 0: Edge-only detection. 1: Edge-and-level detection.	
2	INT2MOD	R/W	INT2 detection mode 0: Edge-only detection. 1: Edge-and-level detection.	

Bit	Function	Type	Description	Condition
1	INT1MOD	R/W	INT1 detection mode 0: Edge-only detection. 1: Edge-and-level detection.	
0	INT0MOD	R/W	INT0 detection mode 0: Edge-only detection. 1: Edge-and-level detection.	

Table 5-37 EXIMOD register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable; 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA; 1: Reset	

Table 5-38 WDCON register

SCON0			Address: 0x98		UART0 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-39 SCON0 register

KBIEN			Address: 0xA9		Keyboard Pin Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	KBIEN[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	KBIEN[7:0]	R/W	Keyboard pin enable 0: Set KBIx function disable, 1: Set KBIx function enable	

Table 5-40 KBIEN register

I2CCON			Address: 0xDA		I2C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	ACKEN	CLKSEL	I2CIE	I2CIF	TXCLK[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ACKEN	R/W	I2C-bus acknowledgement enable bit 0: Disable ACK generation 1: Enable ACK generation	
6	CLKSEL	R/W	Source clock of I2C-bus transmit clock pre-scaler (scaling unit) selection bit 0: I2CCLK=SYSCLK/16" 1: I2CCLK= SYSCLK /512"	
5	I2CIE	R/W	I2C Bus TX/RX Interrupt Enable 0: Disable 1: Enable	
4	I2CIF	R/W	I2C Bus TX/RX Interrupt Flag Clear by the software A I2C bus interrupt occurs 1. When a 1-byte transmitting or receiving operation is terminated. 2. When a general call or slave address match occurs. 3. If bus arbitration fails.	
3:0	TXCLK[3:0]	R/W	I2C-Bus transmit clock pre-scaler. Transmit clock frequency is determined by this 4-bit pre-scaler value, according to the following formula: TX clock = I2CCLK/(TXCLK[7:4]+1) **NOTES:** 1. I2CCLK is determined by CLKSEL	

Table 5-41 I2CCON register

5.6. Reset Source

5.6.1. Introduction

There are eight types of reset sources for the GPM8F1129/1065/1033/1019A: Power-On Reset (POR), Low Voltage Reset (LVR), Pad Reset (RAD_RST), Watchdog Timer Reset (WDT_RST), Software Reset (S/W_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Figure 5-5 shows the block diagram of each reset source.

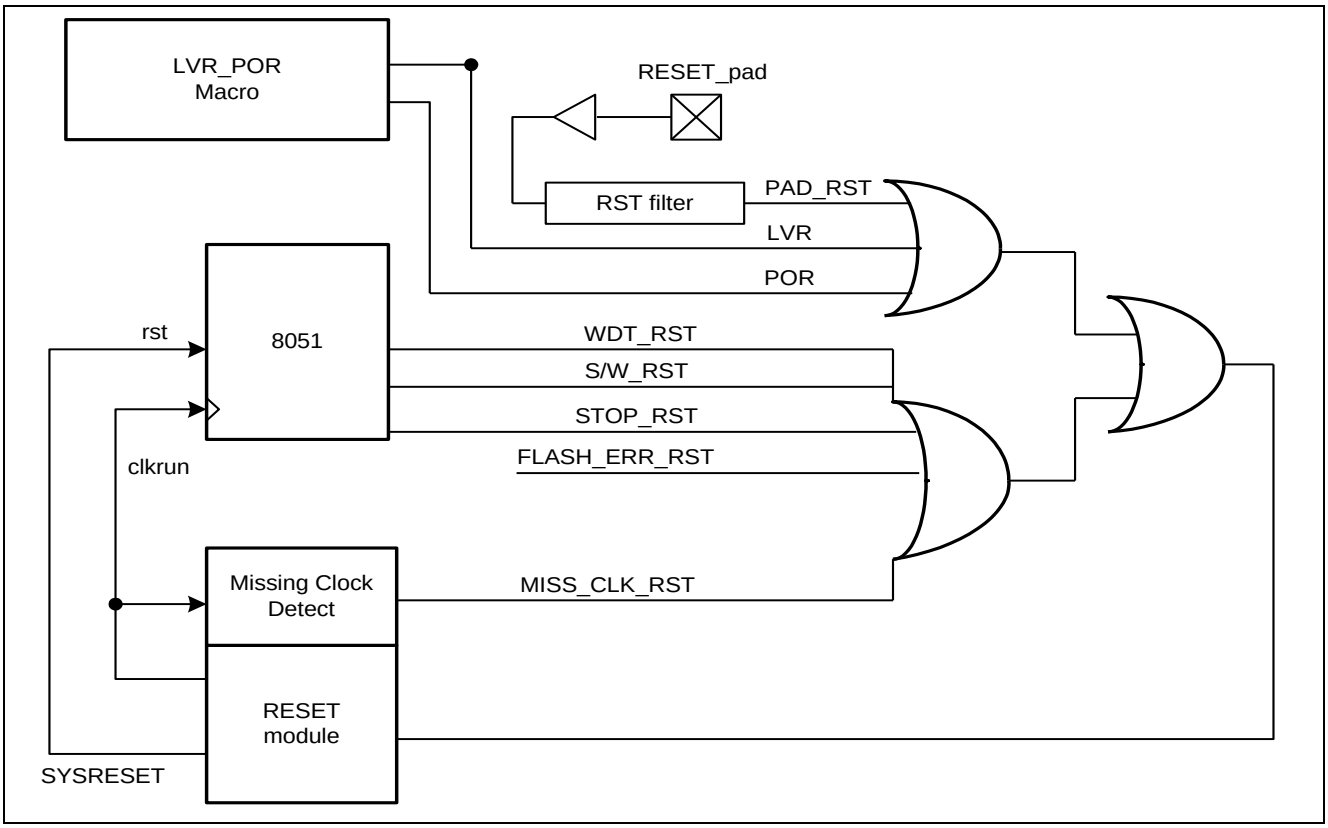


Figure 5-5 Reset sources

5.6.2. Power-On Reset (POR)

A POR is generated when VDD is rising from 0v. When VDD rises to an acceptable level (~1.5V), the power on reset circuit will start a power-on sequence. After that, the system starts to activate and will operate in target speed. The POR will reset whole chip and registers.

5.6.3. Low Voltage Reset (LVR)

The on-chip Low Voltage Reset (LVR) circuitry forces the system entering reset state when power supplying voltage falls below the specific LVR trigger voltage. This function prevents MCU from working at an invalid operating voltage range. To enable or disable this function, the related enable bit can be set. If this function is enabled, the LVR circuit will monitor power level while chip is operating. And the LVR voltage level is 1.9V. If the power is lower than the specific level for a certain period of time, the system reset will take place and go to initial state.

5.6.4. Low Voltage Detection (LVD)

In order to allow software to notify early that a power failure is about to occur, the LVD flag bit can be monitored. Built-in voltage detection circuit controls the LVD flag. The LVD flag is set while VDD supply is below LVD voltage and is cleared when the VDD supply is over LVD voltage. The LVD voltage can be 2.3V, 2.5V, 3.3V or 3.5V by setting LVDSEL[1:0] bits.

5.6.5. Pad Reset (PAD_RST)

The GPM8F1129/1065/1033/1019A provides an external pin to force the system returning to its initial status. The RESET pin is high active as shown in Figure 5-6. When the RESET pin equals to VDD for over 1ms, system will be forced to enter reset state, execute instruction from address 0x0000 or loader zone based on the value of 0x8E in Flash or 0xCF in SFR and all registers go to default state.

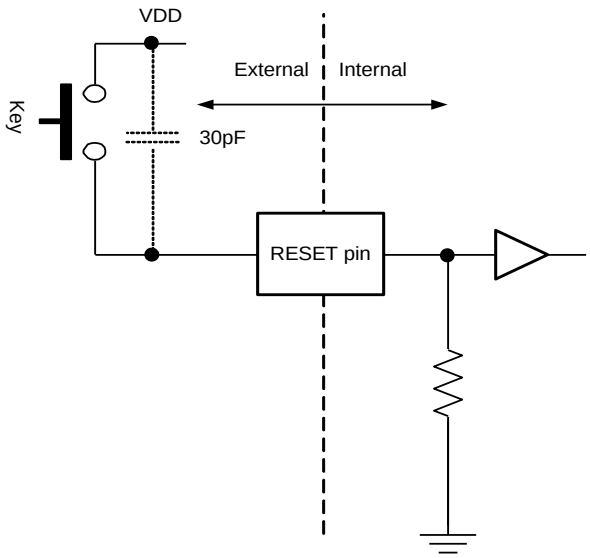


Figure 5-6 Pad reset circuit

5.6.6. Watchdog Timer Reset (WDT_RST)

On-chip watchdog circuitry makes the device entering reset state when MCU goes into unknown state and has no watchdog cleared information. This function prevents the MCU to be stuck in an abnormal condition. The WDT can be enabled or disabled through WDCON register bit 1. At any time prior to reaching its user selected terminal value, software can set the Reset Watchdog Timer (WDCON[0]) bit. If RWT is set before the timeout is reached, the timer will start over. If timeout is reached without RWT being set, the watchdog will reset the CPU. Hardware will automatically clear RWT after software sets it. When the reset occurs, the Watchdog Timer Reset Flag (RSTSTS[2]) will automatically be set to indicate the cause of the reset, however software must clear this bit manually.

WDCON register is a key code design register that prevent it from accidental writes. KEYCODE register is located at 0xEB. Correct sequence, 0xAA and 0x55, is required before write to WDCON register. Reading from such register is not protected. The Watchdog has four timeout selections based on the internal 16K clock frequency. Therefore, the actual timeout interval is dependent on the SYSCLK frequency. The selections are a pre-selected number of clocks and can be set by CKCON[7:6]. In addition, CKCON[5] can be used to set these four timeout selections in fast mode or not, which is implemented in GPM8F1129/1065A only. When CPU wakeups from ILDE mode or STOP mode, software needs to delay about 100us to enter ILDE mode or STOP mode again due to 1T of 16KHz clock source. Figure 5-7 shows the block diagram of Watchdog timer.

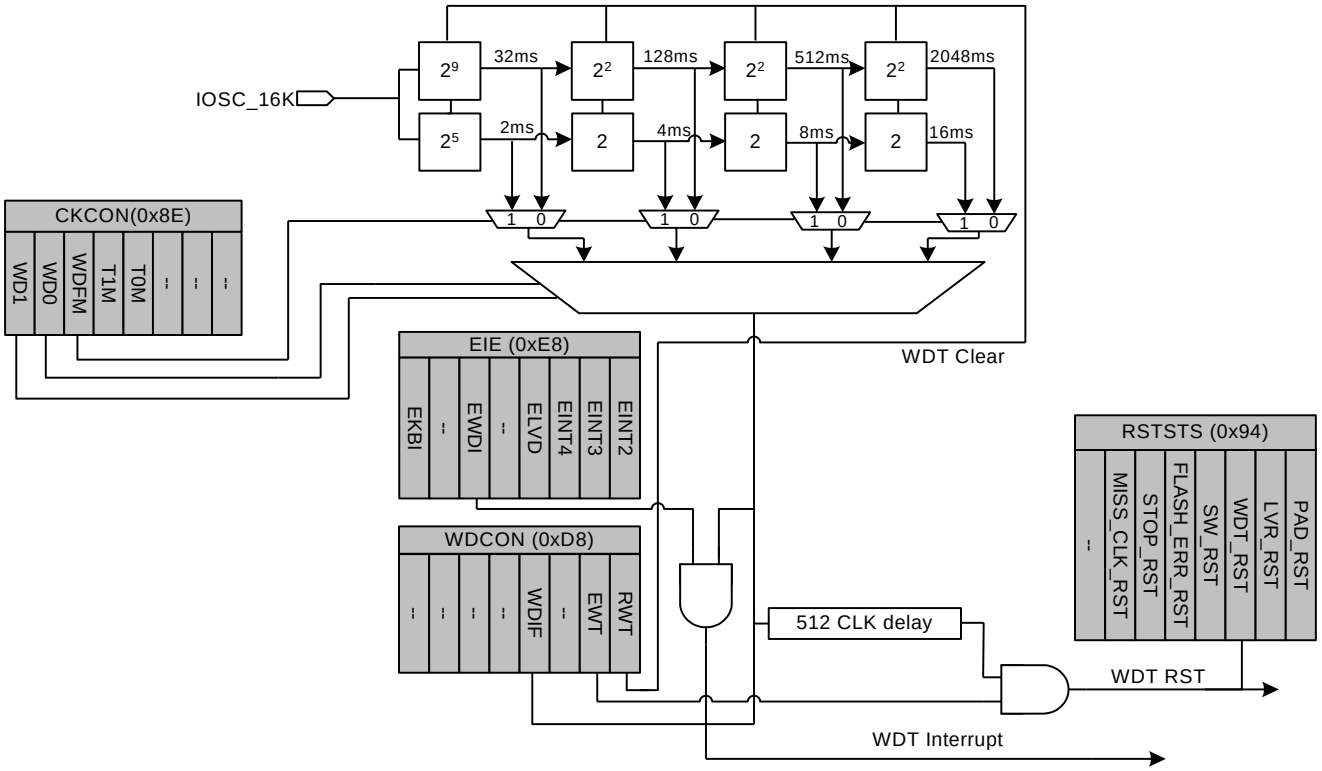


Figure 5-7 The block diagram of Watchdog timer

5.6.7. Other Reset Sources

Other reset sources include Software Reset (S/W_RST), STOP mode Reset (STOP_RST), Flash Error Reset (FLASH_ERR_RST), and missing system clock Reset (MISS_CLK_RST). Software Reset triggers when writing KEY code to KEYCODE register. The key codes are 0x3c and 0xc3. The timing does not matter, but the key codes must be written in order before SW reset takes place. STOP mode Reset is enabled by setting PCON[3] bit. This is the reset when system is reset from STOP mode. Flash Error Reset is the reset when six flash related errors arise. The first error is to execute whole chip erase by software. The second error is to erase/program first page. The third error is access the wrong address. The forth error occurs when flash is programmed in a wrong way. The fifth error is erase/program pure loader zone and the sixth error is to erase/program data flash or loader zone. Each flash error related reset source can be enabled or disabled by clearing or setting a bit in the RSTCON(0x94) as shown in Table 5-47. The corresponding flag when flash error reset occurs can be observed in FLASHERRF register which is shown in Table 5-48. Missing system clock Reset is the reset when system clock is missed over 4095 IOSC clocks if external crystal is utilized as clock source. There are seven reset status flag can be monitored by RSTSTS register which is shown as Table 5-49.

SYSCON0			**Address: 0xAE**		**SYSTEM control0 Register**			
Bit	7	6	5	4	3	2	1	0
Function	LVD_STATUS	LVDENB	LVDSEL1	LVDSEL0	LVRENB	CLKOUT_EN	--	--
Default	0	0	0	0	0	0	0	0
Key Code	FF,00							

Bit	Function	Type	Description	Condition
7	LVD_STATUS	R	LVD status	
6	LVDENB	R/W	LVD enable control 0: enable LVD function 1: disable LVD function	

Bit	Function	Type	Description	Condition
5:4	LVDSEL[1:0]	R/W	LVD voltage selection bits 00: 2.3V 01: 2.5V 10: 3.3V 11: 3.5V	
3	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P34)	
1:0	--	R/W	Reserved	

Table 5-42 SYSCON0 register

WDCON			Address: 0xD8		Watchdog Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	WDIF	--	EWT	RWT
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	WDIF	R/W	Watchdog interrupt flag	
2	--	R/W	Reserved	
1	EWT	R/W	Watchdog timer reset enable bit 0: Disable 1: Enable	
0	RWT	R/W	Reset watchdog timer 0: NA 1: Reset	

Table 5-43 WDCON register

KEYCODE			Address: 0xEB		KEYCODE Register			
Bit	7	6	5	4	3	2	1	0
Function	Keycode register							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
0	KEYCODE[7:0]	R/W	Keycode register	

Note: Some protected registers are required to write correct key code to KEYCODE register before writing data to them.

Table 5-44 KEYCODE register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	0	0	1

<table>
<tr><th>Bit</th><th>Function</th><th>Type</th><th>Description</th><th>Condition</th></tr>
<tr><td>7:6</td><td>WD[1:0]</td><td>R/W</td><td>Watchdog timeout selection bits
If WDFM=0:<table><tr><th>WD[1:0]</th><th>Timeout</th></tr><tr><td>00</td><td>32ms</td></tr><tr><td>01</td><td>128ms</td></tr><tr><td>10</td><td>512ms</td></tr><tr><td>11</td><td>2048ms</td></tr></table>If WDFM=1: (GPM8F1129/1065A only)<table><tr><th>WD[1:0]</th><th>Timeout</th></tr><tr><td>00</td><td>2ms</td></tr><tr><td>01</td><td>8ms</td></tr><tr><td>10</td><td>16ms</td></tr><tr><td>11</td><td>32ms</td></tr></table></td><td></td></tr>
<tr><td>5</td><td>WDFM</td><td>R/W</td><td>Watchdog fast mode selection bit (GPM8F1129/1065A only)
0: watchdog fast mode is disabled
1: watchdog fast mode is enabled</td><td></td></tr>
<tr><td>4</td><td>T1M</td><td>R/W</td><td>Division selection of the system clock that drives Timer 1
0: Timer 1 uses a system clock frequency
1: Timer 1 uses a divided-by-2 of the system clock frequency</td><td></td></tr>
<tr><td>3</td><td>T0M</td><td>R/W</td><td>Division selection of the system clock that drives Timer 0
0: Timer 0 uses a system clock frequency
1: Timer 0 uses a divide-by-2 of the system clock frequency</td><td></td></tr>
<tr><td>2:0</td><td>--</td><td>R/W</td><td>Reserved</td><td></td></tr>
</table>

Table 5-45 CKCON register

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	

Bit	Function	Type	Description	Condition
0	--	R/W	Reserved	

Table 5-46 PCON register

RSTCON			Address: 0x8F		Flash Error RESET Enable Control Register			
Bit	7	6	5	4	3	2	1	0
Function	DF_EP_ ENB	LZ_EP_ENB	FLASH_FLOW_ ENB	XADDR_ENB	FP_EP_ENB	CHIP_E_ENB	MISS_CLK_ENB	FLASH_ERR_ _ENB
Default	0	0	0	1	0	0	0	0
Key Code	4F,72,7A							

Bit	Function	Type	Description	Condition
7	DF_EP_ ENB	R/W	Data flash or loader zone erase/program reset disable control bit 0: enable 1: disable	
6	LZ_EP_ ENB	R/W	Loader zone erase/program reset disable control bit 0: enable 1: disable	
5	FLASH_FLOW_ ENB	R/W	Error flash flow/READONLY_PAGE program reset disable control bit 0: enable 1: disable	
4	XADDR_ENB	R/W	Error flash address access reset disable control bit 0: enable 1: disable	
3	FP_EP_ENB	R/W	First page erase/program reset disable control bit 0: enable 1: disable	
2	CHIP_E_ ENB	R/W	Whole chip erase reset disable control bit 0: enable 1: disable	
1	MISS_CLK _ ENB	R/W	Miss clock reset disable control bit (GPM8F1129/1065A only) 0: enable 1: disable	
0	FLASH_ERR _ ENB	R/W	Global Flash related error reset disable control bit 0: enable 1: disable	

Table 5-47 RSTCON register

FLASHERRF			Address: 0xA6		Flash Error RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	DF_EP_ F	LZ_EP_ F	FLASH_FLOW_F	XADDR_F	FP_EP_F	CHIP_E_F	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	DF_EP_ F	R/W	Error data flash or loader zone erase/program reset flag	
6	LZ_EP_ F	R/W	Error loader zone erase/program reset flag	
5	FLASH_FLOW_F	R/W	Error flash flow/ READONLY_PAGE program reset flag	
4	XADDR_F	R/W	Error flash address access reset flag	
3	FP_EP_F	R/W	Error first page erase/program reset flag	
2	CHIP_E_F	R/W	Error Macro erase reset flag	
1	--	R/W	Reserved	
0	--	R/W	Reserved	

Table 5-48 FLASHERRF register

RSTSTS			Address: 0x94		RESET Status Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	MISS_CLK_RST	STOP_RST	FLASH_ERR_RST	S/W_RST	WDT_RST	LVR_RST	RAD_RST
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	MISS_CLK_RST	R/W	RESET from system clock missing clock	
5	STOP_RST	R/W	RESET from STOP mode	
4	FLASH_ERR_RST	R/W	RESET from FLASH error	
3	SW_RST	R/W	RESET from SW RST	
2	WDT_RST	R/W	RESET from WDT	
1	LVR_RST	R/W	RESET from LVR	
0	PAD_RST	R/W	RESET from RESET PAD	

Table 5-49 RSTSTS register

5.7. Clock Source

GPM8F1129/1065/1033/1019A has two clock sources including internal oscillator (16MHz) and external crystal. These two clocks are chosen to be system clock source by controlling related SFR. In addition, a clock divisor for the system clock source is contained to obtain different frequencies. There are four selections totally and can be selected by users. The block diagram of clock source is shown in Figure 5-8.

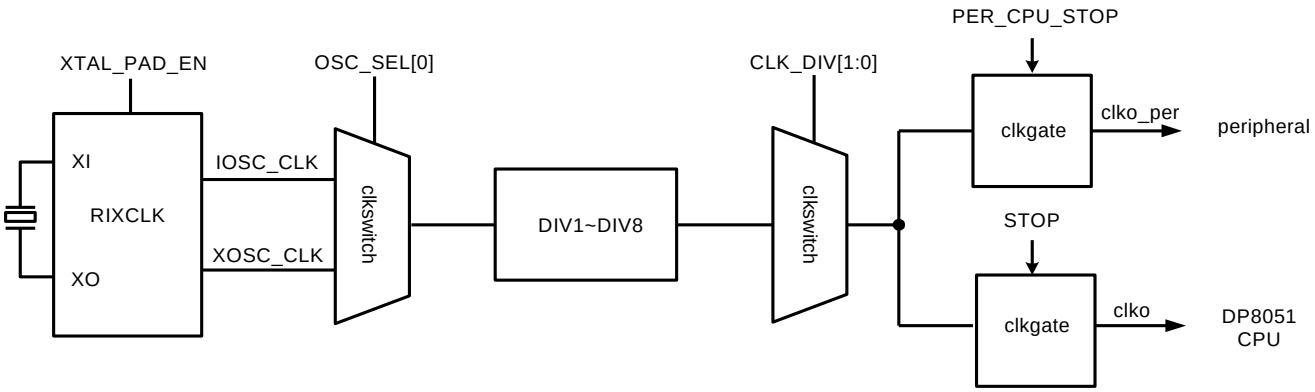


Figure 5-8 The block diagram of clock sources

If crystal mode is utilized, different frequencies can be selected by IOSCT0[1:0] as shown in Table 5-51 and software should delay a period of time according to different crystals for clock stable time.

If internal oscillator mode is utilized, trimming frequencies is possible through IOSCT1[6:0]. Each step of frequency is 0.5%. The IOSCT1 register is shown in Table 5-52.

IOSCCON			Address: 0xF9		IOSC Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	XTAL_PAD_EN	--	OSC_SEL	--	CLKDIV[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description
7:6	--	R/W	Reserved
5	XTAL_PAD_EN	R/W	If using XTAL, XTAL_PAD_EN should be set first for OSC_SEL selection.
4	--	R/W	Reserved

Bit	Function	Type	Description
3	OSC_SEL	R/W	0: Internal ROSC 1: External XTAL If using XTAL, OSC_SEL should be set after XOSC_CLK is stable.
2	--	R/W	Reserved
1:0	CLK_DIV[1:0]	R/W	System Clock source divider CLK_DIV | Clock control 00 | SYSCLK_SOURCE 01 | SYSCLK_SOURCE/2 10 | SYSCLK_SOURCE/4 11 | SYSCLK_SOURCE/8

Table 5-50 The IOSCCON register

IOSCT0			Address: 0xFA		IOSC Timing 0 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--		XFCN[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:3	--	R/W	Reserved	
2:0	XFCN[1:0]	R/W	External XTAL Frequency control bit (XTAL_PAD_EN must be “1”) GPM8F1019A / GPM8F1033A: XFCN | XTAL(HZ) 00 | 1MHz<F<4MHz 01 | 4MHz<F<8MHz 10 | 8MHz<F<12MHz 11 | 12MHz<F<16MHz GPM8F1065A / GPM8F1129A: XFCN | XTAL(HZ) 00 | 1MHz<F<4MHz 01 | 4MHz<F<8MHz 10 | 8MHz<F<16MHz 11 | 16MHz<F<32MHz	

Table 5-51 The IOSCT0 register

IOSCT1			Address: 0xFB		IOSC Timing 1 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	OSC_TRIM[6:0]						
Default								

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6:0	OSC_TUNE[6:0]	R/W	Internal OSC frequency trimming bit, 0.5% each step	

Table 5-52 The IOSCT1 register

SYSCON0			Address: 0xAE		SYSTEM control0 Register			
Bit	7	6	5	4	3	2	1	0
Function	LVD_STATUS	LVDENB	LVDSEL1	LVDSEL0	LVRENB	CLKOUT_EN	--	--
Default	0	0	0	0	0	0	0	0
Key Code	FF, 00							

Bit	Function	Type	Description	Condition
7	LVD_STATUS	R	LVD status	
6	LVDENB	R/W	LVD enable control 0: enable LVD function 1: disable LVD function	
5:4	LVDSEL[1:0]	R/W	LVD voltage selection bits 00: 2.3V 01: 2.5V 10: 3.3V 11: 3.5V	
3	LVRENB	R/W	LVR enable control 0: enable LVR function 1: disable LVR function	
2	CLKOUT_EN	R/W	Clock output enable bit (SYSCLK is output on P34)	
1:0	--	R/W	Reserved	

Table 5-53 SYSCON0 register

5.8. Slow Clock

GPM8F1129/1065/1033/1019A equipped with one internal low-frequency oscillator (4KHz) for slow time interrupt.

5.9. I/O Ports

The GPM8F1129/1065/1033/1019A has four ports, including standard Port 0, Port 1, Port 2 and Port 3. These port pins may be multiplexed with an alternate function for the peripheral features on the device. In general, when an initial reset state occurs, all ports are used as a general purpose input port with open-drain structure. All the ports can be programmable pull high/low by PU and PD registers. The PU and PD registers of Port 0 are controlled by 0xAA and 0xAB, the PU and PD registers of Port 1 are controlled by 0xAC and 0xAD, the PU and PD registers of Port 2 are controlled by 0x9E and 0x9F and the PU and PD registers of P3 are controlled by 0xA2 and 0xA3. Read and write accesses to the I/O port are performed via their corresponding SFRs P0(0x80), P1(0x90), P2(0xA0) and P3(0xB0). When PU and PD are enabled at the same time, the port can output high or low depending on the data. Table 5-54 and Table 5-55 show the truth table of analog pad and digital pad respectively. In GPM8F1129/1065/1033/1019A, P1[3:2] are used for external crystal input and output. The built-in pull high/low resister is 50KΩ. In addition to this, there is a register, SRCON (GPM8F1129/1065A only), for slew rate control (0xA5) of P0~P3. If IO ports are needed to change immediately without slew rate control, the corresponding control bit of each port can be set to '0'. The default state of SRCON register is '0xFF' with 30ns slew rate control. Figure 5-9 and Figure 5-10 show the block diagrams of analog pad and digital pad respectively.

PU	PD	DATA	XTAL_PAD_EN	PAD
0	0	0	0	Driving Low
0	0	1	0	Floating
0	1	0	0	Driving Low
0	1	1	0	Pull low
1	0	0	0	Driving Low
1	0	1	0	Pull high
1	1	0	0	Driving Low

PU	PD	DATA	XTAL_PAD_EN	PAD
1	1	1	0	Driving High
x	x	x	1	Floating

Table 5-54 The truth table of analog pad

PU	PD	DATA	PAD
0	0	0	Driving Low
0	0	1	Floating
0	1	0	Driving Low
0	1	1	Pull low
1	0	0	Driving Low
1	0	1	Pull high
1	1	0	Driving Low
1	1	1	Driving High

Table 5-55 The truth table of digital pad

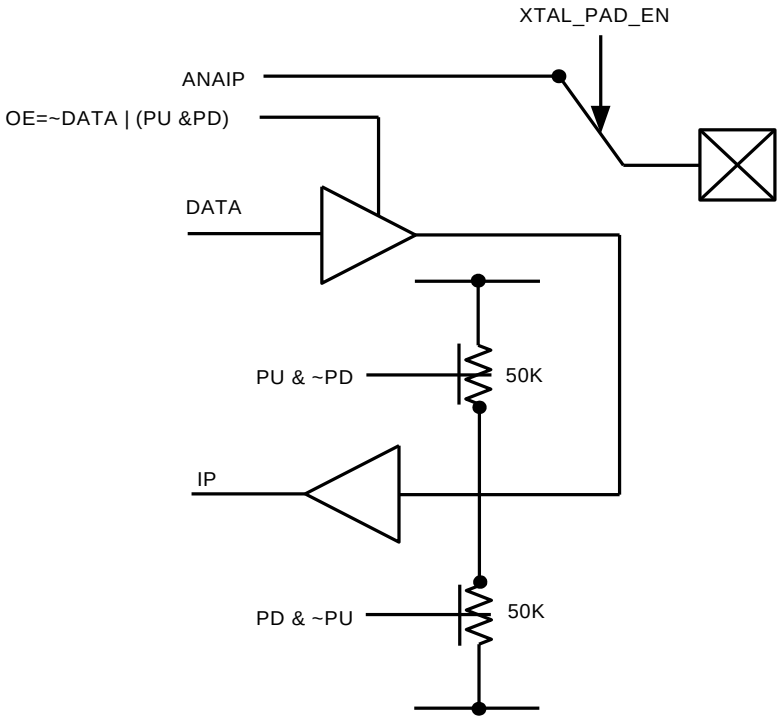


Figure 5-9 The block diagram of analog pad

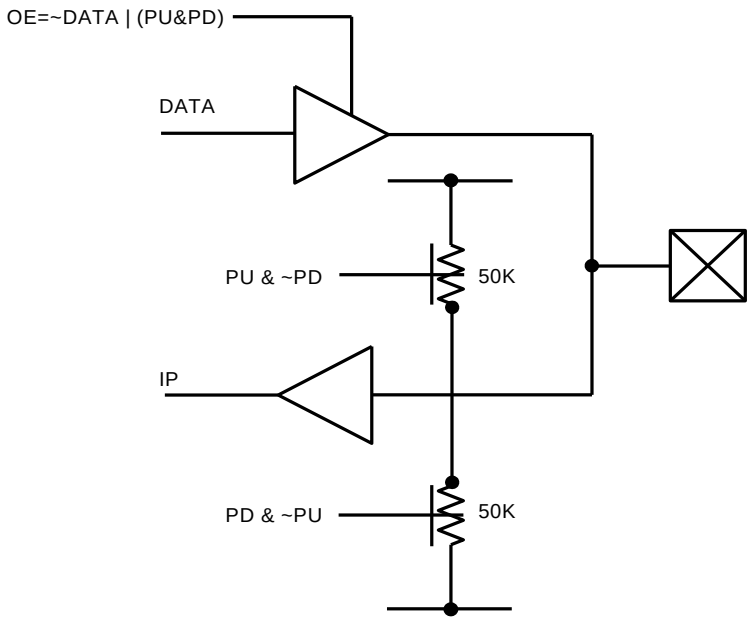


Figure 5-10 The block diagram of digital pad

GPM8F1129/1065/1033/1019A can use M-type and T-type keyboard application. In M-type application, each Port0 can be configured as keyboard pin individual by setting KBIEN register (0xA9). In stop mode, any change in these keyboard pins will cause system wakeup by setting KB_WKUEN bit of WKUEN register. Therefore, user should read Port0 to latch keyboard pin data before CPU enters stop mode. In T-type keyboard application, Port0 and Port3 can be selected as scan key independently by configuring P0_SC, and P3_SC respectively. If the port is configures as scan key, it work as input with pull-high resistor and output fixed frequency low pulse in stop mode. User should scan each TKEY IO status and store its responding TKEY_XOR register to P0_TKEY (0xE3) and P3_TKEY(0xE4) registers before the CPU enters stop mode. User can read the TKEY_XOR register to determine the result of the current scan operation. Figure 5-12 shows the block diagram of TKEY_XOR register. If the status of key scan operation is different from the content of P0_TKEY and P3_TKEY, system will wake up. If the pin is set as scan key, the external interrupt function (P30~P34) and keyboard pin function (P00~P07) are disabled. The number of keys support via T-keys feature is n (n – 1) / 2(n= total I/Os required). Figure 5-11 shows the T-type keyboard scan method.

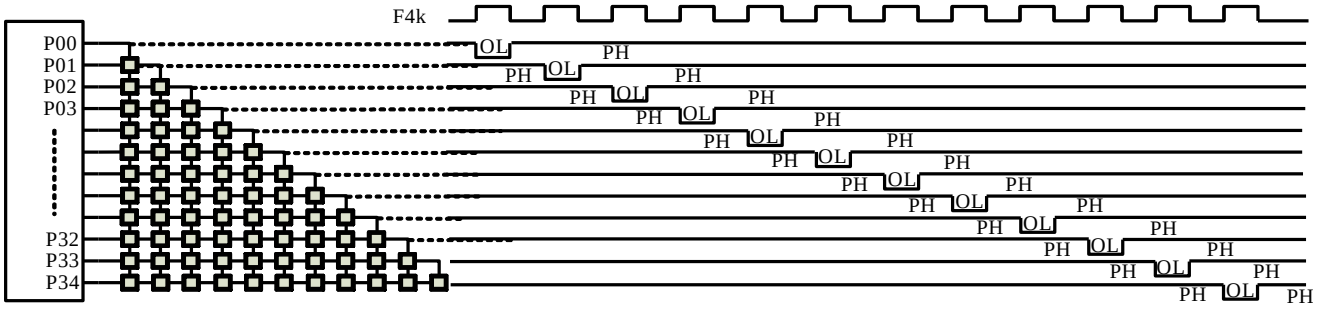


Figure 5-11 T-type keyboard scan method

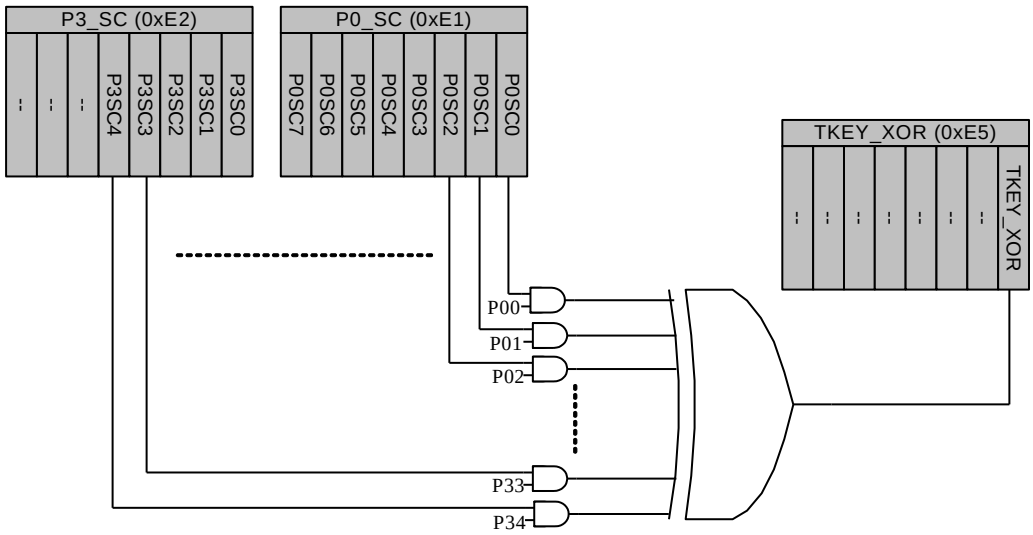


Figure 5-12 TKEY_XOR register

P0			Address: 0x80		Port0 Register			
Bit	7	6	5	4	3	2	1	0
Function	P07	P06	P05	P04	P03	P02	P01	P00
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:0	P0[7:0]	R/W	Port0	

Table 5-56 P0 register

P1			Address: 0x90		Port1 Register			
Bit	7	6	5	4	3	2	1	0
Function	P17	P16	P15	P14	P13	P12	--	--
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:2	P1[7:2]	R/W	Port1	
1:0	--	R/W	Reserved	

Table 5-57 P1 register

P2			Address: 0xA0		Port2 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	P23	P22	P21	P20
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	P2[3:0]	R/W	Port2	

Table 5-58 P2 register

P3			Address: 0xB0		Port3 Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P34	P33	P32	P31	P30
Default	1	1	1	1	1	1	1	1

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3[4:0]	R/W	Port3	

Table 5-59 P3 register

P0_PU			Address: 0xAA		Port0 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_PU	P06_PU	P05_PU	P04_PU	P03_PU	P02_PU	P01_PU	P00_PU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_PU[7:0]	R/W	Port0 pull up control bits 0: floating; 1: pull up	

Table 5-60 P0_PU register

P0_PD			Address: 0xAB		Port0 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P07_PD	P06_PD	P05_PD	P04_PD	P03_PD	P02_PD	P01_PD	P00_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_PD[7:0]	R/W	Port0 pull down control bits 0: floating 1: pull down	

Note: If P0_PU and P0_PD are set to '1' simultaneously, P0 will be output mode.

Table 5-61 P0_PD register

P1_PU			Address: 0xAC		Port1 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P17_PU	P16_PU	P15_PU	P14_PU	P13_PU	P12_PU	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:2	P1_PU[7:2]	R/W	Port1 pull up control bits 0: floating; 1: pull up	
1:0	--	R/W	Reserved	

Table 5-62 P1_PU register

P1_PD			Address: 0xAD		Port1 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	P17_PD	P16_PD	P15_PD	P14_PD	P13_PD	P12_PD	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:2	P1_PD [7:2]	R/W	Port1 pull down control bits 0: floating; 1: pull down	
1:0	--	R/W	Reserved	

Note: If P1_PU and P1_PD are setting to '1' simultaneously, P1 will be output mode.

Table 5-63 P1_PD register

P2_PU			Address: 0x9E		Port2 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	P23_PU	P22_PU	P21_PU	P20_PU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	P2_PU [3:0]	R/W	Port2 pull up control bits 0: floating; 1: pull up	

Table 5-64 P2_PU register

P2_PD			Address: 0x9F		Port2 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	P23_PD	P22_PD	P21_PD	P20_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3:0	P2_PD [3:0]	R/W	Port2 pull down control bits 0: floating; 1: pull down	

Note: If P2_PU and P2_PD are setting to '1' simultaneously, P2 will be output mode.

Table 5-65 P2_PD register

P3_PU			Address: 0xA2		Port3 pull up configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P34_PU	P33_PU	P32_PU	P31_PU	P30_PU
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_PU[4:0]	R/W	Port3 pull up control bits 0: floating; 1: pull up	

Table 5-66 P3_PU register

P3_PD			Address: 0xA3		Port3 pull down configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P34_PD	P33_PD	P32_PD	P31_PD	P30_PD
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_PU[4:0]	R/W	Port3 pull up control bits 0: floating 1: pull up	

Note: If P3_PU and P3_PD are setting to '1' simultaneously, P3 will be output mode.

Table 5-67 P3_PD register

SRCON			Address: 0xA5		Slew Rate Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	P3_SR	P2_SR	P1_SR	P0_SR
Default	0	0	0	0	1	1	1	1

Bit	Function	Type	Description	Condition
7:4	--	R/W	Reserved	
3	P3_SR	R/W	Port3 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
2	P2_SR	R/W	Port2 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
1	P1_SR	R/W	Port1 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	
0	P0_SR	R/W	Port0 slew rate control bit 0: slew rate control disable 1: slew rate control enable 30ns	

Table 5-68 SRCON register

P0_SC			Address: 0xE1		Port0 Key Scan Control Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_SC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_SC[7:0]	R/W	Port0 key scan control 0: Port0x no key scan function 1: Port0x with key scan function	

Table 5-69 P0_SC register

P3_SC			Address: 0xE2		Port3 Key Scan Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	P3_SC[4:0]				
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4:0	P3_SC[4:0]	R/W	Port3 key scan control 0: Port3x no key scan function 1: Port3x with key scan function	

Table 5-70 P3_SC register

P0_TKEY			Address: 0xE3		Port0 TKEY Compare Register			
Bit	7	6	5	4	3	2	1	0
Function	P0_TKEY[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P0_ TKEY [7:0]	R/W	Port0 TKEY compare register	

Table 5-71 P0_TKEY register

P3_TKEY			Address: 0xE4		Port3 TKEY Compare Register			
Bit	7	6	5	4	3	2	1	0
Function	P3_TKEY[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	P3_ TKEY [7:0]	R/W	Port3 TKEY compare register	

Table 5-72 P3_TKEY register

TKEY_XOR			Address: 0xE5		TKEY_XOR Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	--	TKEY_XOR
Default	0	0	0	0	0	0	0	

Bit	Function	Type	Description	Condition
7:1	--	R/W	Reserved	
0	TKEY_XOR	R/W	XOR operation result of TKEY IO	

Table 5-73 TKEY_XOR register

5.10. Timer Module

5.10.1. Introduction

GPM8F1129/1065/1033/1019A is equipped with three timers. They are Timer 0, Timer 1 and Timer 2 respectively. In addition, Timer 2 also features Compare/Capture/Reload function. All of these three timers are up-count timers and 16-bit timer/counter. Each timer's function is described in the following sections.

5.10.2. Timer 0/1

Timer 0 and Timer 1 are fully compatible with the standard 8051 timers. Each timer consists of two 8-bit registers TH0(0x8C), TL0(0x8A), TH1(0x8D), TL1(0x8B). Timers 0 and Timer 1 work in the same three modes except for mode 3 and the related control registers are TMOD(0x89), TCON(0x88) and CKCON(0x8E) registers. In the timer mode, timer registers are incremented every 1/2 SYSCLK periods depends on CKCON(0x8E) setting, when appropriate timer is enabled.

TH0			Address: 0x8C		Timer0 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH0[7:0]	R/W	Timer 0 Load value – high byte	

Table 5-74 TH0 register

TL0			Address: 0x8A		Timer0 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL0[7:0]	R/W	Timer 0 Load value – low byte	

Table 5-75 TL0 register

TH1			Address: 0x8D		Timer1 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH1[7:0]	R/W	Timer 1 Load value – high byte	

Table 5-76 TH1 register

TL1			Address: 0x8B		Timer1 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL1[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL1[7:0]	R/W	Timer 1 Load value – low byte	

Table 5-77 TL1 register

TMOD			Address: 0x89		Timer0/1 Control Mode Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	M11	M10	--	--	M01	M00
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	R/W	Reserved	
5:4	M1[1:0]	R/W	Mode select bits of timer 1, which is tabled as Table 5-79	
3:2	--	R/W	Reserved	
1:0	M0[1:0]	R/W	Mode select bits of timer 0, which is tabled as Table 5-79	

Table 5-78 TMOD register

M1	M0	Mode	Function description
0	0	0	TH0/1 operates as 8-bit timer with a divisor of 32 pre-scaler served by lower 5-bit of TL0/1.
0	1	1	16-bit timer. TH0/1 and TL0/1 are cascaded
1	0	2	TL0/1 operates as 8-bit timer with 8-bit auto-reload by TH0/1
1	1	3	TL0 is configured as 8-bit timer controlled by the standard Timer 0 bits. TH0 is an 8-bit timer controlled by the Timer 1 controls bits. Timer 1 holds its count.

Table 5-79 Four modes of Timer 0 and Timer 1

TCON			Address: 0x88		Timer0/1 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	TF1	TR1	TF0	TR0	IE1	--	IE0	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	TF1	R/W	Timer 1 interrupt (overflow) flag	
6	TR1	R/W	Timer 1 run control bit 0: disabled 1: enabled	
5	TF0	R/W	Timer 0 interrupt (overflow) flag	
4	TR0	R/W	Timer 0 run control bit 0: disabled 1: enabled	
3	IE1	R/W	INT1 interrupt flag	
2	--	R/W	Reserved	
1	IE0	R/W	INT0 interrupt flag	
0	--	R/W	Reserved	

Table 5-80 TCON register

CKCON			Address: 0x8E		Clock Control Register			
Bit	7	6	5	4	3	2	1	0
Function	WD1	WD0	WDFM	T1M	T0M	--	--	--
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:6	WD[1:0]	R/W	Watchdog timeout selection bits If WDFM=0:	

WD[1:0]	Timeout
00	32ms

Bit	Function	Type	Description	Condition
			01 128ms 10 512ms 11 2048ms If WDFM=1: (GPM8F1129/1065A only) WD[1:0] Timeout 00 2ms 01 8ms 10 16ms 11 32ms	
5	WDFM	R/W	Watchdog fast mode selection bit (GPM8F1129/1065A only) 0: watchdog fast mode is disabled 1: watchdog fast mode is enabled	
4	T1M	R/W	Division selection of the system clock that drives Timer 1 0: Timer 1 uses a system clock frequency 1: Timer 1 uses a divided-by-2 of the system clock frequency	
3	T0M	R/W	Division selection of the system clock that drives Timer 0 0: Timer 0 uses a system clock frequency 1: Timer 0 uses a divide-by-2 of the system clock frequency	
2:0	--	R/W	Reserved	

Table 5-81 CKCON register

5.10.2.1. Timer 0: Mode 0(13-Bit Timer)

In this mode, Timer 0 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 0 interrupt flag TF0 is set. The counted input is enabled to the Timer 0 when TR0(TCON[4]) = 1. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Figure 5-13 shows the block diagram of Timer 0 for Mode 0.

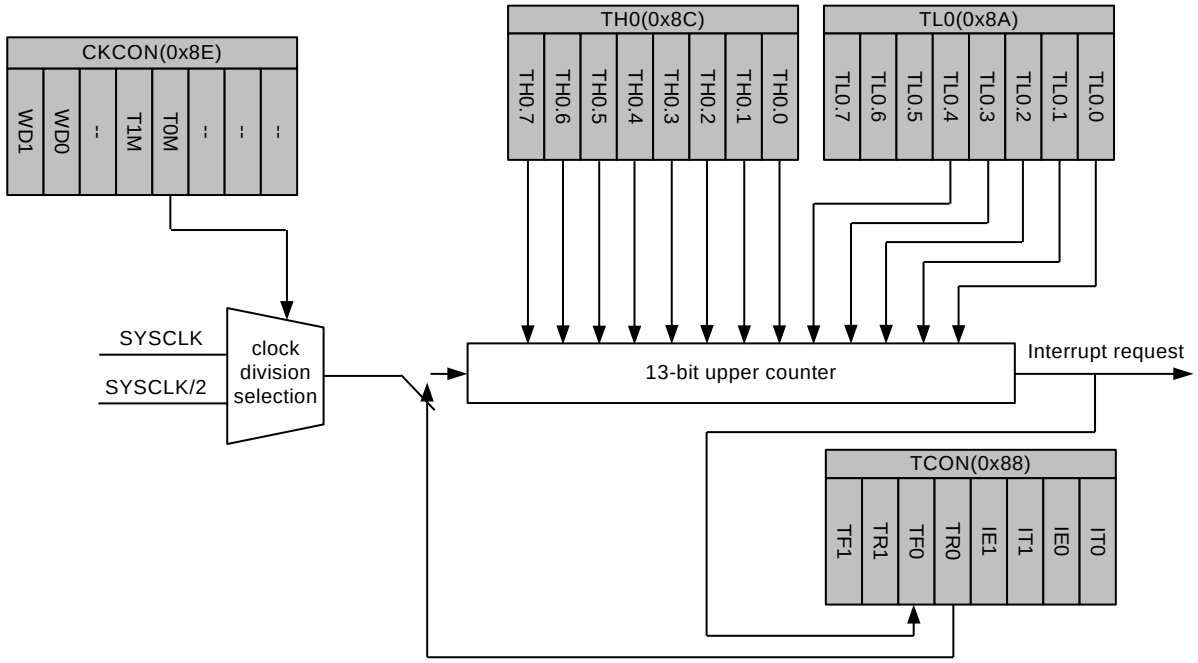


Figure 5-13 The block diagram of Timer 0 for Mode 0

5.10.2.2. Timer 0: Mode 1(16-bit Timer)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-14.

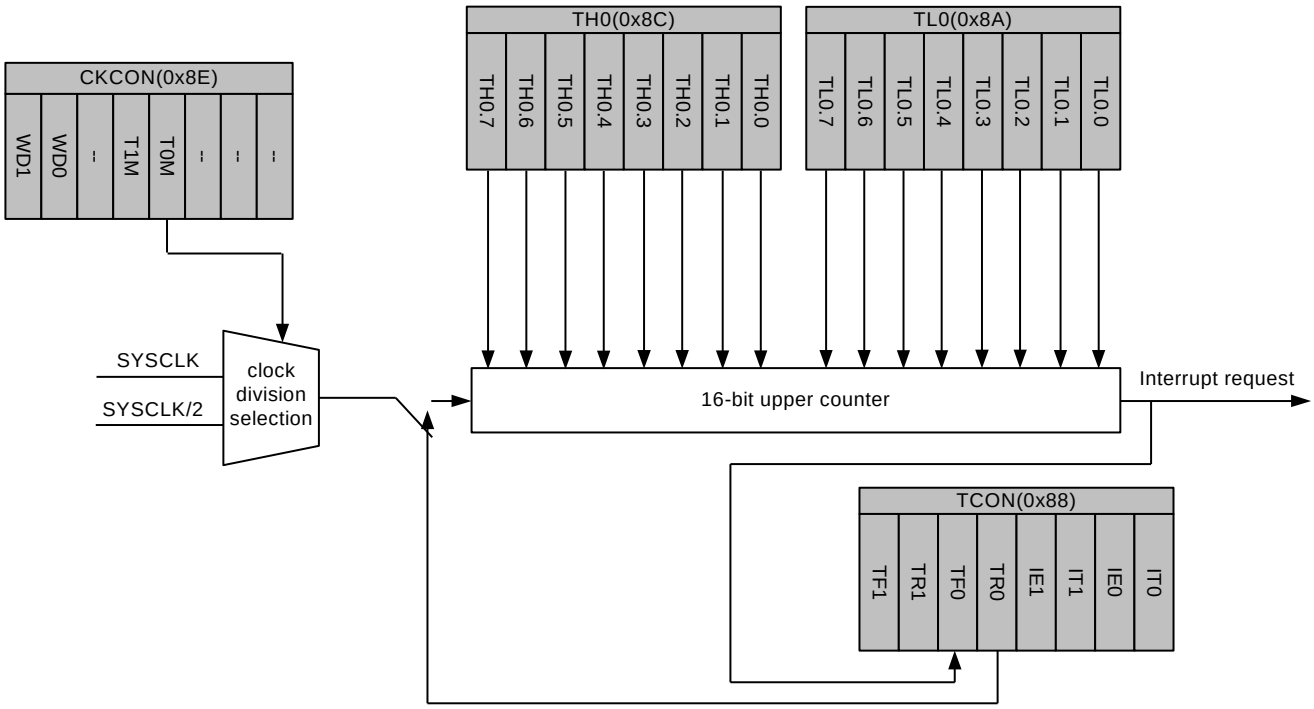


Figure 5-14 The block diagram of Timer 0 for Mode 1

5.10.2.3. Timer 0: Mode 2(8-Bit Timer with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reloads, as shown in Figure 5-15. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is loaded by software. The reload leaves TH0 unchanged.

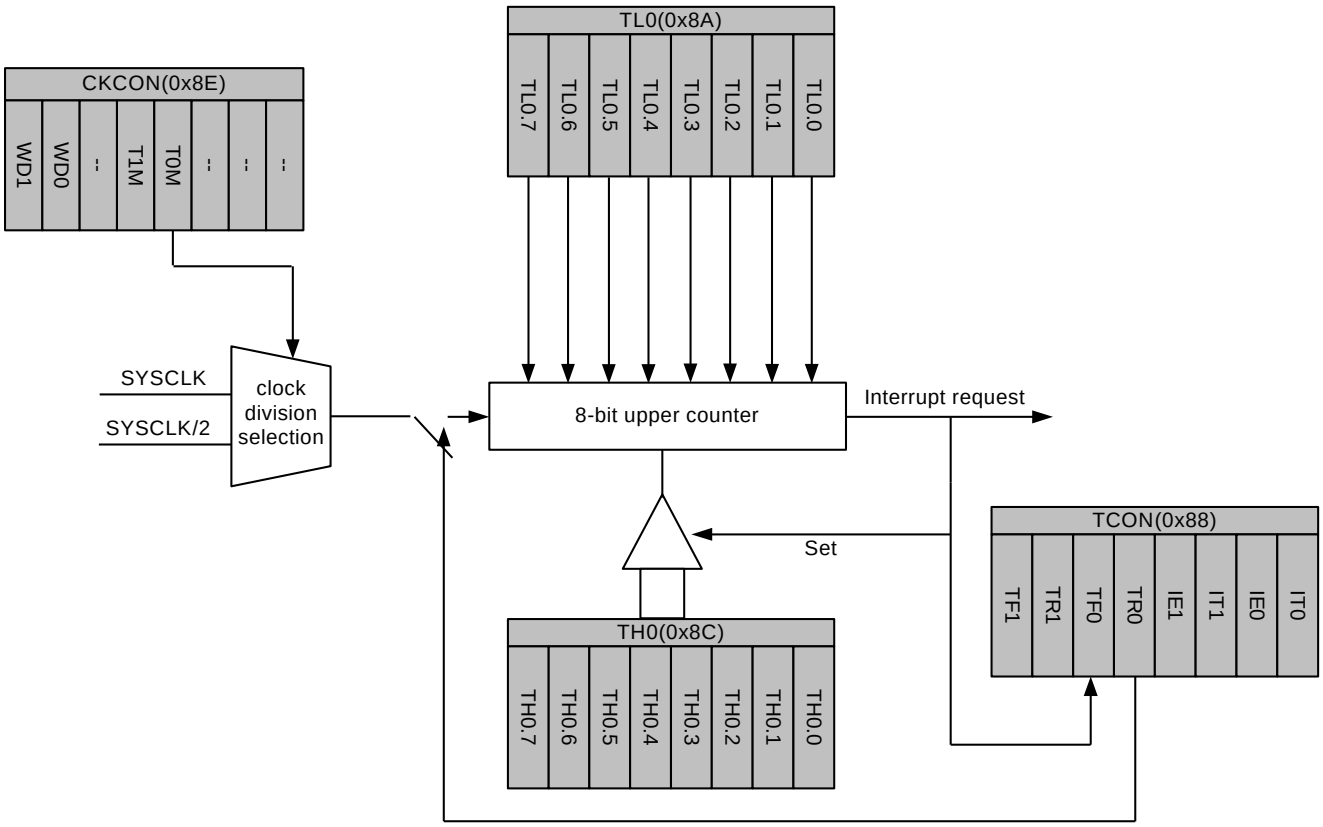


Figure 5-15 The block diagram of Timer 0 for Mode 2

5.10.2.4. Timer 0: Mode 3(Two 8-Bit Timers)

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The block diagram for Mode 3 on Timer 0 is shown in Figure 5-16. TL0 uses the Timer 0 control bits: CT0, TR0, and TF0. TH0 is locked into a timer function and uses the TR1 and TF1 flags from Timer 1 and controls Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer/counter. When Timer 0 is in Mode 3, Timer 1 can be turned off by switching it into its own Mode 3, or can still be used by the serial channel as a baud rate generator, or in any application where interrupt from Timer 1 is not required.

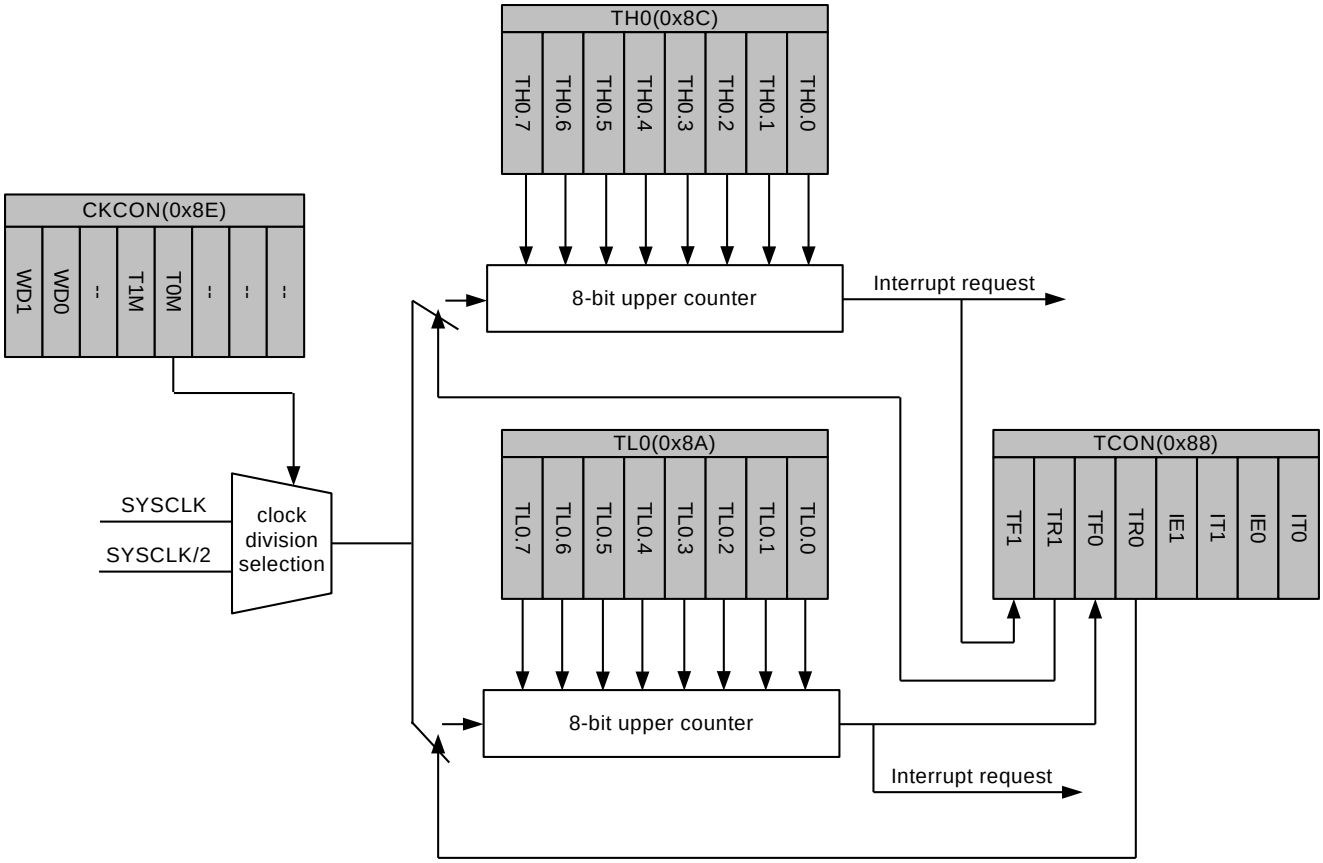


Figure 5-16 The block diagram of Timer 0 for Mode 3

5.10.2.5. Timer 1: Mode 0(13-Bit Timer)

In this mode, the Timer 1 register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, Timer 1 interrupt flag TF1 is set. The counted input is enabled to the Timer1 when TR1(TCON[6]) = 1. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Figure 5-17 shows the block diagram of Timer1 for Mode 0.

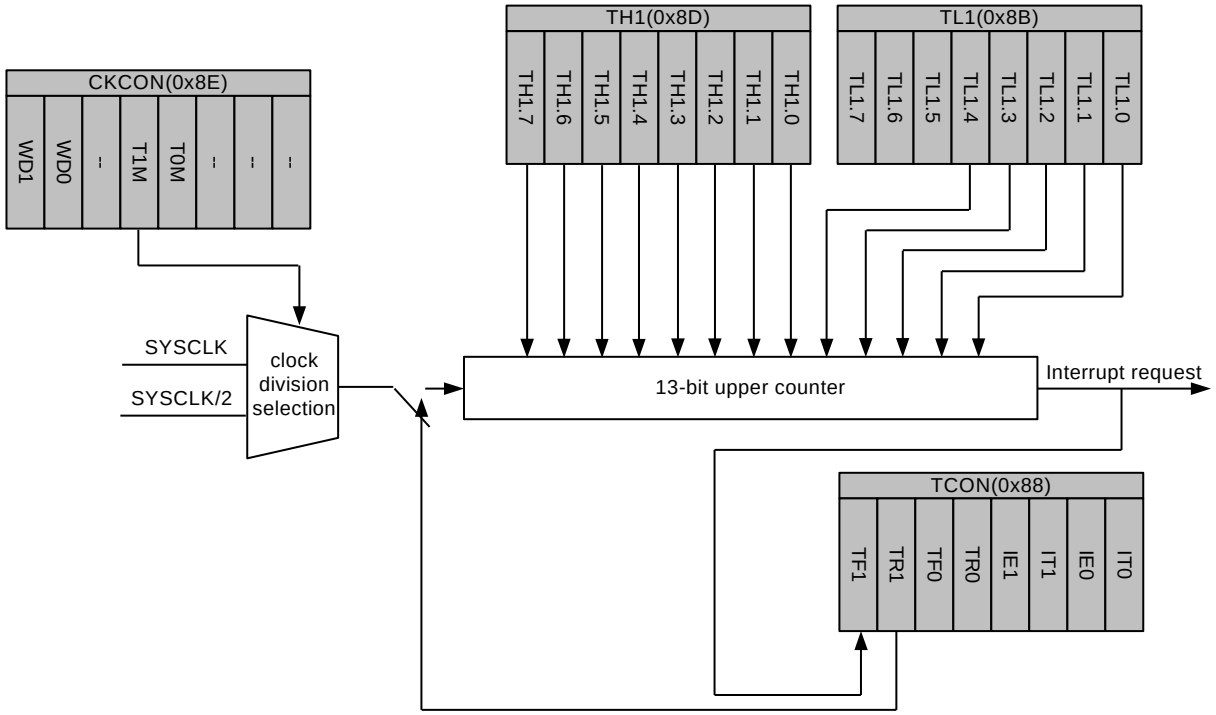


Figure 5-17 The block diagram of Timer 1 for Mode 0

5.10.2.6. Timer 1: Mode 1(16-Bit Timer)

Mode 1 is the same as Mode 0, except that the timer register is running with all 16 bits. The block diagram of Mode 1 is shown in Figure 5-18.

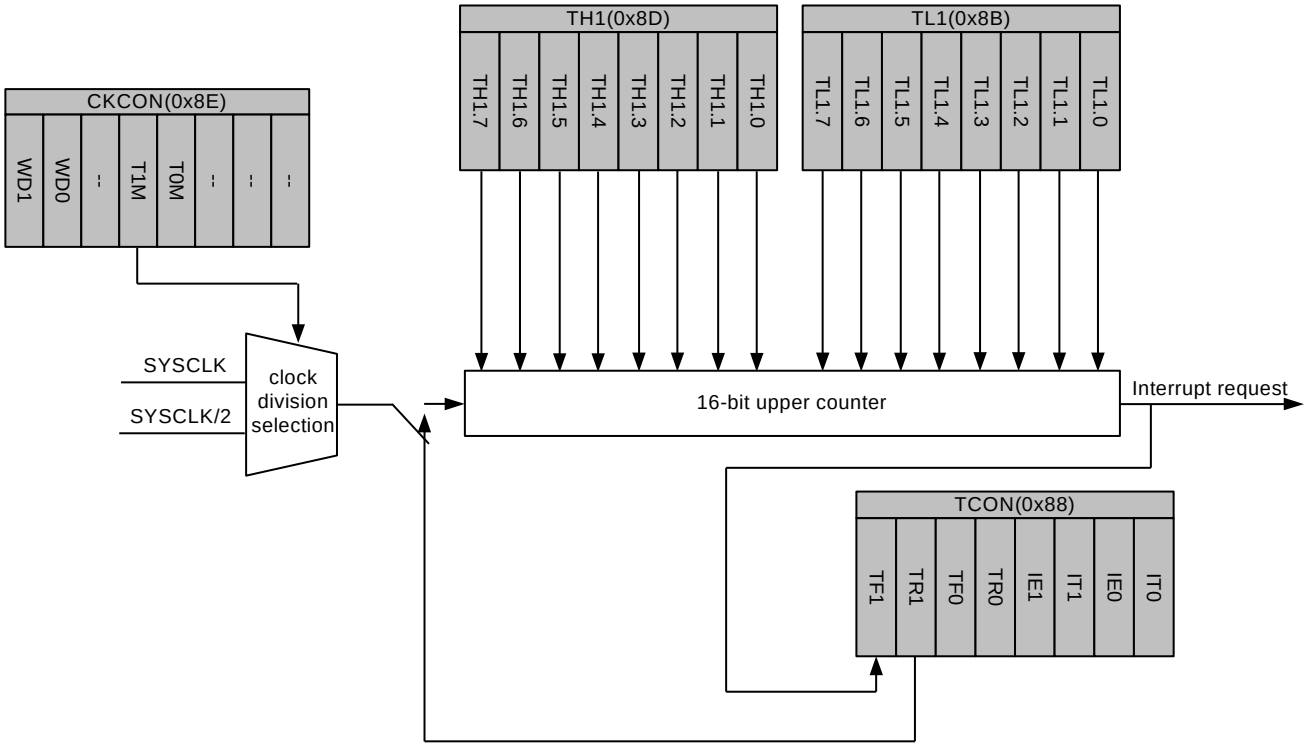


Figure 5-18 The block diagram of Timer 1 for Mode 1

5.10.2.7. Timer 1: Mode 2(8-Bit Timer with Auto-reload Function)

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reloads, as shown in Figure 5-19. Overflow from TL1 not only sets TF1, but it also reloads TL1 with the contents of TH1, which is loaded by software. The reload leaves TH1 unchanged.

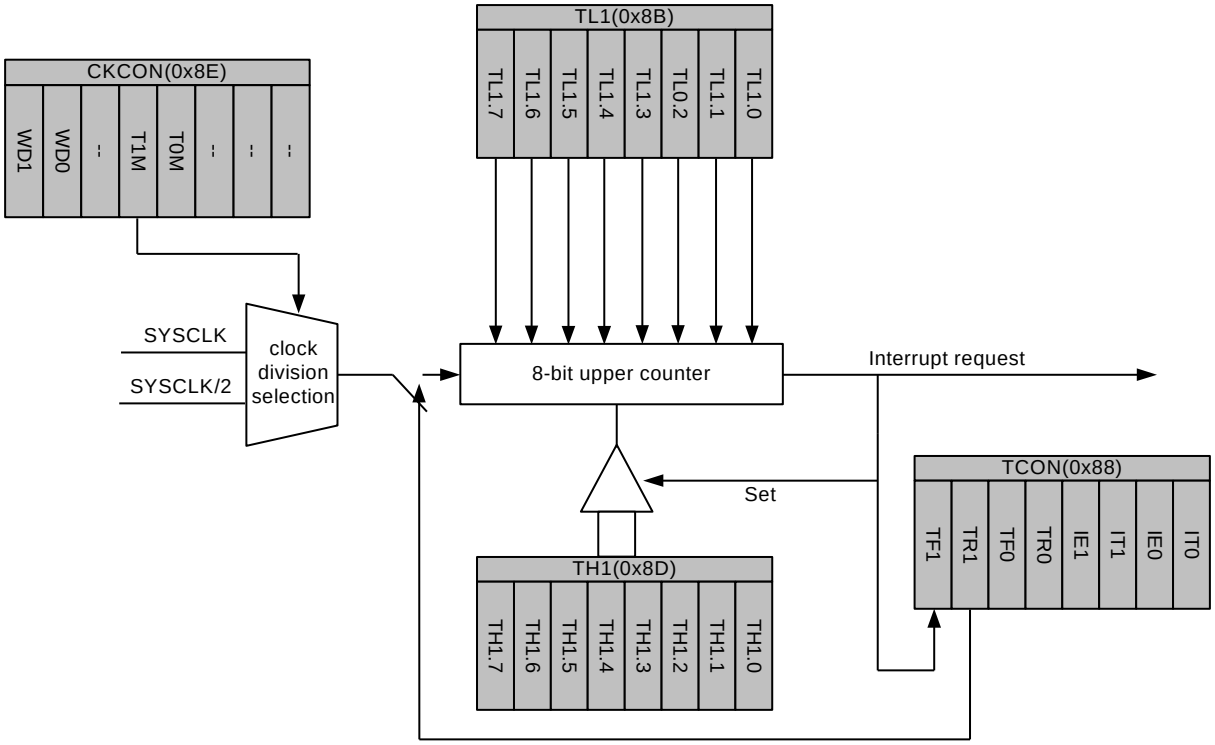


Figure 5-19 The block diagram of Timer 1 for Mode 2

5.10.2.8. Timer 1: Mode 3

Timer 1 in Mode 3 has no timer function. The effect is the same as setting TR1=0.

5.10.3. Timer 2

Timer 2 is a 16-bit-wide register which can operate as a timer. The additional Capture/Reload feature is one of the most powerful peripheral units of the core. It can be used for event capturing such as pulse generation, pulse width measuring etc. Figure 5-20 shows the block diagram of compare and capture function for Timer 2.

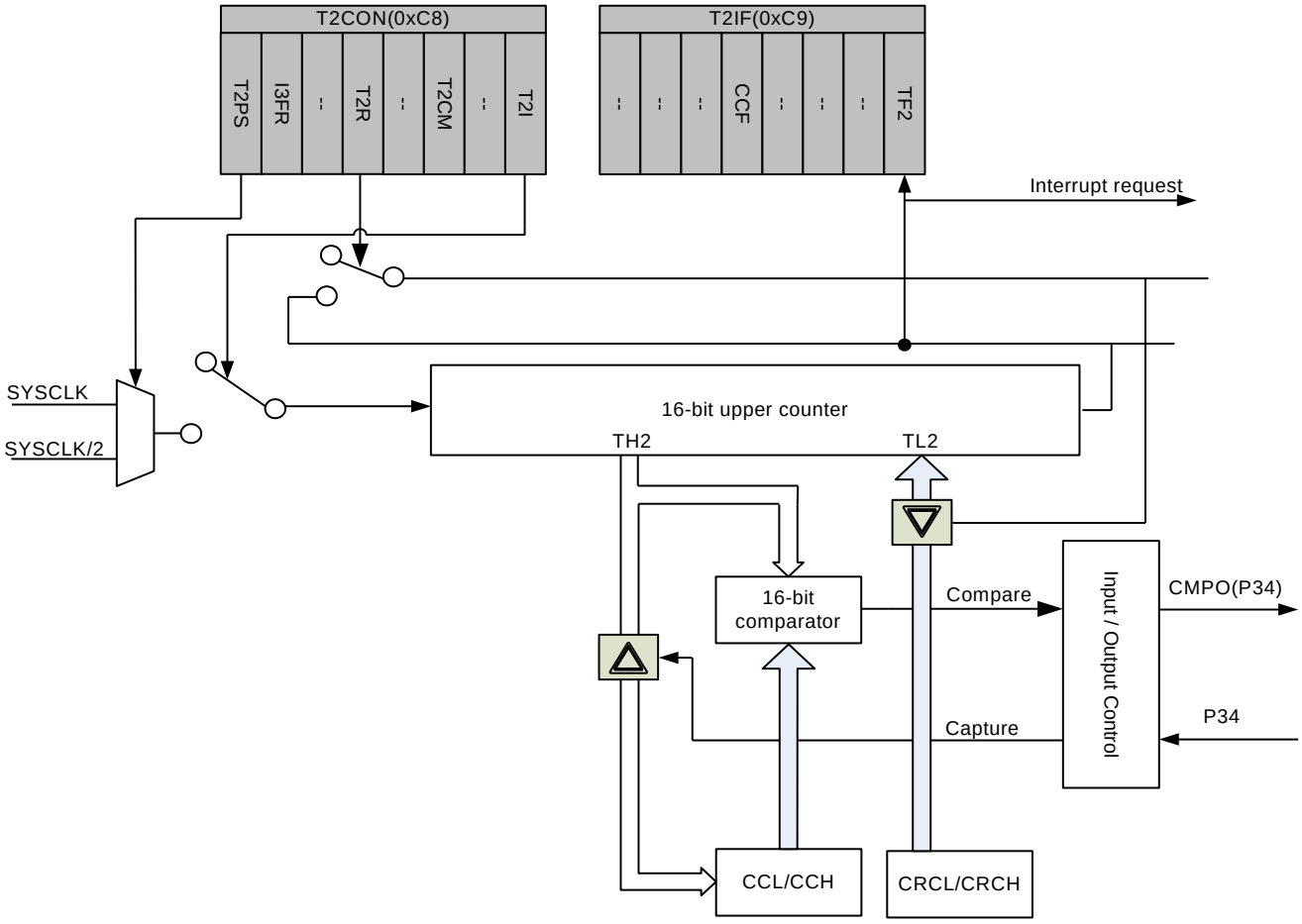


Figure 5-20 The block diagram of compare and capture function for Timer 2

5.10.3.1. Timer Mode

In timer function, the count rate is derived from the oscillator frequency. A pre-scalar offers the possibility of selecting a count rate of 1 or 1/2 of an oscillator frequency. Thus, the 16-bit timer register (consisted of TH2 and TL2) either increases in every 1 clock periods or in every 2 clock periods. The pre-scalar is selected by bit T2PS of T2CON.

5.10.3.2. Reload of Timer 2

The reload mode for timer 2 is selected by T2R bit of T2CON. When timer 2 rolls over from all 1's to all 0's, not only TF2 is set but also timer 2 registers is loaded with the 16-bit value from CRC register. Required CRC value can be set by software. Reloading occurs in the same clock cycle when TF2 is set. Thus, it will overwrite the count value 0x0000.

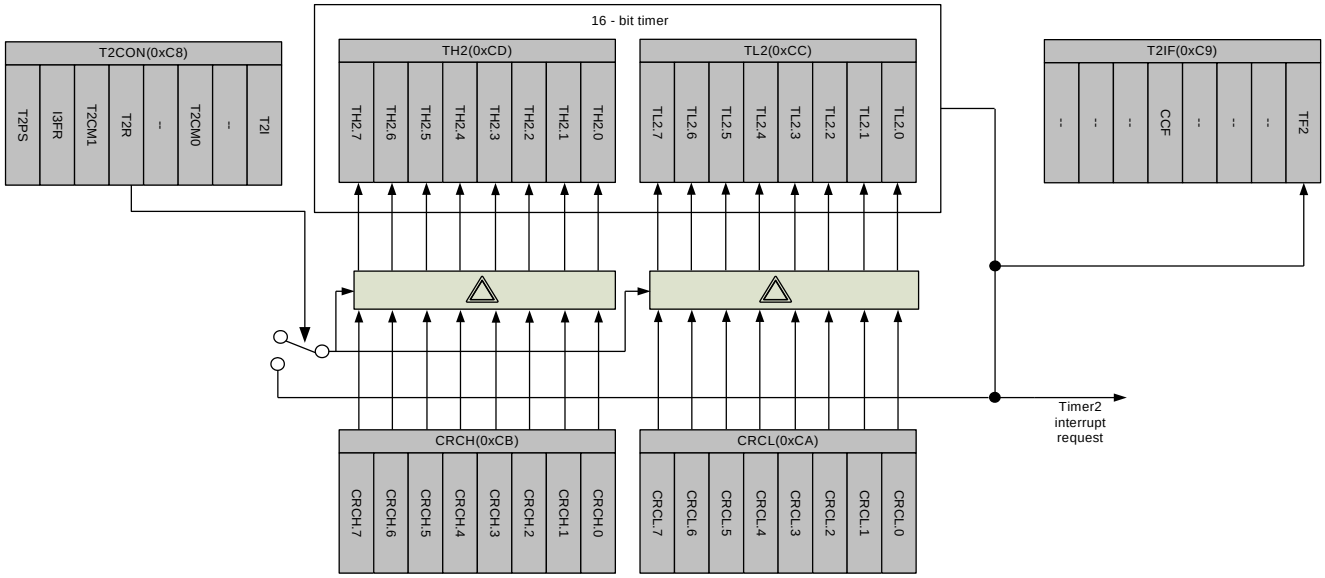


Figure 5-21 The block diagram of reload function for Timer 2

5.10.3.3. Compare Functions

The 16-bit value stored in a compare/capture register is compared with the contents of the timer register. If the count value in the timer register matches the stored value, an appropriate output signal is generated on a corresponding port pin, and an interrupt is requested. The contents of a compare register can be considered as time stamp at which a dedicated output reacts in a predefined way (either with a positive or negative transition). Variation of this time stamp somehow changes the wave of a rectangular output signal at a port pin. This may - as a variation of the duty cycle of a periodic signal - be used for pulse width modulation as well as for a continually controlled generation of any kind of square waveforms. Two compare modes are implemented to cover a wide range of possible applications. The compare mode is selected by bit T2CM in special function register T2CON. In all compare modes, the new value arrives at certain pin of P34 within the same clock cycle in which the internal compare signal is activated.

❑ Compare Mode 0

In compare mode 0, when the timer matches the contents of compare register, an output signal changes from low to high. It goes back to a low level when the timer overflows. In addition, CCP_INVEN bit of CMPO_INV register can also control the polarity of P34. Figure 5-22 shows a functional diagram of a port register in compare mode. The P34 register is directly controlled by the two signals: timer overflow and compare.

❑ Compare Mode 1

In compare mode 1, the software adaptively determines the transition of the output signal. It is commonly used when output signals are not related to a constant signal period. In compare mode 1, both transitions of a signal can be controlled. If mode 1 is enabled, and the software writes to an appropriate output register of P34, a new value will not appear at the output pin until the next compare match occurs. User can select this way whether the output signal should make a new transition or should keep its old value, until the Timer 2 counter matches the stored compare value. Figure 5-23 shows a functional diagram of Timer 2 in compare mode 1.

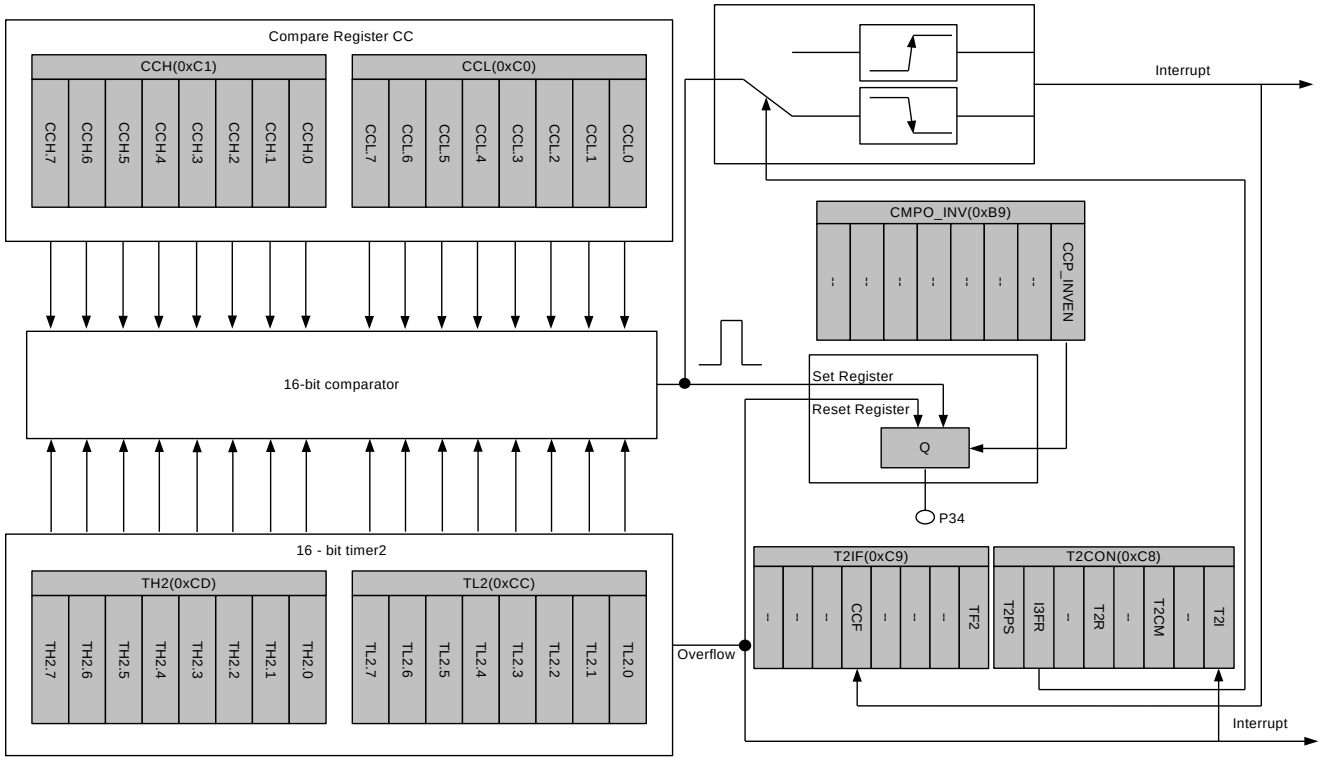


Figure 5-22 The block diagram of compare mode 0 for Timer 2

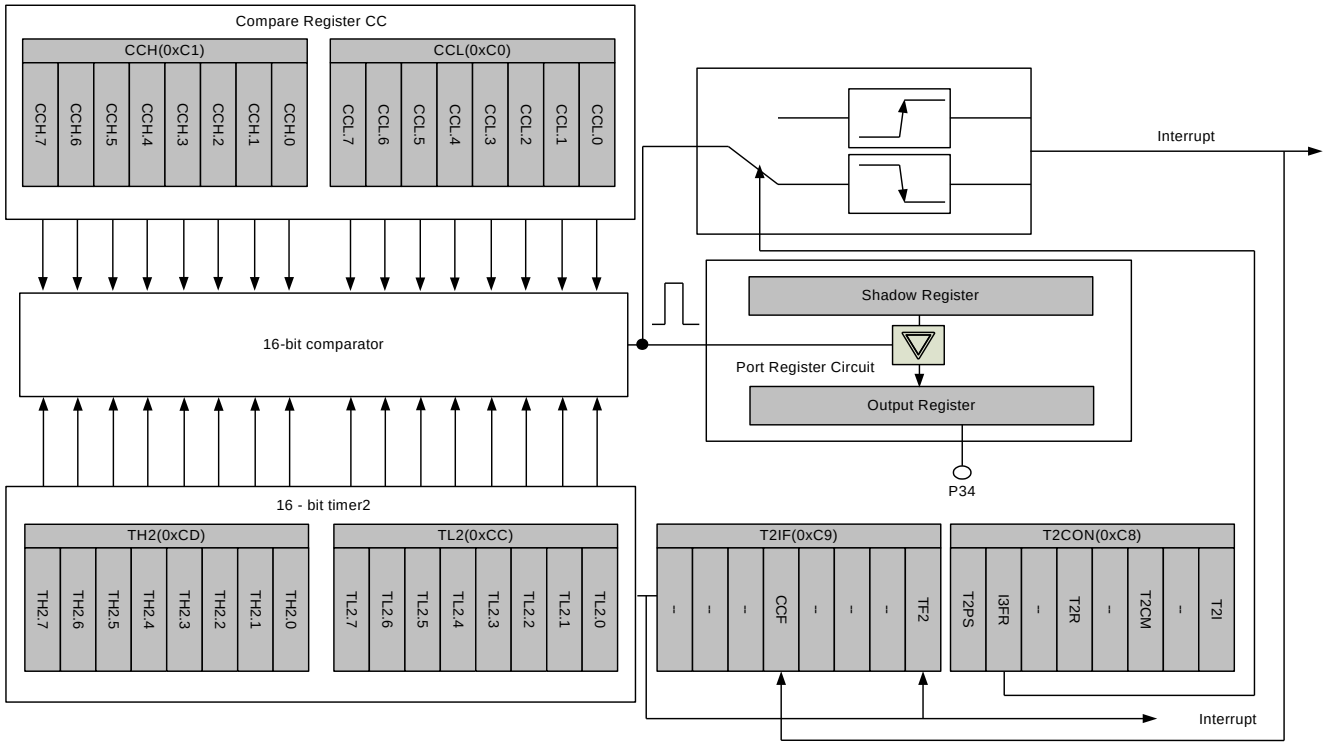


Figure 5-23 The block diagram of compare mode 1 for Timer 2

5.10.3.4. Capture Functions

The compare/capture register can be used to latch the current 16-bit value of the timer 2 registers TL2 and TH2. Two different modes are provided for this function.

❑ Capture Mode 0

In mode 0, an external event latches timer 2 contents to the compare/capture register. A positive or negative transition on the CAPTURE pin caused a capture, depending on the bit I3FR of T2CON. If I3FR flag is cleared, a capture occurs in response to a negative transition; otherwise, a capture occurs in response to a positive transition on CAPTURE pin.

❑ Capture mode 1

In mode 1, a capture will occur upon writing to the low order byte of the 16-bit capture register (CCL). This mode is provided to allow software reading of timer 2 contents on-the fly. The capture occurs in response to a write instruction to the low order byte of a capture register. The write-to-register signal (e.g. write-to-CCL) is used to initiate a capture. The value written to the dedicated capture register is irrelevant for this function. The contents of timer 2 will be latched into the capture register in the cycle following the write instruction. In this mode, no interrupt request will be generated. Figure 5-24 shows functional diagrams of the timer 2 capture function.

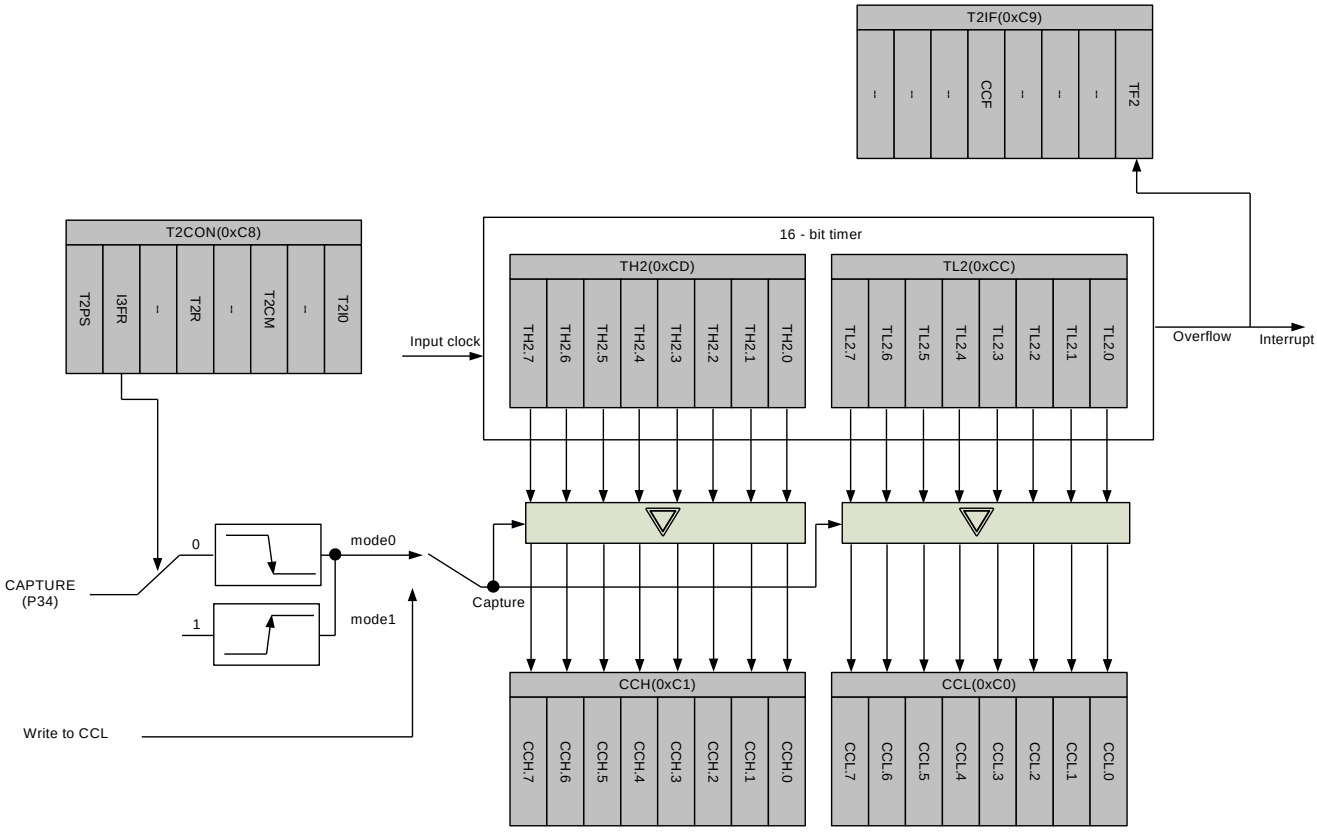


Figure 5-24 The block diagram of Timer 2 capture mode 0 for CCL and CCH

5.10.3.5. Timer 2 Related Registers

T2CON			Address: 0xC8		Timer2 Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	T2PS	I3FR	--	T2R	--	T2CM	--	T2I
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	T2PS	R/W	Pre-scaler selection bit 0: SYSCLK 1: SYSCLK/2	
6	I3FR	R/W	Interrupt edge activity selection bit of compare 0 function in combination with capture 0 function and register CRC Compare 0: 0: a negative transition on compare0 output can generate interrupt 1: a positive transition on compare0 output can generate interrupt Capture 0 : 0: capture to CC register occurs on a negative transition of CAPTURE pin 1: capture to CC register occurs on a positive transition of CAPTURE pin	
5	--	R/W	Reserved	
4	T2R	R/W	Timer 2 auto-reload mode enable bit	
3	--	R/W	Reserved	
2	T2CM	R/W	Compare mode selection bit for registers CC 0: compare mode 0 is selected 1: compare mode 1 is selected	
1	--	R/W	Reserved	
0	T2I	R/W	Timer 2 input selection bit 0: No input selected, timer 2 is stopped 1: Timer function input frequency SYSCLK (T2PS=0) SYSCLK/2 (T2PS=1)	

Table 5-82 T2CON register

CCEN			Address: 0xCE		Compare/Capture Enable Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	--	--	--	CMH	CML
Default	0	0	0	0	0	0	0	1

Bit	Function	Type	Description	Condition
7:2	--	R/W	Reserved	
1:0	CM	R/W	Compare/capture mode for CC register CMH / CML / Function 0 / 0 / Compare/capture disabled 0 / 1 / Capture on falling/rising edge of CAPTURE pin 1 / 0 / Compare enabled 1 / 1 / Capture on write operation into register CCL	

Table 5-83 CCEN register

T2IF			Address: 0xC9		Timer 2 Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	CCF	--	--	--	TF2
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	--	R/W	Reserved	
4	CCF	R/W	Compare and capture flag. Cleared by the software	
3:1	--	R/W	Reserved	
0	TF2	R/W	Timer 2 overflow flag. Cleared by the software	

Table 5-84 T2IF register

CCH			Address: 0xC1		Timer 2 CC Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC[15:8]	R/W	Timer2 compare/capture - high byte	

Table 5-85 The CCH register

CCL			Address: 0xC0		Timer 2 CC Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CC[7:0]	R/W	Timer2 compare/capture - low byte	

Table 5-86 The CCL register

CRCH			Address: 0xCB		CRC Register - high byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[15:8]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[15:8]	R/W	CRC - high byte	

Table 5-87 The CRCH register

CRCL			Address: 0xCA		CRC Register - low byte			
Bit	7	6	5	4	3	2	1	0
Function	CRC[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	CRC[7:0]	R/W	CRC - low byte	

Table 5-88 The CRCL register

TH2			Address: 0xCD		Timer 2 High Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TH2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TH2[7:0]	R/W	Timer 2 Load value – high byte	

Table 5-89 TH2 register

TL2			Address: 0xCC		Timer 2 Low Byte Register			
Bit	7	6	5	4	3	2	1	0
Function	TL2[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	TL2[7:0]	R/W	Timer 2 Load value – low byte	

Table 5-90 TL2 register

5.11. UART0

UART0 has the same functionality as a standard 8051 UART. The serial port is full duplex, meaning it can transmit and receive concurrently. It is reception with double-buffer, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Figure 5-25 shows the block diagram of UART module. The serial port can operate in 4 modes: one synchronous and three asynchronous modes. Mode 2 and 3 has a special feature for multiprocessor communications. This feature is enabled by setting SM02 bit in SCON0 register. The master processor first sends out an address byte, which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM02 = 1, no slave will be interrupted by a data byte. An address byte will interrupt all slaves. The addressed slave will clear its SM02 bit and prepare to receive the data bytes that will be coming. The slaves that were not being addressed leave their SM02 set and ignoring the incoming data.

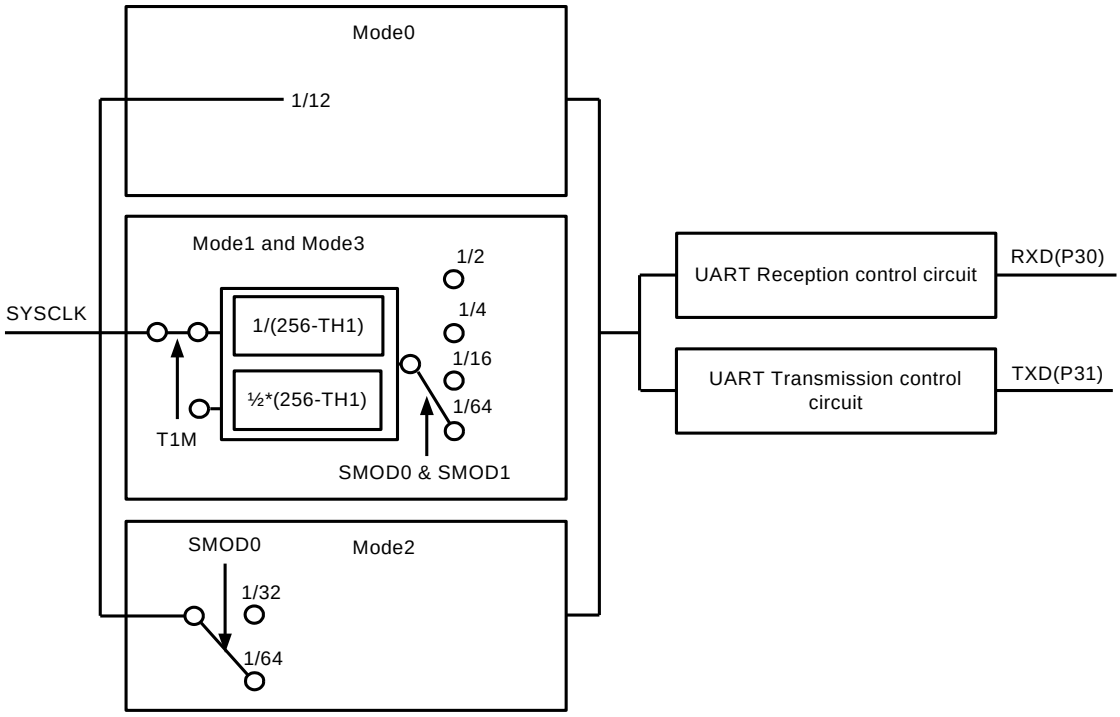


Figure 5-25 The block diagram of UART module

5.11.1. UART0: Mode 0(Synchronous Shift register)

This mode is used as shift register IO control, and not for real communication application. The baud rate is fixed at 1/12 of the system clock frequency and TXD0(P31) output is a shift clock. Eight bits are transmitted with LSB first. Reception is initialized by setting the flags in SCON0 as follows: RI0 =0 and REN0 =1. Figure 5-26 shows the timing diagram of UART0 transmission mode 0.

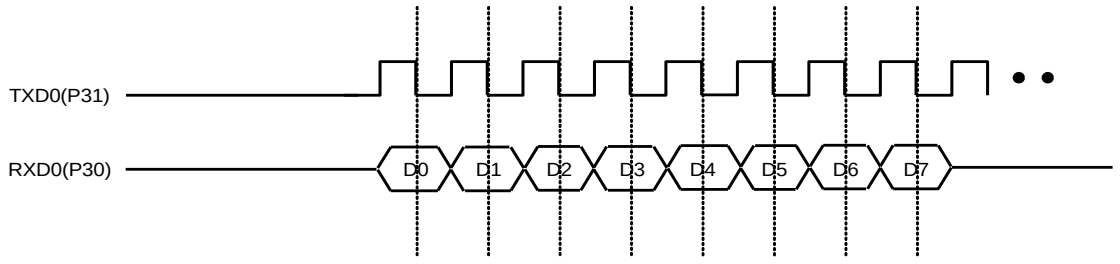


Figure 5-26 The timing diagram of UART0 transmission mode 0

5.11.2. UART0: Mode 1(8-Bit UART, Variable Baud Rate, Timer1 Clock Source)

In mode 1, TXD0 serves as serial output. 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receiving, a start bit synchronizes the reception, 8 data bits are available by reading SBUF0 and stop bit sets the flag RB08 in the SFR SCON0. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-27 shows the format of UART0 transmission mode 1.

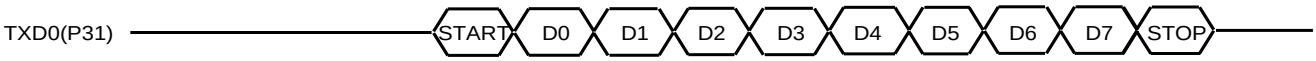


Figure 5-27 The format of UART0 transmission mode 1

5.11.3. UART0: Mode 2(9-Bit UART, Fixed Baud Rate)

This mode is similar to Mode 1 with two differences. The baud rate is fixed at 1/32 or 1/64 of system clock frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the UART0 interface: at transmission, bit TB08 in SCON0 is output as the 9th bit, and at receive, the 9th bit affects RB08 in SCON0. Figure 5-28 shows the format of UART0 transmission mode 2.

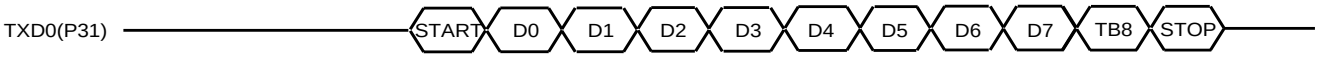


Figure 5-28 The format of UART0 transmission mode 2

5.11.4. UART0: Mode 3(9-Bit UART, Variable Baud Rate, Timer1 Clock Source)

The only difference between Mode 2 and Mode 3 is that the baud rate is a variable in Mode 3. When REN0 =1 data receiving is enabled. The baud rate is variable and depends from Timer 1 mode. The SMOD0 and SMOD1 bits of PCON (0x87) are used to set the baud rate as $T1_{ov}/2$ or $T1_{ov}/4$ or $T1_{ov}/16$ or $T1_{ov}/64$. Figure 5-29 shows the format of UART0 transmission mode 1.

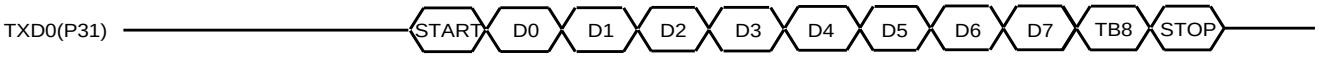


Figure 5-29 The format of UART0 transmission mode 3

5.11.5. UART0 Related Registers

The UART0 related registers are: SBUF0(0x99), SCON0(0x98), PCON(0x87), IE(0xA8) and IP(0xB8). The UART0 data buffer (SBUF0) consists of two separate registers: transmit and receive registers. A data writes into the SBUF0 sets this data in UART0 output register and starts a transmission. A data reads from SBUF0, reads data from the UART0 receive register.

SBUF0			**Address: 0x99**		**UART0 Buffer Register**			
Bit	7	6	5	4	3	2	1	0
Function	SBUF0[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
2:0	SBUF0[7:0]	R/W	UART 0 buffer	

Table 5-91 SBUF0 register

SCON0			**Address: 0x98**		**UART0 Configuration Register**			
Bit	7	6	5	4	3	2	1	0
Function	SM00	SM01	SM02	REN0	TB08	RB08	TI0	RI0
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	SM0[1:0]	R/W	Mode and baud rate setting which described as below table	
5	SM02	R/W	Enables a multiprocessor communication feature	
4	REN0	R/W	Enable serial reception.	
3	TB08	R/W	The 9th transmitted data bit in Modes 2 and Mode 3	
2	RB08	R/W	In Mode 0 this bit is not used In Mode 1, if SM02 is 0, RB08 is the stop bit. In Mode 2 and Mode 3, it is the 9th data bit received	
1	TI0	R/W	UART0 transmitter interrupt flag	
0	RI0	R/W	UART0 receiver interrupt flag	

Table 5-92 SCON0 register

SM00	SM01	Mode	Function	Baud rate
0	0	0	Shift register	SYSCLK/12
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	SYSCLK/32(SMOD0=0) SYSCLK/64(SMOD0=1)
1	1	3	9-bit UART	variable

❑ variable: in Mode1 and Mode 3(T1M=0)

SMOD1	SMOD0	Baud rate
0	0	T1ov/64(T1ov=SYSCLK/(256-TH1))
0	1	T1ov/16(T1ov=SYSCLK/(256-TH1))
1	0	T1ov/4(T1ov=SYSCLK/(256-TH1))
1	1	T1ov/2(T1ov=SYSCLK/(256-TH1))

Note: if SMOD1=SMOD0=1, TH1 should be over than 0x10.

❑ Baud rate setting example (SYSCLK = 16MHz, T1M=0)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/16	0x30(48)	4807.69	0.16%
9600	T1ov/16	0x98(152)	9615.38	0.16%
19200	T1ov/16	0xCC(204)	19230.77	0.16%
38400	T1ov/16	0xE6(230)	38461.54	0.16%
57600	T1ov/2	0x75(117)	57553.96	-0.08%
115200	T1ov/2	0xBB(187)	115942.03	0.64%

❑ Baud rate setting example (SYSCLK = 8MHz)

Bit rate	Baud rate	Timer reload setting (TH1)	Actual rate	Error deviation (%)
4800	T1ov/16	0x98(152)	4807.69	0.16%
9600	T1ov/16	0xCC(204)	9615.38	0.16%
19200	T1ov/16	0xE6(230)	19230.77	0.16%
38400	T1ov/16	0xF3(243)	38461.54	0.16%
57600	T1ov/2	0xBB(187)	57971.01	0.64%
115200	T1ov/2	0xDD(221)	114285.71	-0.79%

PCON			Address: 0x87		Power Configuration Register			
Bit	7	6	5	4	3	2	1	0
Function	SMOD0	SMOD1	CPU_IDLE	PWE	STOP_RST_EN	--	STOP	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	SMOD0	R/W	UART0 baud rate bit when clocked by Timer1	
6	SMOD1	R/W	UART0 baud rate bit when clocked by Timer1	
5	CPU_IDLE	R/W	IDLE mode enable bit 0: IDLE mode disabled ; 1: IDLE mode entered	
4	PWE	R/W	Program Write Enable (PWE) 0: Disable Flash write activity during MOVX instruction 1: Enable Flash write activity during MOVX instruction	
3	STOP_RST_EN	R/W	Wakeup state selection bit 0: Next instruction state after wakeup 1: Reset state afer wakeup	
2	--	R/W	Reserved	
1	STOP	R/W	STOP mode enable bit 0: Disabled 1: Enabled	
0	--	R/W	Reserved	

Table 5-93 PCON register

5.12. SPI

A Serial Peripheral Interface (SPI) controller is built in GPM8F1129/1065/1033/1019A to facilitate communicating with other devices and components. The SPI controller includes four master modes. There are four control signals on SPI including SPCSB, SPSCK, MOSI and MISO, these four pins cannot be GPIOs, while SPI module is enabled by corresponding control bit. In other words, any setting on corresponding GPIO control register will have no effect. The SPI provides following features.

- ❑ Programmable phase and polarity of master clock
- ❑ Programmable master SPSCK clock frequency

In master mode, the shifting clock (SPSCK) is generated by SPI block. There are two control bits to control the clock phase and polarity. The transmission starts immediately after SPI_START is set(SPICON[0]=1,0xFC). The SPI shifts the 8-bit data from MSB to LSB through the MOSI pin during 8 SCK cycles. Programmer can read SPI data from MISO control register by setting SPI_RD =1. The following four diagrams depict the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”). The related registers are SYSCON1 register, SPICON register, SPITXD register and SPIRXD registers which are tabled as Table 5-96 to Table 5-97.

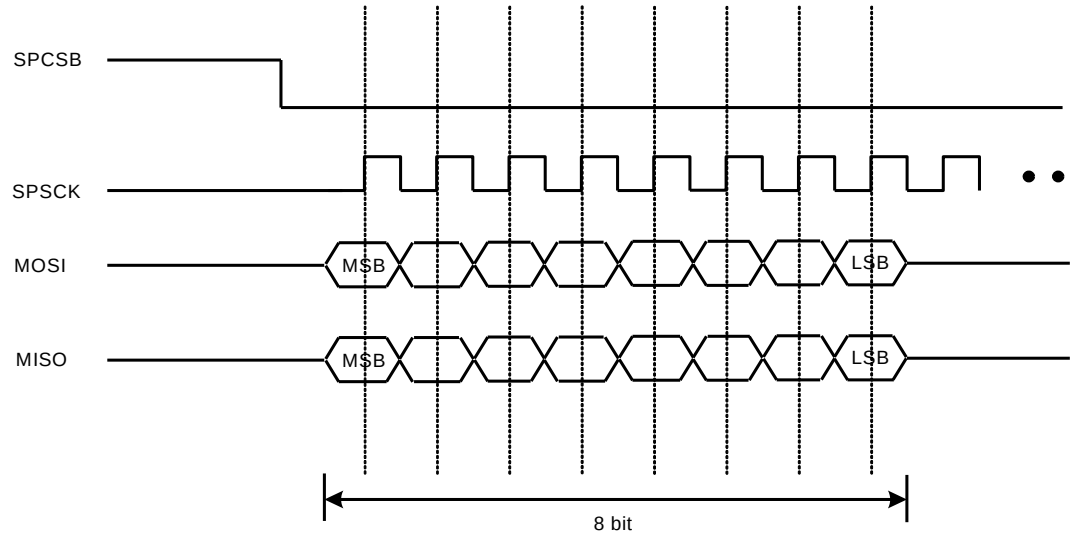


Figure 5-30 Master Mode, POLARITY=0, PHASE=0

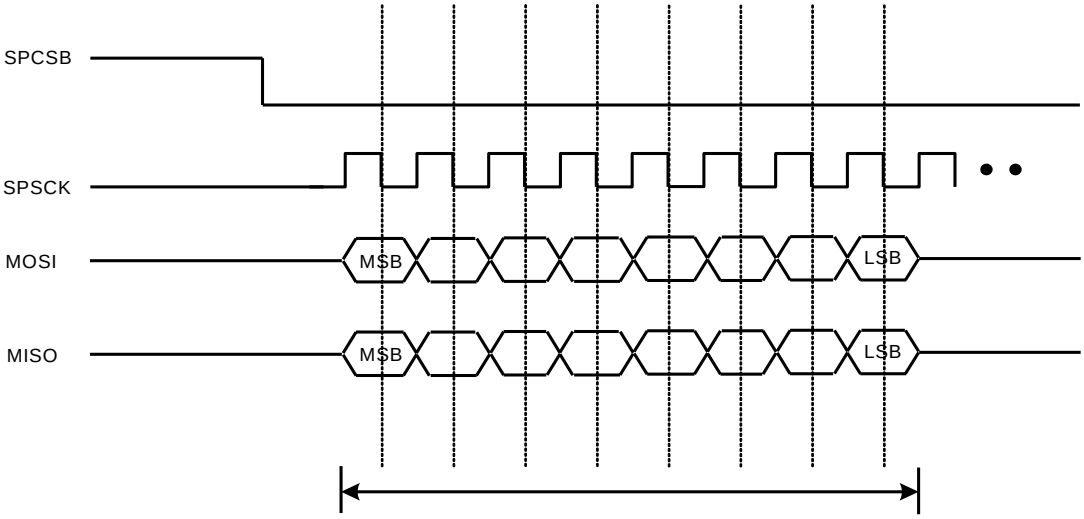


Figure 5-31 Master Mode, POLARITY=0, PHASE=1

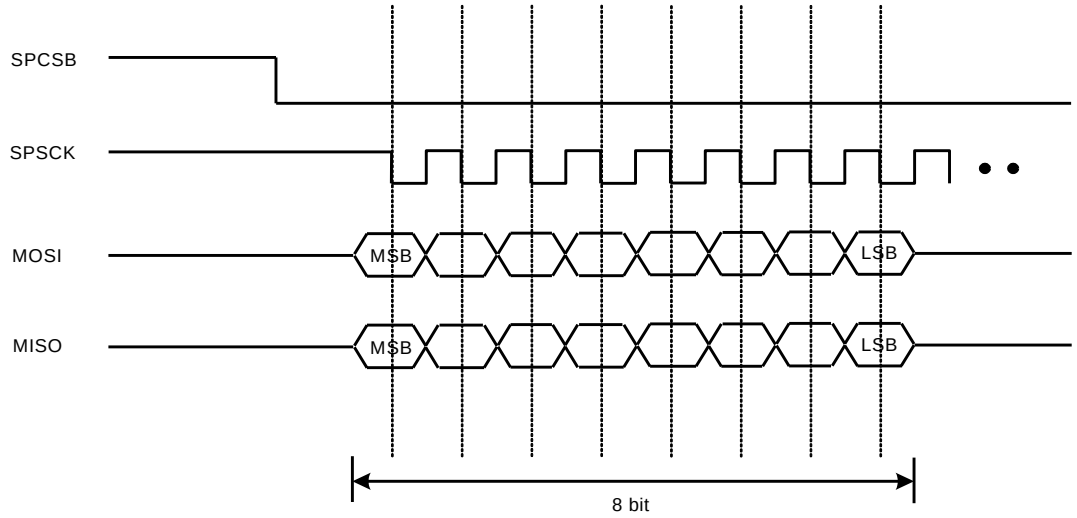


Figure 5-32 Master Mode, POLARITY=1, PHASE=0

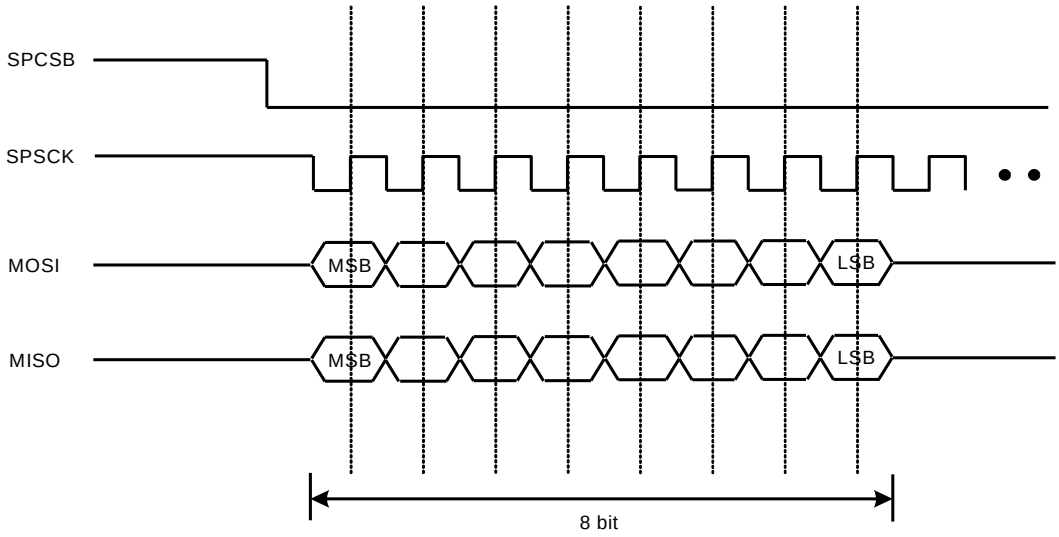


Figure 5-33 Master Mode, POLARITY=1, PHASE=1

SYSCON1			Address: 0xAF		System Control Register 1			
Bit	7	6	5	4	3	2	1	0
Function	--	--	ADorDA	SPI_EN	I2CEN	I2C_AUTO_RW	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	--	Reserved	
5	ADorDA	R	I2C Address or Data indication bit for slave mode 0: Address 1: Data	
4	SPI_EN	R/W	SPI signals forward to P1[7:4] enable P1[4]: SPI_TX P1[5]: SPI_CLK P1[6]: SPI_RX P1[7]: SPI_CSB	
3	I2CEN	R/W	Change P2[3:2] to I2C usage. 0: P2[3:2] is used as GPIO. 1: P2[3:2] is used as I2C interface.	
2	I2C_AUTO_RW	R/W	I2C auto read write mode enable bit (for slave mode) 0: Disable 1: Enable	
1	IRTX_SW	R/W	IRTX pin selection bit 0: IRTX pin in on P21 1: IRTX pin in on P34	
0	--	--	Reserved	

Table 5-94 SYSCON1 register

SPICON			Address: 0xFC		SPI Control Register			
Bit	7	6	5	4	3	2	1	0
Function	POLARITY	PHASE	SPI_CLK_SEL[1:0]		CSB_KEEP	--	SPI_RD	SPI_START
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	POLARITY	R/W	SPI CLK initial state 0: low state; 1: high state	
6	PHASE	R/W	SPI CLK type control 0: 1st edge sample; 1: 2nd edge sample	
5:4	SPI_CLK_SEL[1:0]	R/W	SPI Clock output selection: 00: SYSCLK/2 01: SYSCLK/4 10: SYSCLK/8 11: SYSCLK/16	
3	CSB_KEEP	R/W	SPCSB keep low state control bit 0: SPCSB keeps low state only in communication 1: SPCSB always keeps low state	
2	--	--	Reserved	
1	SPI_RD	R/W	SPI read command	
0	SPI_START	R/W	Read: busy flag 0 = SPI is not busy 1 = SPI is busy Write: SPI start bit 1: SPI starts to transmit or receive	

Table 5-95 SPICON register

SPITXD			Address: 0xFD		SPI Output Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	SPITXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPITXD	R/W	SPI output buffer	

Table 5-96 SPITXD register

SPIRXD			Address: 0xFE		SPI Input Buffer Register			
Bit	7	6	5	4	3	2	1	0
Function	SPIRXD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	SPIRXD	R/W	SPI input buffer	

Table 5-97 SPIRXD register

5.13. I2C

An I2C Interface (I2C) is equipped in GPM8F1129/1065/1033/1019A. Only two wires (SCK and SDA) are needed to implement the protocol. The multi-master I2C-bus controller provides a mechanism to communicate between bus masters and peripheral devices by using two signals, a serial data line (SDA) and a serial clock line (SCK). To avoid all possibilities of confusion, data loss and blockage of information, the master and slave devices must have a defined protocol. In multi-master I2C-bus mode, multiple microprocessors can receive or transmit serial data to or from slave devices. The master that initiates a data transfer over the I2C-bus is responsible for terminating the transfer. It is possible to combine several masters, in addition to several slaves onto an I2C-bus to form a multi-master system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16 K.

5.13.1. I2C Bus Protocol

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A “Start” condition is a high-to-low transition of SDA line while SCK is high. A “Stop” condition is a Low-to-High transition of the SDA line while SCK is high. Start and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the I2C-bus will be free, again. Figure 5-34 shows Start and Stop conditions.

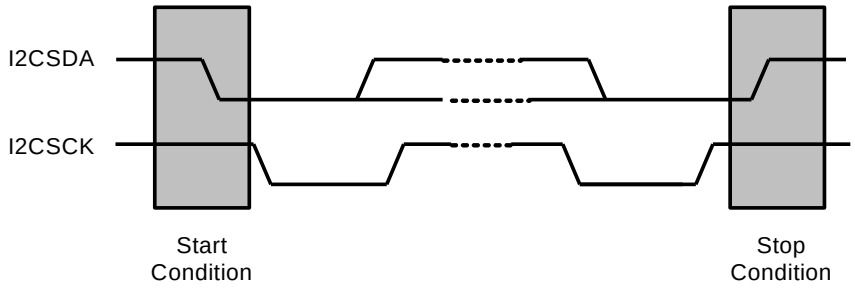


Figure 5-34 Start and Stop conditions

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is 0, it indicates a write operation(transmit operation); if bit 8 is 1, it indicates a request for data read(receive operation). Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the I2C-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first. To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit. Figure 5-35 and Figure 5-36 shows the format of I2C data transmission.

In the master mode, after the data is transferred, the I2C-bus interface will wait until pending interrupt is cleared. Until the interrupt is cleared, the SCL line will be held low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should write a new data into I2CDAT register before clear the pending interrupt. In the receive mode, after a data is received, the I2C-bus interface will wait until pending interrupt is cleared. Until the pending interrupt is cleared, the SCL line will be held low. After the pending interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should read the data from I2CDAT register before clear the pending interrupt.

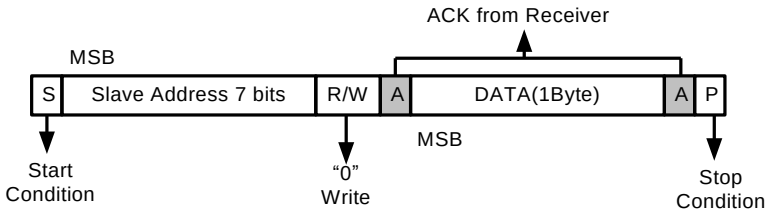


Figure 5-35 Write mode with 7-bits address

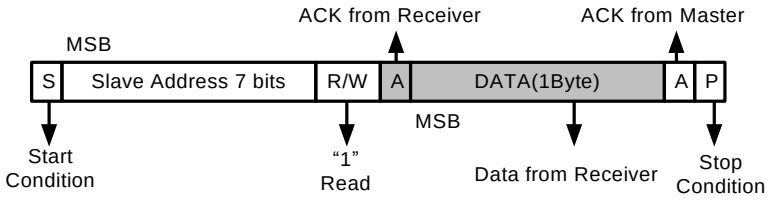


Figure 5-36 Read mode 7-bits address

5.13.2. Bus Arbitration Procedures

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns high. However when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the lowering of SDA line is stronger than maintaining high on the line. For example, one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect low on the bus because "Low" is stronger than "High" even if first master is trying to maintain high on the line. When this occurs, low-generating (as the first bit of address) master will get the mastership and high-generating (as the first bit of address) master should withdraw the mastership. If both masters generate low as the first bit of address, there should be arbitration for second address bit, again. This arbitration will continue to the end of last address bit.

SYSCON1			**Address: 0xAF**		**System Control Register 1**			
Bit	7	6	5	4	3	2	1	0
Function	--	--	ADorDA	SPI_EN	I2CEN	I2C_AUTO_RW	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	--	Reserved	
5	ADorDA	R	I2C Address or Data indication bit for slave mode 0: Address 1: Data	
4	SPI_EN	R/W	SPI signals forward to P1[7:4] enable P1[4]: SPI_TX P1[5]: SPI_CLK P1[6]: SPI_RX P1[7]: SPI_CSB	
3	I2CEN	R/W	Change P2[3:2] to I2C usage. 0: P2[3:2] is used as GPIO. 1: P2[3:2] is used as I2C interface.	

Bit	Function	Type	Description	Condition
2	I2C_AUTO_RW	R/W	I2C auto read write mode enable bit (for slave mode) 0: Disable 1: Enable	
1	IRTX_SW	R/W	IRTX pin selection bit 0: IRTX pin in on P21 1: IRTX pin in on P34	
0	--	--	Reserved	

Table 5-98 SYSCON1 register

I2CCON			Address: 0xDA		I2C Control Register			
Bit	7	6	5	4	3	2	1	0
Function	ACKEN	CLKSEL	I2CIE	I2CIF	TXCLK[3:0]			
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ACKEN	R/W	I2C-bus acknowledgement enable bit 0: Disable ACK generation 1: Enable ACK generation	
6	CLKSEL	R/W	Source clock of I2C-bus transmit clock pre-scaler selection bit 0: I2CCLK=SYSCLK/16 1: I2CCLK= SYSCLK /512	
5	I2CIE	R/W	I2C Bus TX/RX Interrupt Enable 0: Disable 1: Enable	
4	I2CIF	R/W	I2C Bus TX/RX Interrupt Flag Clear by the software A I2C bus interrupt occurs 1. When a 1-byte transmitting or receiving operation is terminated. 2. When a general call or slave address match occurs. 3. If bus arbitration fails.	
3:0	TXCLK[3:0]	R/W	I2C-Bus transmit clock pre-scaler. Transmit clock frequency is determined by this 4-bit pre-scaler value, according to the following formula: TX clock = I2CCLK/(TXCLK[3:0]+1) **NOTES:** 1. I2CCLK is determined by CLKSEL	

Table 5-99 I2CCON register

I2CSTS			Address: 0xDB		I2C Status Register			
Bit	7	6	5	4	3	2	1	0
Function	MODE[1:0]		BUSY	DataEN	ArbS	SS	GC	ACK
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	MODE[1:0]	R/W	I2C-bus master/slave Tx/Rx mode select bits:	

Bit	Function	Type	Description	Condition
			00 = Slave receive mode. 01 = Slave transmit mode. 10 = Master receive mode. 11 = Master transmit mode. NOTE: Under following two situations, the I2C mode will change to slave receive mode automatically. In slave mode, receives slave address 0x00. In master mode, detects bus arbitration failed.	
5	BUSY	R/W	Read: I2C-Bus busy signal status bit: 0 = I2C-bus not busy 1 = I2C-bus busy Write: 0: I2C-bus interface STOP signal generation 1: a. I2C-bus interface START signal generation b. If BUSY is set by software as an active Master, a repeated START will be generated after the next ACK cycle	
4	DataEn	R/W	I2C-bus data output enable/disable bit: 0 = Disable Rx/Tx 1 = Enable Rx/Tx	
3	ArbS	R	I2C-bus arbitration procedure status flag bit: 0 = Bus arbitration status okay 1 = Bus arbitration failed during serial I/O	
2	SS	R	I2C-bus address-as-slave status flag bit: 0 = START/STOP condition is generated 1 = Received slave address matches the address value in the I2CADR.	
1	GC	R	I2C-bus address zero status flag bit (General call): 0=START/STOP condition is generated 1=Received slave address is "0x00"	
0	ACK	R	I2C-bus last-received bit status flag bit: 0 = Last-received bit is "0" (ACK is received) 1 = Last-received bit is "1" (ACK is not received)	

Table 5-100 I2CSTS register

I2CADR			Address: 0xDC		I2C Address Register			
Bit	7	6	5	4	3	2	1	0
Function	Addr[7:1]							--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:1	Addr[7:1]	R/W	7-bit slave address, latched from the I2C-bus: It is allowable to read IAR value at any time — Slave address = [7:1]	

Bit	Function	Type	Description	Condition
			— Not mapped = [0]	
0	--	--	Reserved	

Table 5-101 I2CADR register

I2CDAT			Address: 0xDD		I2C Data Register			
Bit	7	6	5	4	3	2	1	0
Function	Data[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	Data[7:0]	R/W	8-bit data shift register for I2C-bus TX/RX operation: It is allowable to read the I2CDAT value at any time.	

Table 5-102 I2CDAT register

I2CDEB			Address: 0xDE		I2C De-bounce Clock Register			
Bit	7	6	5	4	3	2	1	0
Function	DEBCLK[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DEBCLK[7:0]	R/W	De-bounce Clock I2C input signal will be latched every DEBCLK cycles of system clock. 1~256: 1~256 cycles of system clock	

Table 5-103 I2CDEB register

5.14. Carrier Modulator/Demodulator Timer

In GPM8F1129/1065/1033/1019A, there are two timers, timer A and timer B, for Carrier Modulator/Demodulator Timer module. One is an 8-bit up counter and one is a 16-bit up counter. Timer A is special for generating carrier signal and capturing the frequency of input signal in IR control application. Timer B is used as modulator/demodulator for envelop generation and detection. Three operation modes, including PWM output with carrier mode, PWM output with no carrier mode, and direct control mode, are included, which will be described in the following sections. Moreover, one space extension function is realized in CMDT module. Figure 5-37 shows the overall block diagram of CMDT module and Table 5-104 lists the features of Timer A and Timer B.

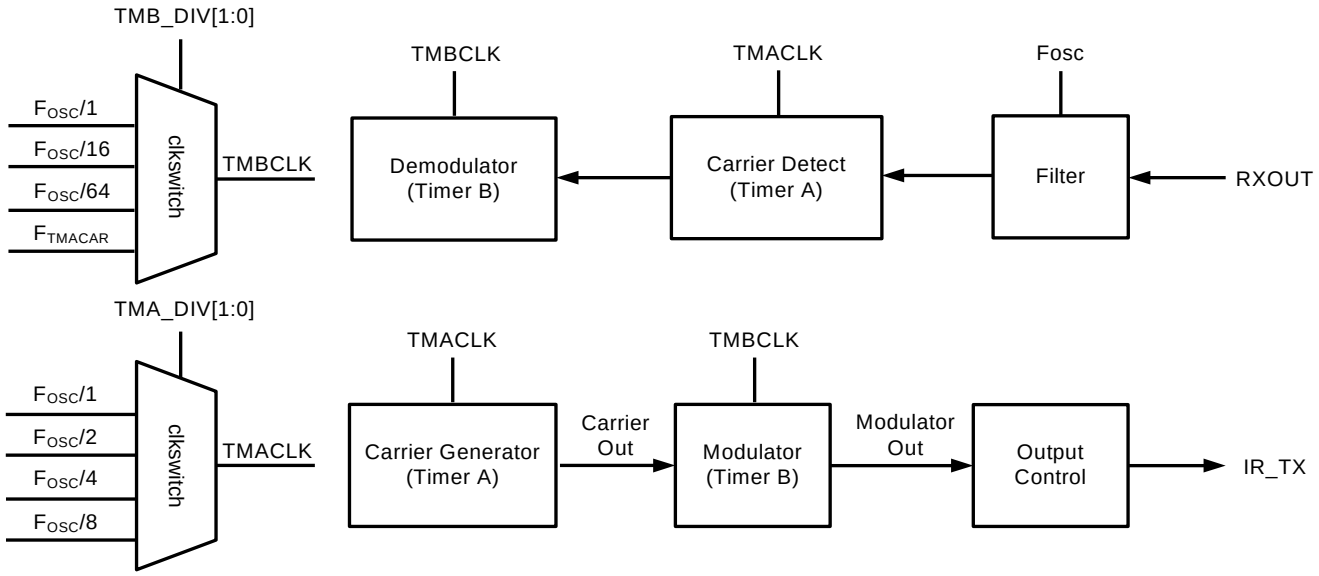


Figure 5-37 The block diagram of CMDT module

Timer	Timer A	Timer B
Feature 1	Readable and writable	Readable and writable
Feature 2	Clock source selectable	Clock source selectable
Feature 3	Interrupt-on-overflow from #$FF to #$00	Interrupt-on-overflow from #$FFFF to #$0000
Feature 4	Support PWM with carrier signal mode	Support PWM without carrier signal mode
Feature 5	NA	Gate the output with PWM with carrier signal mode
Feature 6	Detection of input carrier signal in IR control application	Detection of input envelop signal in IR control application

Table 5-104 The features of Timer A and Timer B

5.14.1. Carrier Generator

Timer A is used as carrier generator and consists of an 8-bit register. It is an up counter with input clock selectable (Fosc/1, Fosc/2, Fosc/4, and Fosc/8), which can be configured by control of TMA_DIV[1:0]. The resolution of timer A is from 62.5ns to 500ns based on different setting of TMA_DIV[1:0] with 16MHz internal oscillator. The carrier signal is generated by PERIOD register and DUTY register. PERIOD register controls carrier period and DUTY register controls the duty of carrier signal. After enabling Timer A, it starts to count and the carrier output is driving high. After each increment, the contents of the counter are compared with duty register and period register. If the count value in the timer register is larger than duty value, a low output signal is generated at carrier out. If the count value in the timer register is reached to period value, a high output is produced and the counter is reset and continues to increase. The periodic signal, carrier output, is generated in this way. The rising flag and falling flag (RISEIF and FALLIF) are set respectively at the rising edge and falling edge of carrier signal, this provides user a means to update new period and duty registers. Figure 5-38 and Figure 5-39 show the block and timing diagram of Timer A module. Table 5-105 lists the resolution and frequency range of the carrier signal with 16MHz internal oscillator.

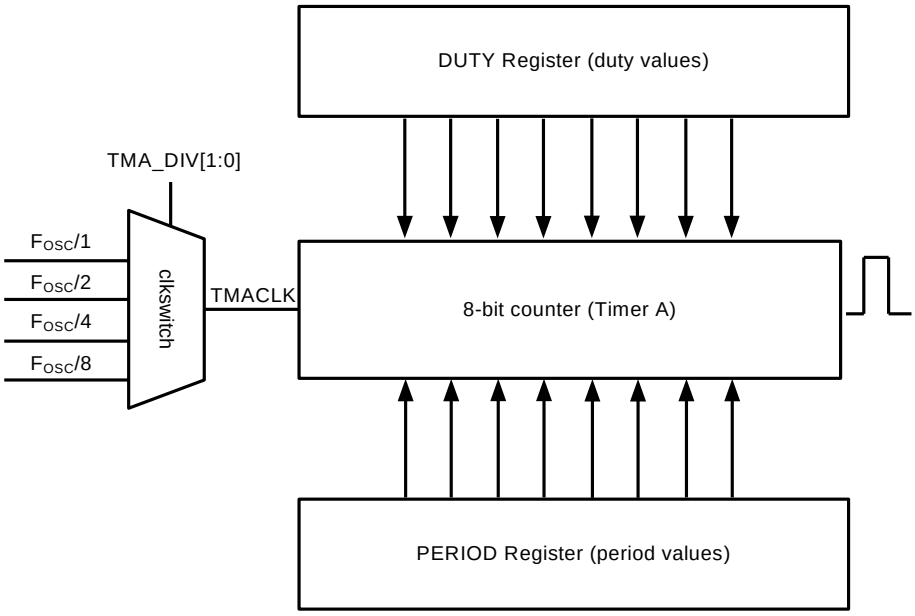


Figure 5-38 The block diagram of Timer A module

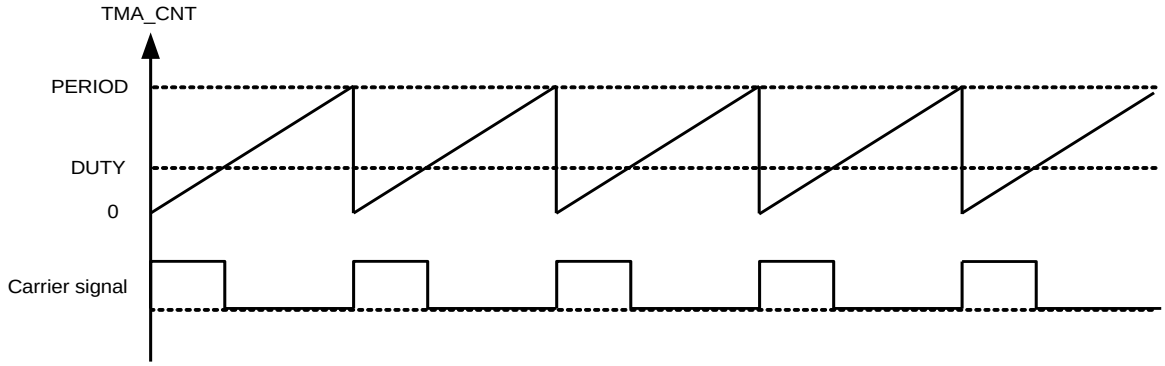


Figure 5-39 The timing diagram of Timer A module

TMA_DIV[1:0]	Carrier generator resolution	Minimum carrier frequency	Maximum carrier frequency
2'b00(16MHz)	0.0625us	62.75KHz	8MHz
2'b01(8MHz)	0.125us	31.37KHz	4MHz
2'b10(4MHz)	0.25us	15.69KHz	2MHz
2'b11(2MHz)	0.5us	7.84KHz	1MHz

Table 5-105 The resolution and frequency range of the carrier signal with 16MHz internal oscillator.

Carrier frequency	TMA_DIV[1:0]	Period register setting	Actual frequency	Error deviation (%)
15KHz	2'b11(TMACLK=2MHz)	0x85(133)	15.0376KHz	0.25%
36KHz	2'b10(TMACLK=4MHz)	0x6F(111)	36.0360KHz	0.10%
38KHz	2'b10(TMACLK=4MHz)	0x69(105)	38.0952KHz	0.25%
40KHz	2'b10(TMACLK=4MHz)	0x64(100)	40.0000KHz	0.00%
56KHz	2'b10(TMACLK=4MHz)	0x47(71)	56.3380KHz	0.60%
100KHz	2'b10(TMACLK=4MHz)	0x04(4)	40.0000KHz	0.00%

Table 5-106 Carrier frequency setting example

5.14.2. Modulator

Modulator module is realized by Timer B, it is special for envelope signal generation with gating the carrier onto the modulator output in IR controller application. The 16-bit timer is an up counter with input clock selectable (Fosc/1, Fosc/16, Fosc/64, FTMACAR) via TMB_DIV[2:0]. The minimum resolution of timer B is 62.5ns with Fosc/1 setting by TMB_DIV[2:0]. The envelop signal is generated by counting the number of input clocks for both mark and space times. The mark and space time values are programmable by two MARK/SPACE data registers. After each increment, the contents of the counter are compared with mark/space data registers. If the count value in the timer register matches the stored mark/space value, an appropriate output signal is generated at a modulator out. For example, if counter is compared with MARK register now, a match will cause the modulator output to be driven low, the counter continues to increase and the compare register is directed to the SPACE register until next match is achieved. When match is reached, counter is reset and the modulator output would be driven high. The flags of MARK and SPACE (MARKIF and SPACEIF) are set respectively when a compared is match, this provides user a means to update new MARK and SPACE registers in advance. Figure 5-40 and Figure 5-41 show the block and timing diagram of Timer B module. Table 5-107 lists the resolution and the period range of the envelop signal with 16MHz internal oscillator.

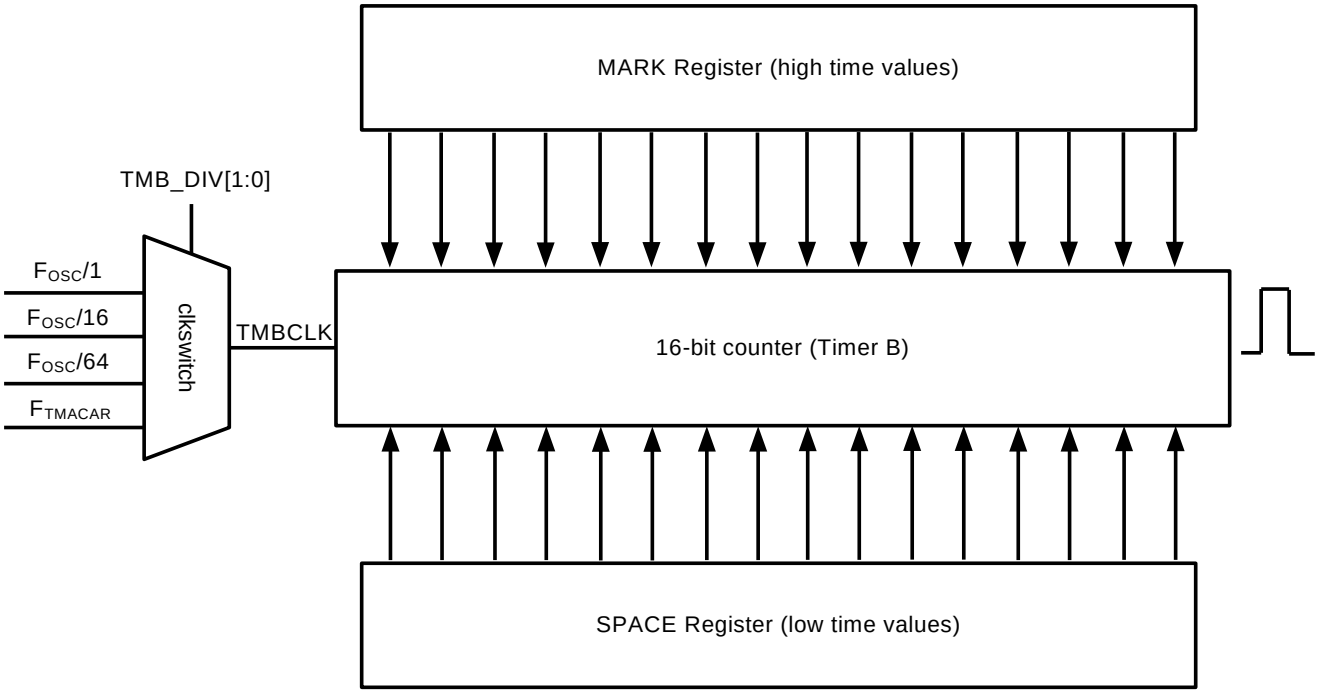


Figure 5-40 The block diagram of Timer B module

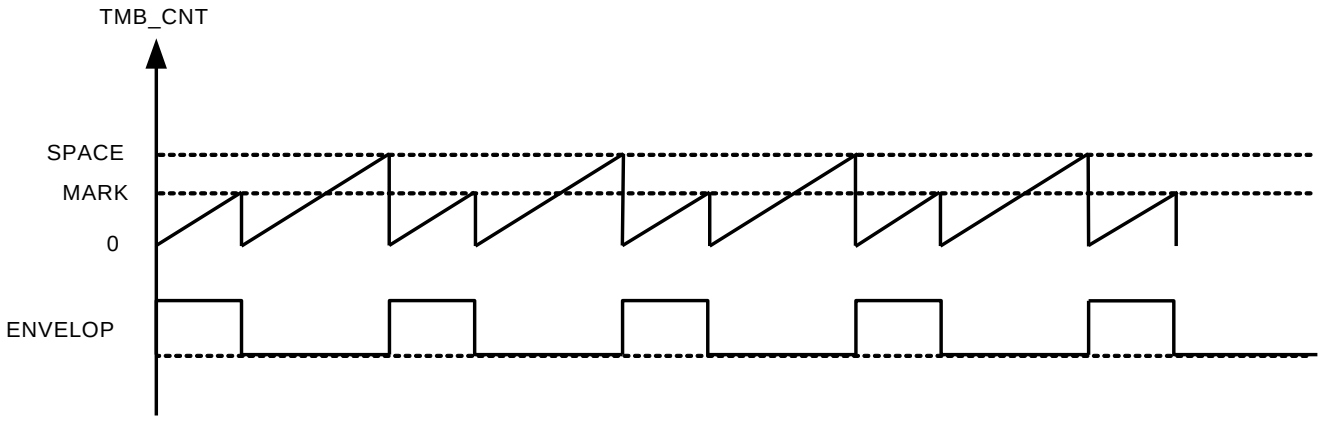


Figure 5-41 The timing diagram of Timer B module

TMB_DIV[1:0]	Envelop resolution	Minimum envelop period	Maximum envelop period
2'b00(16MHz)	62.5ns	125ns(MARK=62.5ns/SPACE=62.5ns)	81.92us(MARK=40.96us/SPACE=40.96us)
2'b01(1MHz)	1us	2us(MARK=1us/SPACE=1us)	131.07ms(MARK=65.535ms/SPACE=65.535ms)
2'b10(0.25MHz)	4us	8us(MARK=4us/SPACE=4us)	524.28ms
2'b11	carrier frequency	2÷FTMACARR	(65535*2)÷FTMACARR

Table 5-107 The resolution and period range of the envelop signal with 16MHz internal oscillator

5.14.2.1. PWM output with carrier signal mode

In the PWM output with carrier signal mode, user can independently defines the duty and the frequency of carrier signal by duty and period registers. The modulator gate is open and the carrier output is transmitted to IR_TX. The enable bit of Timer A should be set first by TMAEN bit in order to start the function of timer A. Figure 5-42 shows the timing diagram of PWM output with carrier signal mode.

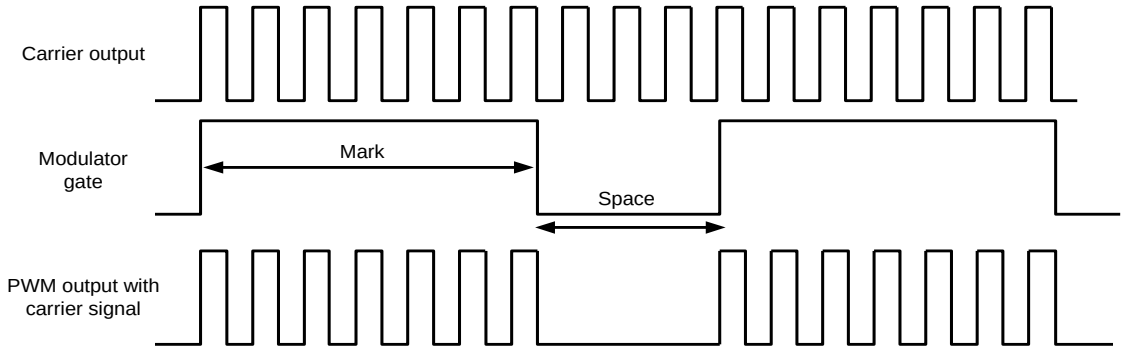


Figure 5-42 The timing diagram of PWM output with carrier signal mode

5.14.2.2. PWM output without carrier signal mode

In the PWM output without carrier signal mode, the mark and space period is based on the mark and space counts of timer B resolution. It is similar to PWM output with carrier signal mode, the only difference is the carrier signal is not transmitted to IR_TX. The PWM output is logic 1 in the mark period and is logic 0 in the space period.

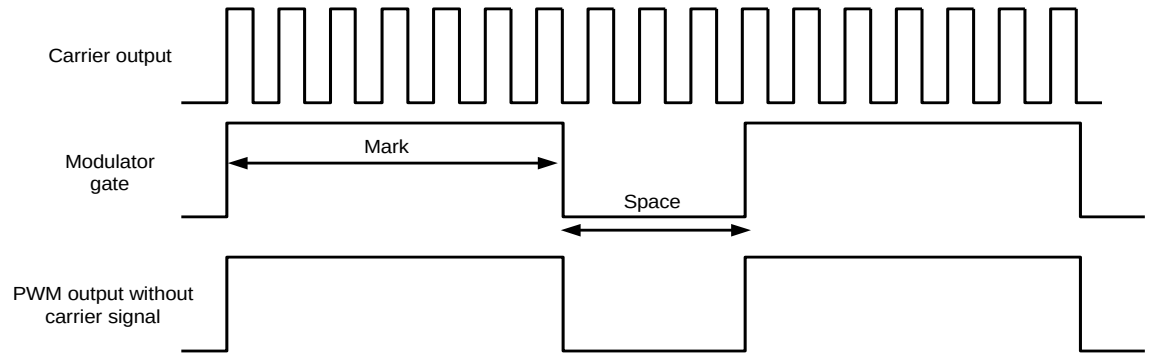


Figure 5-43 The timing diagram of PWM output without carrier signal mode

5.14.2.3. Direct control mode

This mode enables user to directly control the state of the IR_TX pin by writing to the TX_STATE bit by software. In this mode, TMAEN and TMBEN bit must be disabled and IRTX_EN must be enabled to accomplish this function which the output of IR_TX is totally controlled by the TX_STATE bit.

5.14.3. Output control

The output control block controls the state of IR_TX no matter carrier modulator/demodulator timer is enabled or disabled. If carrier modulator/demodulator timer is enabled, a polarity bit controls the high true or low true of IR_TX output. If carrier modulator/demodulator timer is disabled, the state of IR_TX is only controlled by the TX_STATE bit.

5.14.4. Extended space operation

In PWM output with carrier signal mode and PWM output without carrier signal mode, the space period can be extended than the expected value of the space registers. Setting the EXSPC bit will force the modulator output into the extended space mode and the following mark and space period will be treated as space period. The length of extended space period is equal to the number multiplied by 65536 plus space times(2^{16} ×n+N_{space}). Clearing EXSPC bit will return modulator to the normal operation. Figure 5-44 shows the timing diagram of extended space operation. Setting EXSPC should be during Mark period, and clearing EXSPC should be before timer 2 overflow(TMBOIF).

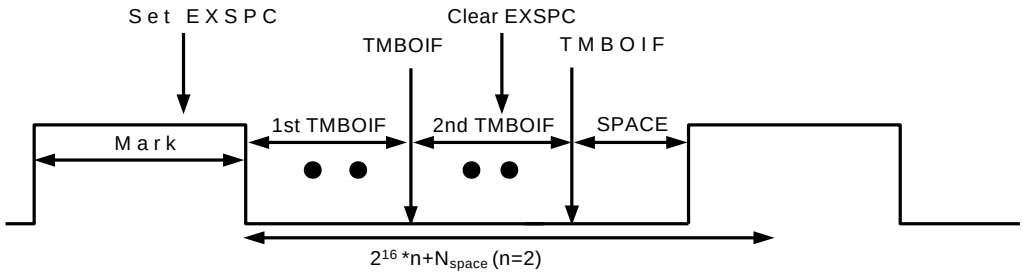


Figure 5-44 The timing diagram of extended space operation

CMDTCON			Address: 0xB1		CMDT Control Register			
Bit	7	6	5	4	3	2	1	0
Function	IRTX_EN	TX_STATE	ENVDET	EXSPC	PWM_MODE	POLARITY	TMBEN	TMAEN
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	IRTX_EN	R/W	IR_TX pin enable bit 0: P21 is used as GPIO 1: P21 is used as IR_TX pin	
6	TX_STATE	R/W	The state of IR_TX when TMAEN,TMBEN=0 and IRTX_EN=1 0: Low state 1: High state	
5	ENVDET	R	Envelop status	
4	EXSPC	R/W	Extended space operation enable bit	
3	PWM_MODE	R/W	Modulator output mode 0: PWM output with carrier signal mode 1: PWM output without carrier signal mode	
2	POLARITY	R/W	The polarity of IR_TX when IR_TX pin is enabled 0: IR_TX is IR_TX 1: IR_TX is inverse of IR_TX	
1	TMBEN	R/W	Timer B timer function enable bit	
0	TMAEN	R/W	Timer A timer function enable bit	

Table 5-108 CMDTCON register

SYSCON1			Address: 0xAF		System Control Register 1			
Bit	7	6	5	4	3	2	1	0
Function	--	--	ADorDA	SPI_EN	I2CEN	I2C_AUTO_RW	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:6	--	--	Reserved	
5	ADorDA	R	I2C Address or Data indication bit for slave mode 0: Address 1: Data	
4	SPI_EN	R/W	SPI signals forward to P1[7:4] enable P1[4]: SPI_TX P1[5]: SPI_CLK P1[6]: SPI_RX P1[7]: SPI_CSB	
3	I2CEN	R/W	Change P2[3:2] to I2C usage. 0: P2[3:2] is used as GPIO. 1: P2[3:2] is used as I2C interface.	
2	I2C_AUTO_RW	R/W	I2C auto read write mode enable bit (for slave mode) 0: Disable 1: Enable	
1	IRTX_SW	R/W	IRTX pin selection bit 0: IRTX pin in on P21 1: IRTX pin in on P34	
0	--	--	Reserved	

Table 5-109 SYSCON1 register

CAPCON			Address: 0xB2		CAPTURE Control Register			
Bit	7	6	5	4	3	2	1	0
Function	CAPB_MODE	CAPB_EN	TMB_DIV[1:0]		RXOUT_INV	CAPA_MODE	TMA_DIV[1:0]	
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	CAPB_MODE	R/W	0: Timer B captures at every changing state 1: Timer B captures at 1st CAPAIF and TMAOIF	
6	CAPB_EN	R/W	Timer B capture function enable bit	
5:4	TMB_DIV[1:0]	R/W	Timer B input clock selection 00: SYSCLK/1 01: SYSCLK/16 10: SYSCLK/64 11: F_{TMACAR}	
3	RXOUT_INV	R/W	0: RXOUT = RXOUT_p 1: RXOUT = ~RXOUT_p	
2	CAPA_MODE	R/W	0: capture mode is off 1: RXOUT captures at every rising edge	
1:0	TMA_DIV[1:0]	R/W	Timer A input clock selection 00: SYSCLK/1 01: SYSCLK/2 10: SYSCLK/4 11: SYSCLK/8	

Table 5-110 CAPCON register

TMAIF			Address: 0xB3		Timer A Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	--	--	--	CAPAIF	TMAOIF	FALLIF	RISEIF	TMAIE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:5	--	R/W	Reserved	
4	CAPAIF	R/W	Timer A capture flag	
3	TMAOIF	R/W	Timer A overflow flag	
2	FALLIF	R/W	Falling edge flag of carrier output	
1	RISEIF	R/W	Rising edge flag of carrier output	
0	TMAIE	R/W	Timer A interrupt enable bit	

Table 5-111 TMAIF register

PERIOD			Address: 0xB4		Carrier Period Register			
Bit	7	6	5	4	3	2	1	0
Function	PERIOD[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	PERIOD	R/W	Carrier period register	

Table 5-112 PERIOD register

DUTY			Address: 0xB5		Carrier Duty Register			
Bit	7	6	5	4	3	2	1	0
Function	DUTY[7:0]							
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7:0	DUTY	R/W	Carrier duty register	

Table 5-113 DUTY register

TMBIF			Address: 0xBA		Timer B Interrupt Flag Register			
Bit	7	6	5	4	3	2	1	0
Function	ENVDETIF	MASK_oe	FCAPBIF	RCAPBIF	TMBOIF	SPACEIF	MARKIF	TMBIE
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	ENVDETIF	R/W	ENVDET rising and falling flag	7
6	MASK_oe	R/W	Timer B capture flag masking enable bit 0: RCAPBIF, FCAPBIF is not masked 1: RCAPBIF, FCAPBIF is masked	
5	FCAPBIF	R/W	Timer B falling capture flag	
4	RCAPBIF	R/W	Timer B rising capture flag	
3	TMBOIF	R/W	Timer B overflow flag	

Bit	Function	Type	Description	Condition
2	SPACEIF	R/W	Space flag when count of timer B is match to space register	
1	MARKIF	R/W	Mark flag when count of timer B is match to mark register	
0	TMBIE	R/W	Timer B interrupt enable bit	

Table 5-114 TMBIF register

MARKH			Address: 0xBC		MSB of Mark Register			
Bit	7	6	5	4	3	2	1	0
Function	MARK[15:8]							
Default	1	1	0	0	0	0	0	0

MARKL			Address: 0xBB		LSB of Mark Register			
Bit	7	6	5	4	3	2	1	0
Function	MARK[7:0]							
Default	0	0	0	0	0	0	0	0

Table 5-115 MARK register

SPACEH			Address: 0xBE		MSB of Space Register			
Bit	7	6	5	4	3	2	1	0
Function	SPACE[15:8]							
Default	1	1	0	0	0	0	0	0

SPACEL			Address: 0xBD		LSB of Space Register			
Bit	7	6	5	4	3	2	1	0
Function	SPACE[7:0]							
Default	0	0	0	0	0	0	0	0

Table 5-116 SPACE register

5.14.5. Carrier detect and demodulator

In IR learning function application, Timer A and Timer B should be configured as capture mode for measuring the period and envelop of input signal from IR_RX pin. Timer A is an 8 bit up count timer which counts from a 0x00 value with input clock and captures at every rising edge for the information of carrier period. The count of timer A is captured to DUTY register. Timer B is a 16-bit up counter and is used to capture the information of envelop. The capture mode of Timer B should be set to '0' first to determine what kind of input signal it is(PWM output with carrier mode or PWM output without carrier mode). In this mode, Timer B captures at every changing state with CAPB_MODE=0. The counts of timer B are captured to MARK register at falling edge of RXOUT, and are captured to SPACE register at rising edge of RXOUT. After several captures, if no TMAOIF occurs, input signal is supposed to be PWM output with carrier mode. At this time, user needs to change capture mode of Timer B to '1' to capture ENVDET signal. In this mode, TMAOIF would capture the count of timer B to MARK registers and reset timer B and 1st CAPAIF would capture the count of timer B to SPACE registers. In this case, Timer A contents must be reloaded with 0xFF-T -OFFSET by software and OFFSET value is decided by user for the count margin. When the timer A overflows, the overflow interrupt (TMAOIF) occurs(that's over 256* TMACLK), it makes ENVDET changed to "0", so check ENVDET bit can know whether envelope exist or not. As to space period, If the counter for space period is over 0xFFFF, then its length equals to n_{TMBOIF}*0xFFFF + space value. Figure 5-45 and Figure 5-46 show the block diagram and timing diagram of carrier detect and envelop detecting operation. Figure 5-47 shows the timing diagram of envelop detect for PWM output without carrier mode.

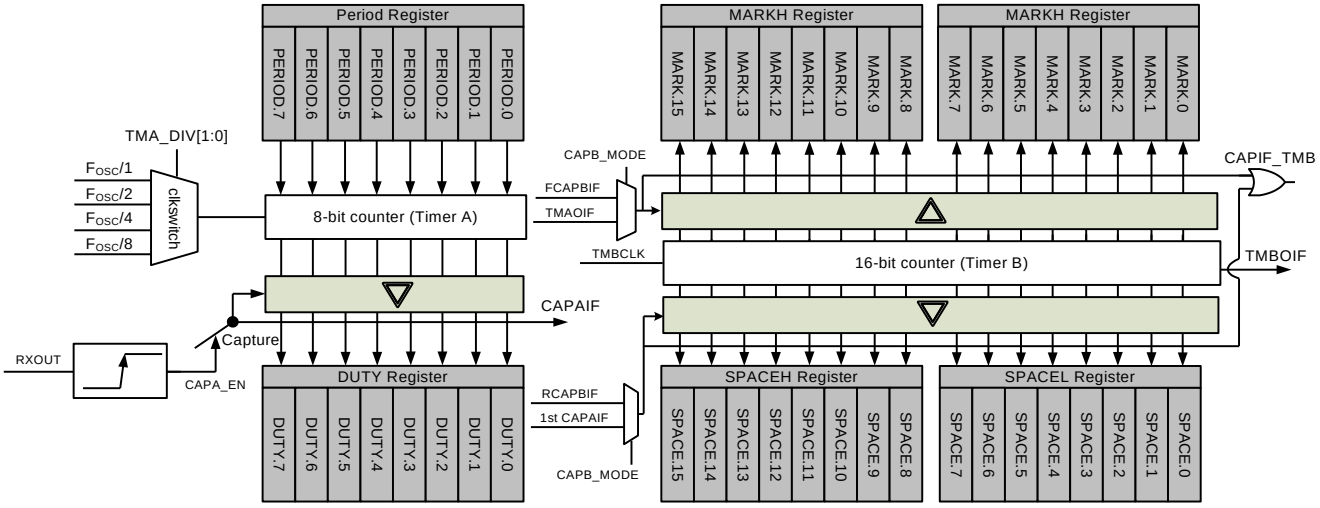


Figure 5-45 The block diagram of carrier detect operation

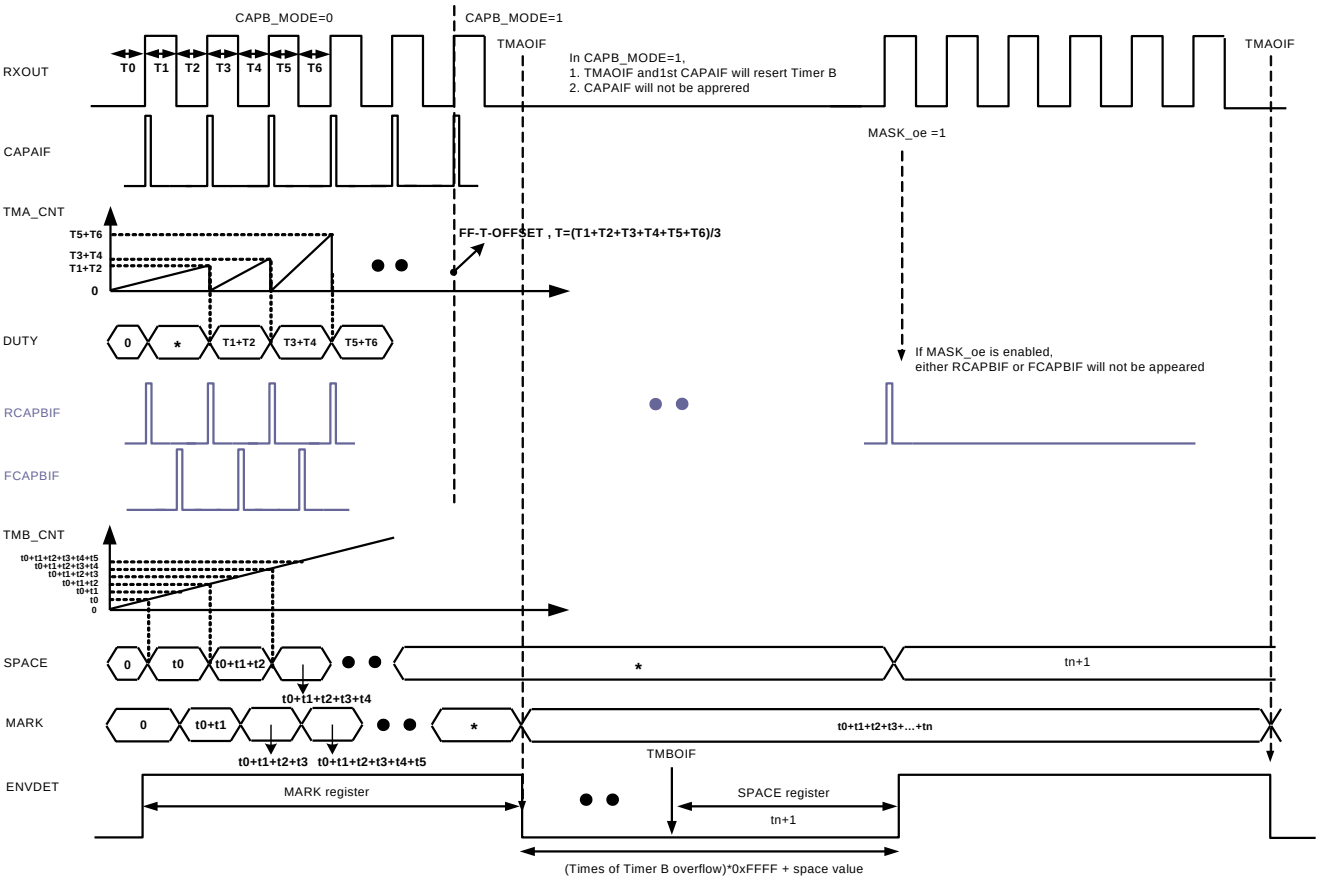


Figure 5-46 The timing diagram of envelop detect for PWM output with carrier mode

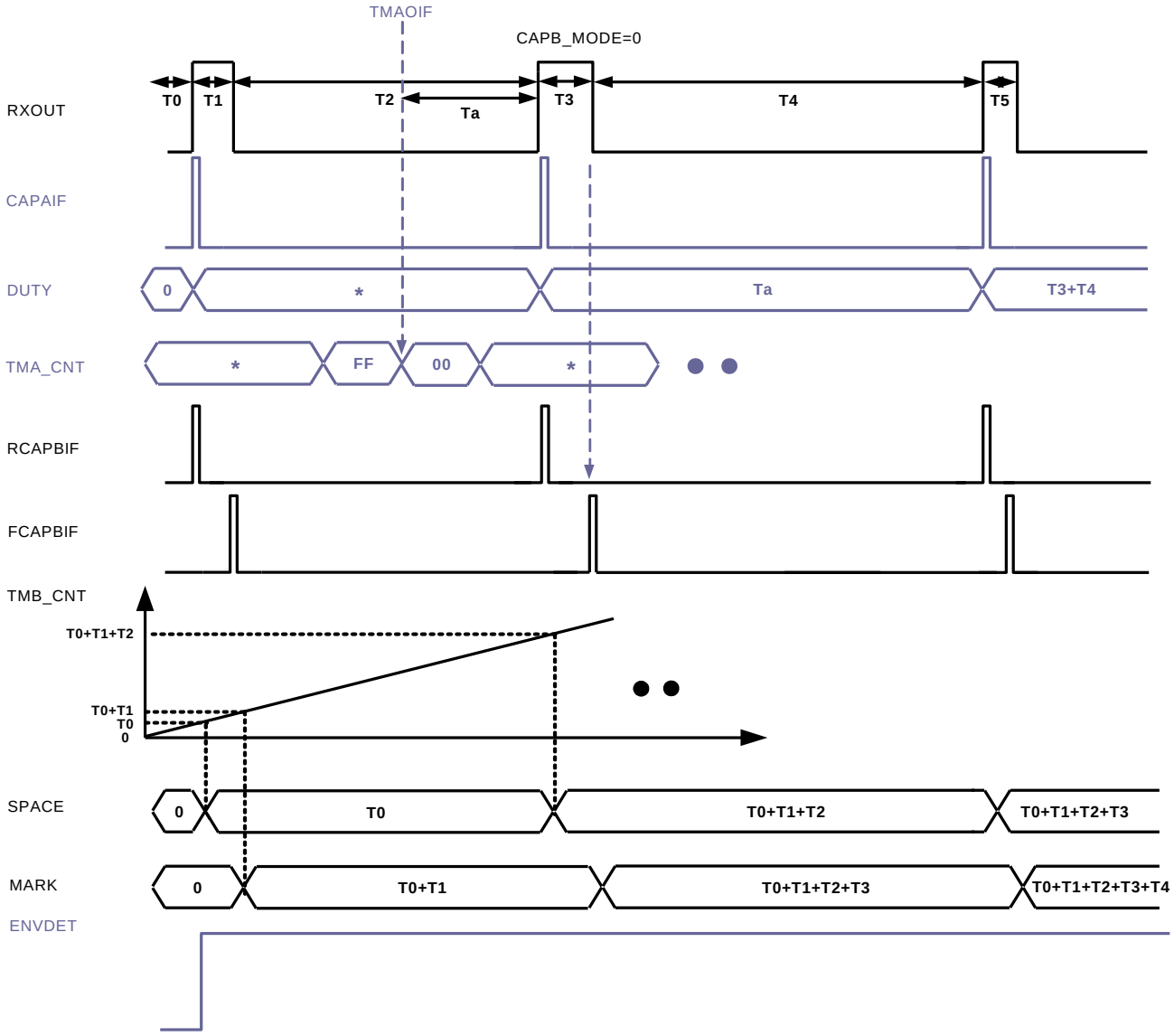


Figure 5-47 The timing diagram of envelop detect for PWM output without carrier mode

RXCON			Address: 0xBF		Receive Control Register			
Bit	7	6	5	4	3	2	1	0
Function	--	RXOUT	FILTER_SEL[1:0]		--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit	Function	Type	Description	Condition
7	--	R/W	Reserved	
6	RXOUT	R	RXOUT status	
5:4	FILTER_SEL[1:0]	R/W	RXOUT filter selection bits 00: 0ns 01: 125ns 10: 375ns 11: 875ns	
5:0	--	R/W	Reserved	5:0

Table 5-117 RXCON register

5.15. Alphabetical List of Instruction Set

5.15.1. Arithmetic Operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A,direct	Add direct byte to accumulator	0x25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A,#data	Add immediate data to accumulator	0x24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A,#data	Add immediate data to A with carry flag	0x34	2	2
SUBB A,Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	1	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	2	3
INC DPTR	Increment data pointer	0xA3	1	1
MUL A,B	Multiply A and B	0xA4	1	2
DIV A,B	Divide A by B	0x84	1	6
DA A	Decimal adjust accumulator	0xD4	1	3

5.15.2. Logic Operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A,direct	AND direct byte to accumulator	0x55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A,#data	AND immediate data to accumulator	0x54	2	2
ANL direct,A	AND accumulator to direct byte	0x52	2	3
ANL direct,#data	AND immediate data to direct byte	0x53	3	3
ORL A,Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A,direct	OR direct byte to accumulator	0x45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A,#data	OR immediate data to accumulator	0x44	2	2
ORL direct,A	OR accumulator to direct byte	0x42	2	3
ORL direct,#data	OR immediate data to direct byte	0x43	3	3
XRL A,Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	0x64	2	2

Mnemonic	Description	Code	Bytes	Cycles
XRL direct,A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	1

5.15.3. Boolean Operations

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C,bit	AND direct bit to carry flag	0x82	2	2
ANL C,/bit	AND complement of direct bit to carry	0xB0	2	2
ORL C,bit	OR direct bit to carry flag	0x72	2	2
ORL C,/bit	OR complement of direct bit to carry	0xA0	2	2
MOV C,bit	Move direct bit to carry flag	0xA2	2	2
MOV bit,C	Move carry flag to direct bit	0x92	2	3

5.15.4. Data Transfers

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A,direct	Move direct byte to accumulator	0xE5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A,#data	Move immediate data to accumulator	0x74	2	2
MOV Rn,A	Move accumulator to register	0xF8-0xFF	1	1
MOV Rn,direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn,#data	Move immediate data to register	0x78-0x7F	2	2
MOV direct,A	Move accumulator to direct byte	0xF5	2	2
MOV direct,Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1,direct2	Move direct byte to direct byte	0x85	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct,#data	Move immediate data to direct byte	0x75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri,#data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR,#data16	Load 16-bit constant into active DPH and DPL in LARGE mode	0x90	3	3
MOV DPTR,#data24	Load 16-bit constant into active DPH and DPL in Flat mode	0x90	4	4
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	0x93	1	5

Mnemonic	Description		Code	Bytes	Cycles
MOVC A,@A+PC	Move code byte relative to PC to accumulator		0x83	1	4
MOVX A,@Ri	Move external RAM (8-bit address) to A	XDM	0xE2-0xE3	1	3*
		SXDM			3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	XDM	0xE0	1	2*
		SXDM			2
MOVX @Ri,A	Move A to external XDM (8-bit address)	ODE inside ROM/RAM	0xF2-0xF3	1	4*
		Other cases			5*
	Move A to external SXDM (8-bit address)	All cases			3
MOVX @DPTR,A	Move A to external XDM (16-bit address)	CODE inside ROM/RAM	0xF0	1	3*
		Other cases			4*
	Move A to external SXDM (16-bit address)	All cases			2
PUSH direct	Push direct byte onto IDM stack		0xC0	2	3
POP direct	Pop direct byte from IDM stack		0xD0	2	2
XCH A,Rn	Exchange register with accumulator		0xC8-0xCF	1	2
XCH A,direct	Exchange direct byte with accumulator		0xC5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator		0xC6-0xC7	1	3
XCHD A,@Ri	Exchange low-order nibble indirect RAM with A		0xD6-0xD7	1	3

5.15.5. Program Branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call (For GPM8F1033A/1019A)	0x11-0xF1	2	4
ACALL addr19	Absolute subroutine call (For GPM8F1129A/1065A)	0x11-0xF1	3	5
LCALL addr16	Long subroutine call (For GPM8F1033A/1019A)	0x12	3	4
LCALL addr23	Long subroutine call (For GPM8F1129A/1065A)	0x12	4	6
RET	Return from subroutine (For GPM8F1033A/1019A)	0x22	1	4
RET	Return from subroutine (For GPM8F1129A/1065A)	0x22	1	5
RETI	Return from interrupt (For GPM8F1033A/1019A)	0x32	1	4
RETI	Return from interrupt (For GPM8F1129A/1065A)	0x32	1	5
AJMP addr11	Absolute jump	0x01-0xE1	2	3
LJMP addr16	Long jump	0x02	3	4
SJMP rel	Short jump (relative address)	0x80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	5
JZ rel	Jump if accumulator is zero	0x60	2	4
JNZ rel	Jump if accumulator is not zero	0x70	2	4
JC rel	Jump if carry flag is set	0x40	2	3
JNC	Jump if carry flag is not set	0x50	2	3
JB bit,rel	Jump if direct bit is set	0x20	3	5
JNB bit,rel	Jump if direct bit is not set	0x30	3	5
JBC bit,direct rel	Jump if direct bit is set and clear bit	0x10	3	5
CJNE A,direct rel	Compare direct byte to A and jump if not equal	0xB5	3	5
CJNE A,#data rel	Compare immediate to A and jump if not equal	0xB4	3	4
CJNE Rn,#data rel	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4
CJNE @Ri,#data rel	Compare immediate to ind. and jump if not equal	0xB6-0xB7	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	0xD8-0xDF	2	4
DJNZ direct,rel	Decrement direct byte and jump if not zero	0xD5	3	5
NOP	No operation	0x00	1	1

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Rating

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{STG}	-65	-	150	˚C	Flash memory blank status
		-40	-	150	˚C	Flash memory programming already performed

6.2. DC Characteristics (VDD = 5V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.8	5	5.5	V	
Operating Current	I_{OP}	-	6	8	mA	F_{CPU} = 16MHz @ 5.5V, no load
		-	5	7	mA	F_{CPU} = 8MHz @ 5.5V, no load
Standby Current	I_{STBY}	-	-	5.0	uA	VDD = 5.5V, TKEY disabled and LVR disabled
		-	-	7.0	uA	VDD = 5.5V, TKEY enabled and LVR disabled
		-	-	9.0	uA	VDD = 5.5V, LVR enabled and TKEY disabled
		-	-	10.0	uA	VDD = 5.5V, TKEY enabled and LVR enabled
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 5.0V
Output High Level	V_{OH}	0.8VDD	-	-	V	I_{OH} = -12mA at VDD = 5.0V
Output Low Level	V_{OL}	-	-	0.2VDD	V	I_{OL} = 12mA at VDD = 5.0V
Input Pull High Resistor	R_{PH}	30	50	70	KΩ	VDD =5.0V
Input Pull High Resistor	R_{PL}	30	50	70	KΩ	VDD = 5.0V
Low Voltage Reset	V_{LVR}	1.9×(1-5%)	1.9	1.9×(1+5%)	V	
Low Voltage Detect	V_{LVD}	2.3/2.5/3.3/3.5×(1-5%)	2.3/2.5/3.3/3.5	2.3/2.5/3.3/3.5×(1+5%)	V	
Flash operation voltage	V_{FLASH}	V_{LVR}	--	--	V	

6.3. DC Characteristics (VDD = 3.3V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	1.8	3.3	3.6	V	
Operating Current	I_{OP}	-	6	8	mA	F_{CPU} = 16MHz @ 3.6V, no load
		-	5	7	mA	F_{CPU} = 8MHz @ 3.6V, no load
Standby Current	I_{STBY}	-	-	4.0	uA	VDD = 3.6V, TKEY disabled and LVR disabled
		-	-	6.0	uA	VDD = 3.6V, TKEY enabled and LVR disabled
		-	-	8.0	uA	VDD = 3.6V, LVR enabled and TKEY disabled

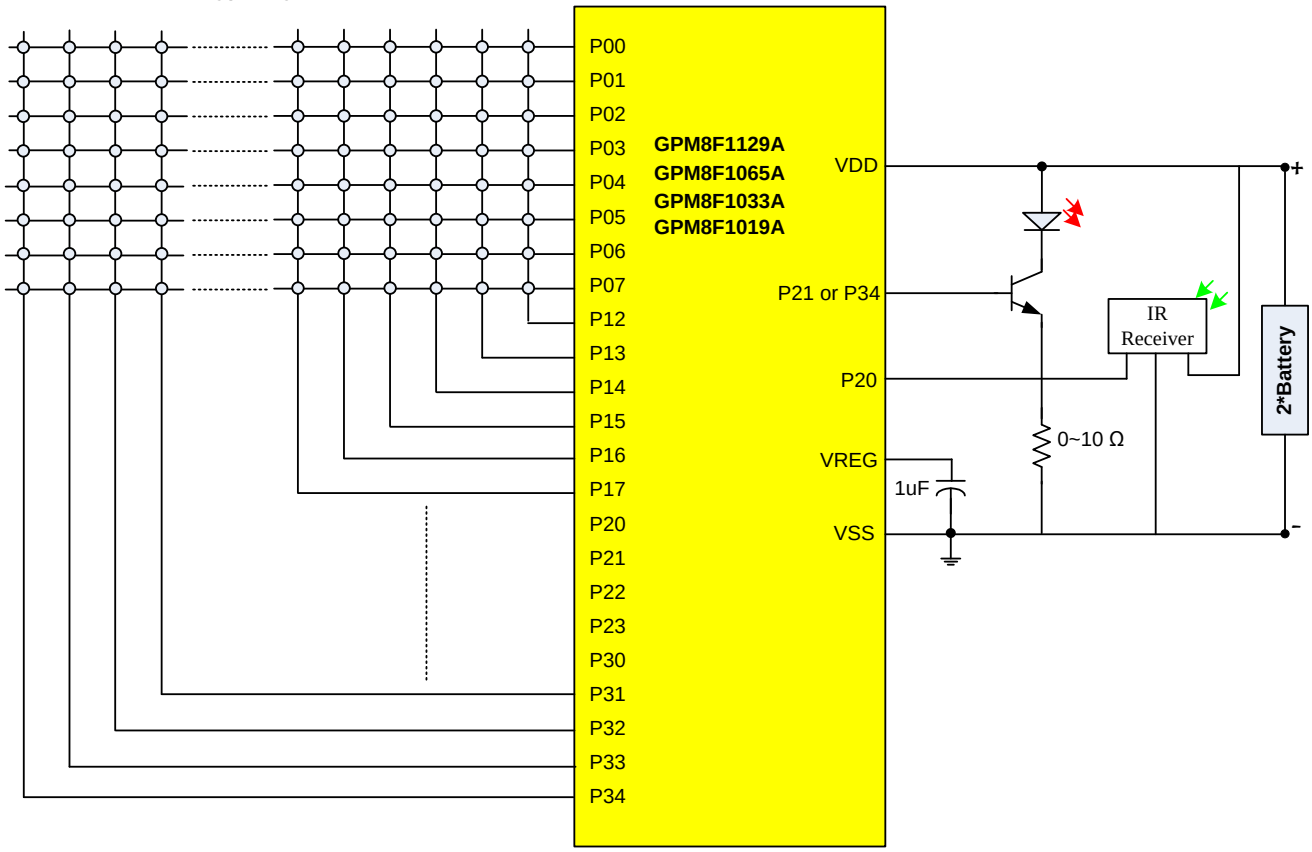
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
		-	-	9.0	uA	VDD = 3.6V, TKEY enabled and LVR enabled
Input High Level	V_{IH}	0.7VDD	-	-	V	VDD = 3.3V
Input Low Level	V_{IL}	-	-	0.3VDD	V	VDD = 3.3V
Output High Level	V_{OH}	0.8VDD	-	-	V	I_{OH} = -7mA at VDD = 3.3V
Output Low Level	V_{OL}	-	-	0.2VDD	V	I_{OL} = 7mA at VDD = 3.3V
Input Pull High Resistor	R_{PH}	30	50	70	KΩ	VDD =3.3V
Input Pull High Resistor	R_{PL}	30	50	70	KΩ	VDD = 3.3V
Low Voltage Reset	V_{LVR}	1.9×(1-5%)	1.9	1.9×(1+5%)	V	
Low Voltage Detect	V_{LVD}	2.3/2.5/3.3/3.5×(1-5%)	2.3/2.5/3.3/3.5	2.3/2.5/3.3/3.5×(1+5%)	V	
Flash operation voltage	V_{FLASH}	V_{LVR}	--	--	V	

6.4. AC Characteristics (T_A = 25℃)

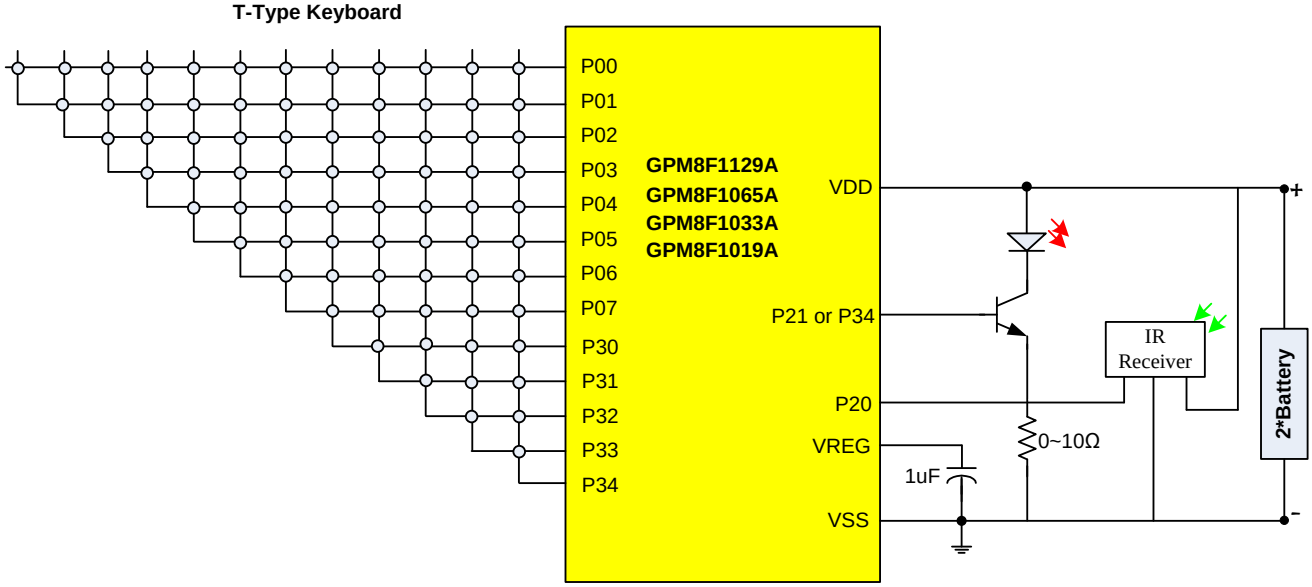
Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
INOSC Frequency	F_{OSC}	16×(1-1.5%)	16	16×(1+1.5%)	MHz	VDD = 2.0~5.5V

7. APPLICATION CIRCUITS

M-Type Keyboard



T-Type Keyboard



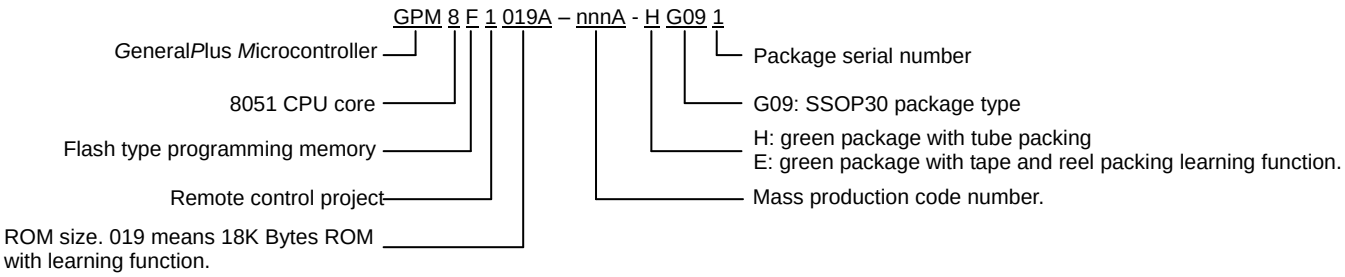
8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type	Packing Information
GPM8F1129A – nnnA – HG09x	Green Package	Tube
GPM8F1065A – nnnA – HG09x	Green Package	Tube
GPM8F1033A – nnnA – HG09x	Green Package	Tube
GPM8F1019A – nnnA – HG09x	Green Package	Tube
GPM8F1129A – nnnA – T	-	Wafer
GPM8F1065A – nnnA – T	-	Wafer
GPM8F1033A – nnnA – T	-	Wafer
GPM8F1019A – nnnA – T	-	Wafer
GPM8F1129A – nnnA – EG09x	Green Package	Tape and Reel
GPM8F1065A – nnnA – EG09x	Green Package	Tape and Reel
GPM8F1033A – nnnA – EG09x	Green Package	Tape and Reel
GPM8F1019A – nnnA – EG09x	Green Package	Tape and Reel

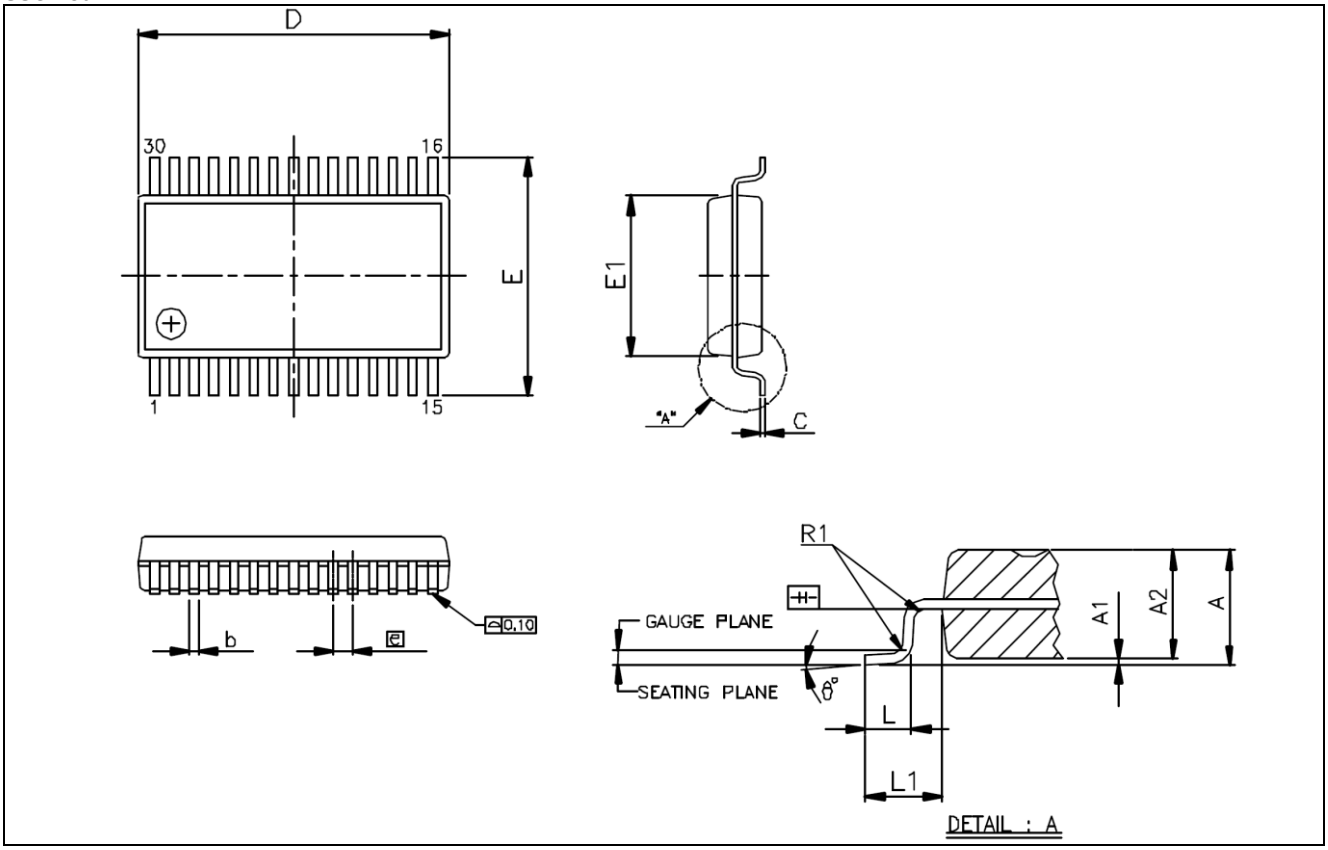
Note:

1. nnn: code number from 000 to 999. To run mass production code, please apply a new code from our sales assistant first. And if no nnnA number, it means a chip without code inside. Ex: GPM8F1129A-HG091 is a standard chip.
2. x: package serial number from 0 to 9. It will depend on the top side mark.
3. Product naming rule: ex: GPM8F1019A-nnnA-HG09x.



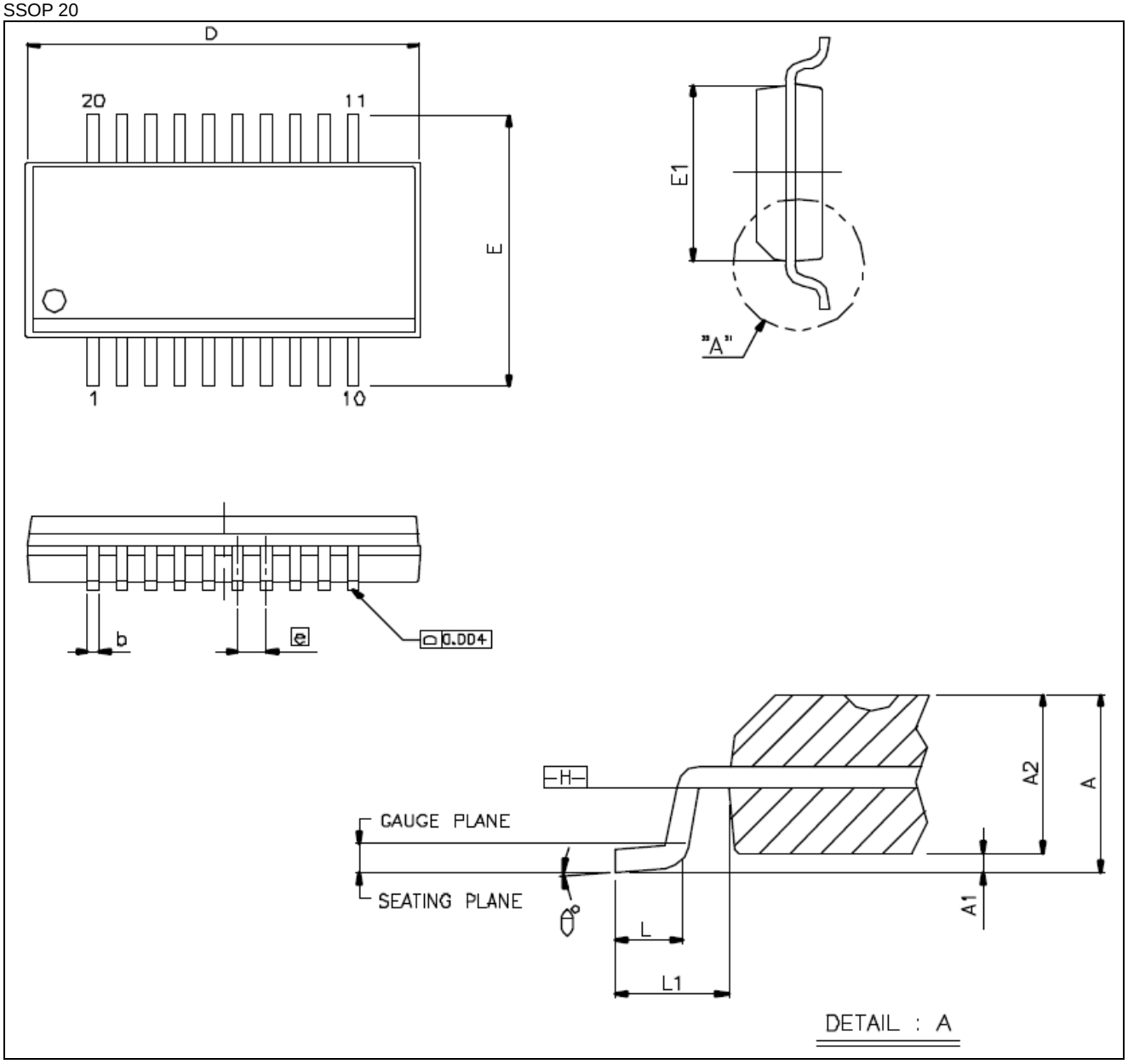
8.2. Package Information

SSOP 30



Symbol	Millimeter		
	Min.	Nom.	Max.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
c	0.09	--	0.21
D	9.90	10.20	10.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF		
R1	0.09	--	--
θ°	0°	4°	8°

SSOP 20



UNIT:INCH

Symbol	Min.	Nom.	Max.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
b	0.008	--	0.012
C	0.007	--	0.010
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
e	0.025 BSC		
L	0.016	0.025	0.050
L1	0.041 REF		
θ°	0°	-	8°

9.DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 28, 2011	0.1	Original	93
Jun. 22, 2012	0.2	1. Modify FL_LEVEL register description on page 16 2. Add FLASHCON register description on page 22 3. Add SRCON register description on page 51 4. Modify Figure 5-46 and Figure 5-47 5. Modify Table 10-1 description on page 90 6. Add Flash program/erase voltage on page 91 and page 92 7. Add GPM8F1129A and GPM8F1065A ordering information on page 95	97
Jul 10, 2012	0.3	1. Add DPX0/DPX1 register description 2. Modify Figure 5-35 and Figure 5-36 3. Add more chip information in chapter 8.1.	98
Aug. 29, 2012	0.4	1. Add KEYCODE data at ACON register on page 27	98
Nov. 26, 2013	0.5	1. Add Alphabetical list of instruction set on page 92 ~ page 95	102
Dec. 08, 2014	0.6	1. Add Storage Temperature information 2. Modify the block diagram of watchdog timer in Figure 5-7 3. Update RSTCON register description 4. Add pad reset deglitch time on page 38 5. Add SSOP20 Pin map and PKG information	104
Jan. 21, 2015	1.0	Update SYSCON1 register description	