SOJ, TSOP, FP-BGA
Commercial Temp
Industrial Temp

128K x 8
1Mb Asynchronous SRAM

7, 8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

Features

- Fast access time: 7, 8, 10, 12 ns
- CMOS low power operation: 140/120/95/80 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: –40° to 85°C
- Package line up
  - J: 400 mil, 32-pin SOJ package
  - TP: 400 mil, 32-pin TSOP Type II package
  - SJ: 300 mil, 32-pin SOJ package
  - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package

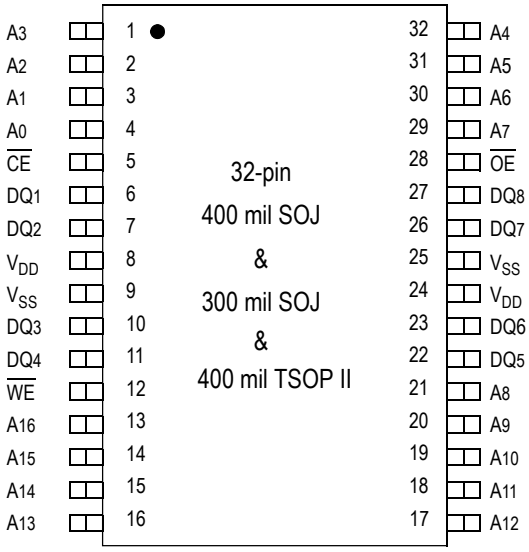
Description

The GS71108A is a high speed CMOS Static RAM organized as 131,072 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS71108A is available in a 6 mm x 8 mm Fine Pitch BGA package, as well as in 300 mil and 400 mil SOJ and 400 mil TSOP Type-II packages.

Pin Descriptions

Symbol	Description
A_0–A_{16}	Address input
DQ_1–DQ_8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

SOJ & TSOP-II 128K x 8-Pin Configuration



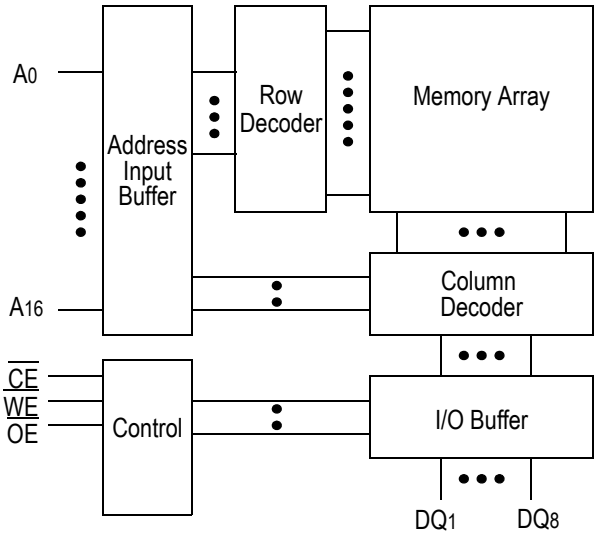
Packages J, TP, and SJ

Fine Pitch BGA 128K x 8-Bump Configuration

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A2	A6	A7	NC
B	DQ1	NC	A1	A5	$\overline{CE}$	DQ8
C	DQ2	NC	A0	A4	NC	DQ7
D	V_{SS}	NC	NC	A3	NC	V_{DD}
E	V_{DD}	NC	NC	NC	NC	V_{SS}
F	DQ3	NC	A14	A11	DQ5	DQ6
G	DQ4	NC	A15	A12	$\overline{WE}$	A8
H	NC	A10	A16	A13	A9	NC

Package U
6 mm x 8 mm, 0.75 mm Bump Pitch
Top View

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	V_{DD} Current
H	X	X	Not Selected	I_{SB1}, I_{SB2}
L	L	H	Read	I_{DD}
L	X	L	Write	
L	H	H	High Z	

Note: X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -7/-8/-10/-12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{AI}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA	2.4	—
Output Low Voltage	V_{OL}	I_{LO} = +4 mA	—	0.4 V

Power Supply Currents

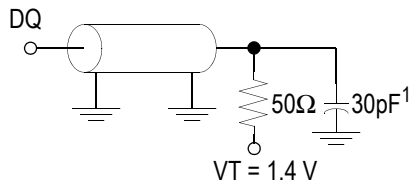
Parameter	Symbol	Test Conditions	0 to 70°C				–40 to 85°C			
			7 ns	8 ns	10 ns	12 ns	7 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	140 mA	120 mA	95 mA	80 mA	145 mA	125 mA	100 mA	85 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	25 mA	20 mA	20 mA	15 mA	30 mA	25 mA	25 mA	20 mA
Standby Current	I_{SB2}	$\overline{CE} \ge V_{DD}$ – 0.2 V All other inputs $\ge V_{DD}$ – 0.2 V or $\le$ 0.2 V	2 mA				5 mA			

AC Test Conditions

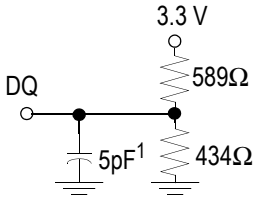
Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}

Output Load 1



Output Load 2



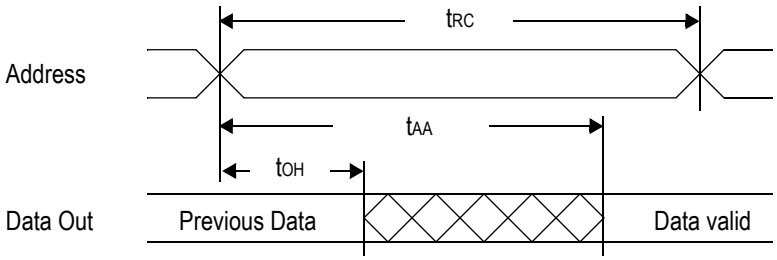
AC Characteristics

Read Cycle

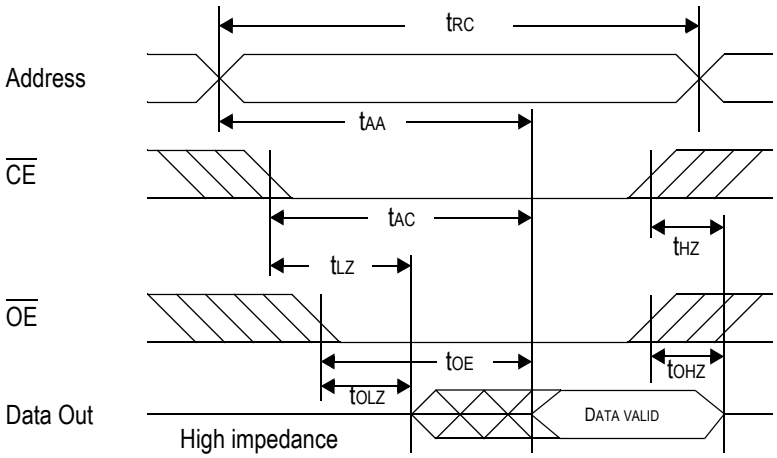
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	7	—	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	7	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	7	—	8	—	10	—	12	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	3.5	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



Read Cycle 2: $\overline{WE}$ = V_{IH}

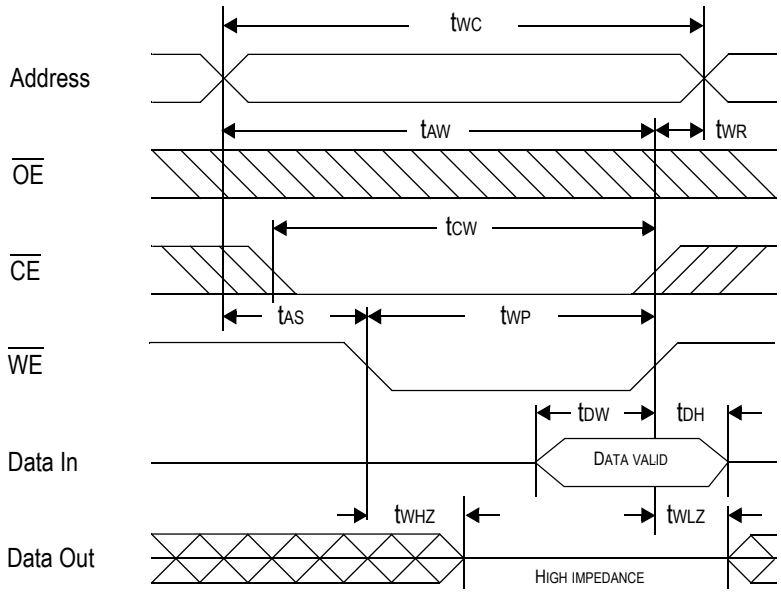


Write Cycle

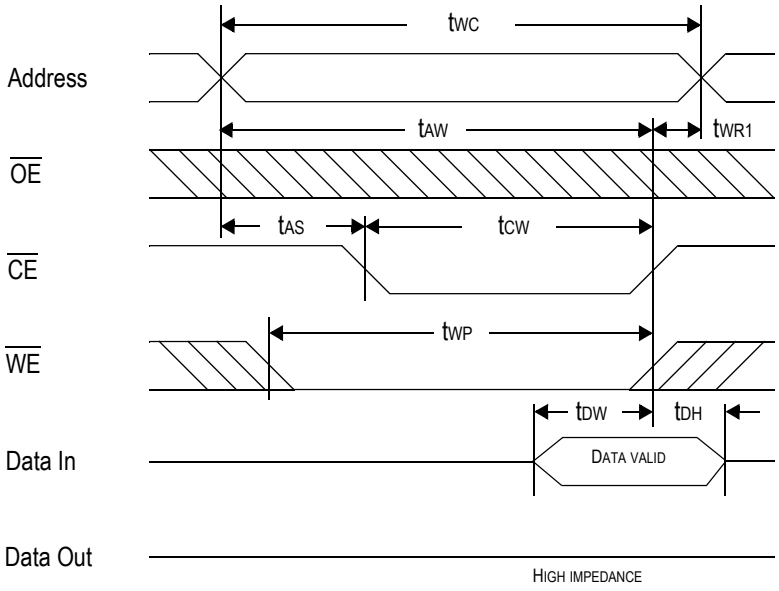
Parameter	Symbol	-7		-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	7	—	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5	—	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5	—	5.5	—	7	—	8	—	ns
Data set up time	tDW	3	—	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	5	—	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested

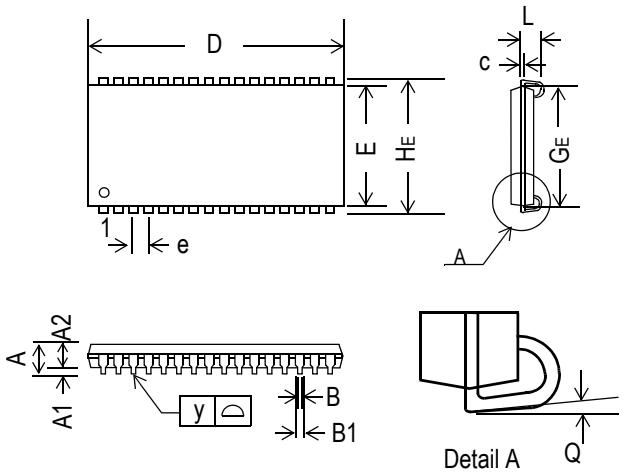
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



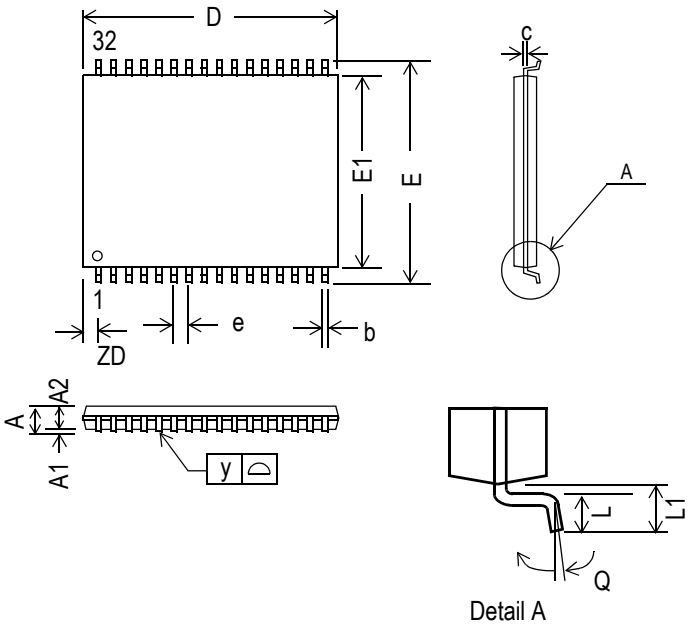
32-Pin SOJ, 400 mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.146	—	—	3.70
A1	0.026	—	—	0.66	—	—
A2	0.105	0.110	0.115	2.67	2.80	2.92
B	0.013	0.017	0.021	0.33	0.43	0.53
B1	0.024	0.028	0.032	0.61	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.824	0.829	20.83	20.93	21.06
E	0.395	0.400	0.405	10.04	10.16	10.28
e	—	0.05	—	—	1.27	—
HE	0.430	0.435	0.440	10.93	11.05	11.17
GE	0.354	0.366	0.378	9.00	9.30	9.60
L	0.082	—	—	2.08	—	—
y	—	—	0.004	—	—	0.10
Q	0^o	—	10^o	0^o	—	10^o

Notes:
1. Dimension D& E do not include interlead flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: inches

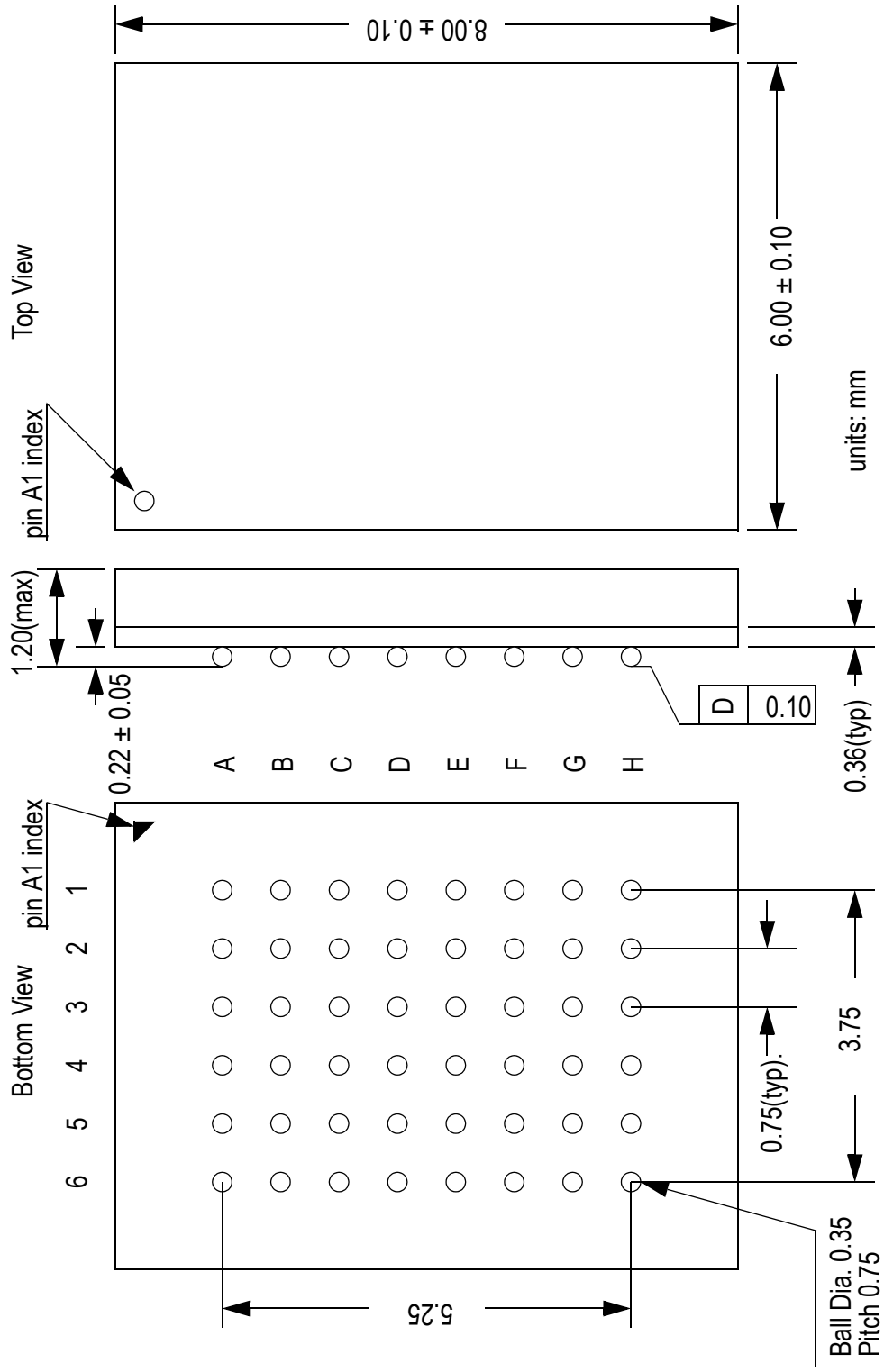
32-Pin TSOP-II, 400mil



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.039	—	0.05	—	—	1.27
A1	0.002	—	0.006	0.01	—	0.15
A2	0.037	0.040	0.045	0.90	1.02	1.14
b	0.012	0.016	0.018	0.30	0.40	0.45
c	0.0047	0.0051	0.0062	0.12	0.13	0.16
D	0.820	0.825	0.830	20.82	20.95	21.08
ZD	—	0.037	—	—	0.95	—
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e	—	0.05	—	—	1.27	—
L	0.017	0.020	0.023	0.40	0.50	0.60
L1	0.024	0.031	0.039	0.60	0.80	1.00
y	0.00	—	0.003	0.00	—	0.76
Q	0^o	—	5^o	0^o	—	5^o

Notes:
1.Dimension D includes mold flash, protrusions or gate burrs.
2. Dimension E does not include interlead flash
3. Controlling dimension: mm

6 mm x 8 mm Fine Pitch BGA



Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS71108ATP-7	400 mil TSOP-II	7 ns	Commercial	
GS71108ATP-8	400 mil TSOP-II	8 ns	Commercial	
GS71108ATP-10	400 mil TSOP-II	10 ns	Commercial	
GS71108ATP-12	400 mil TSOP-II	12 ns	Commercial	
GS71108ATP-7I	400 mil TSOP-II	7 ns	Industrial	
GS71108ATP-8I	400 mil TSOP-II	8 ns	Industrial	
GS71108ATP-10I	400 mil TSOP-II	10 ns	Industrial	
GS71108ATP-12I	400 mil TSOP-II	12 ns	Industrial	
GS71108ASJ-7	300 mil SOJ	7 ns	Commercial	
GS71108ASJ-8	300 mil SOJ	8 ns	Commercial	
GS71108ASJ-10	300 mil SOJ	10 ns	Commercial	
GS71108ASJ-12	300 mil SOJ	12 ns	Commercial	
GS71108ASJ-7I	300 mil SOJ	7 ns	Industrial	
GS71108ASJ-8I	300 mil SOJ	8 ns	Industrial	
GS71108ASJ-10I	300 mil SOJ	10 ns	Industrial	
GS71108ASJ-12I	300 mil SOJ	12 ns	Industrial	
GS71108AJ-7	400 mil SOJ	7 ns	Commercial	
GS71108AJ-8	400 mil SOJ	8 ns	Commercial	
GS71108AJ-10	400 mil SOJ	10 ns	Commercial	
GS71108AJ-12	400 mil SOJ	12 ns	Commercial	
GS71108AJ-7I	400 mil SOJ	7 ns	Industrial	
GS71108AJ-8I	400 mil SOJ	8 ns	Industrial	
GS71108AJ-10I	400 mil SOJ	10 ns	Industrial	
GS71108AJ-12I	400 mil SOJ	12 ns	Industrial	

Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS71108AU-7	6 mm x 8 mm Fine Pitch BGA	7 ns	Commercial	
GS71108AU-8	6 mm x 8 mm Fine Pitch BGA	8 ns	Commercial	
GS71108AU-10	6 mm x 8 mm Fine Pitch BGA	10 ns	Commercial	
GS71108AU-12	6 mm x 8 mm Fine Pitch BGA	12 ns	Commercial	
GS71108AU-7I	6 mm x 8 mm Fine Pitch BGA	7 ns	Industrial	
GS71108AU-8I	6 mm x 8 mm Fine Pitch BGA	8 ns	Industrial	
GS71108AU-10I	6 mm x 8 mm Fine Pitch BGA	10 ns	Industrial	
GS71108AU-12I	6 mm x 8 mm Fine Pitch BGA	12 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS71108ATP-8T

1Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
71108A_r1		• Creation of new datasheet
71108A_r1; 71108A_r1_01	Content	• Added 6 ns speed bin to entire document
71108A_r1_01; 71108A _r1_02	Content	• Updated all power numbers • Changed 6 mm x 10 mm package designator from U to X
71108A_r1_02; 71108A _r1_03	Content	• Updated Recommended Operating Conditions table on page 3 • Updated Power Supply Currents table • Changed FPBGA package from 6 x 10 to 6 x 8 (package U)
71108A_r1_03; 71108A _r1_04	Content	• Removed 6 ns speed bin from entire document • Added 7 ns speed bin to entire document

