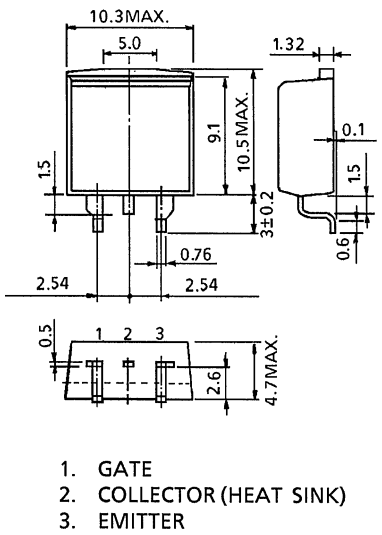
TOSHIBA INSULATED GATE BIPOLAR TRANSISTOR SILICON N−CHANNEL IGBT

GT25G101(SM)

STROBE FLASH APPLICATIONS

- High Input Impedance
- Low Saturation Voltage : $V_{CE\ (sat)}$ = 8V (Max.) (I_C = 170A)
- Enhancement−Mode
- 12V Gate Drive

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2−10S2C

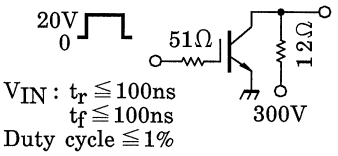
Weight: 1.4g

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

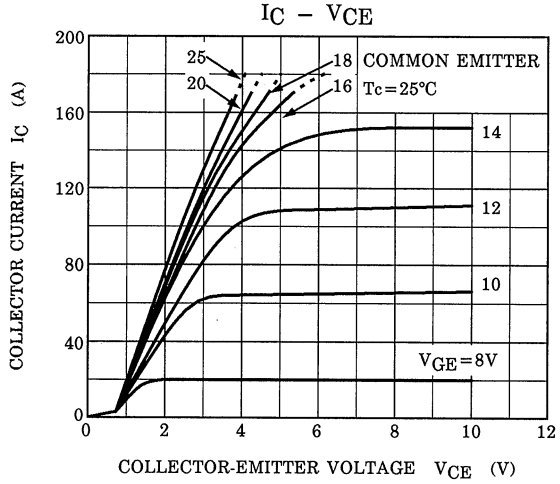
CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector−Emitter Voltage		V_{CES}	400	V
Gate−Emitter Voltage		V_{GES}	±25	V
Collector Current	DC	I_C	25	A
	1ms	I_{CP}	170	
Collector Power Dissipation	Ta = 25°C	P_C	1.3	W
	Tc = 25°C	P_C	75	
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

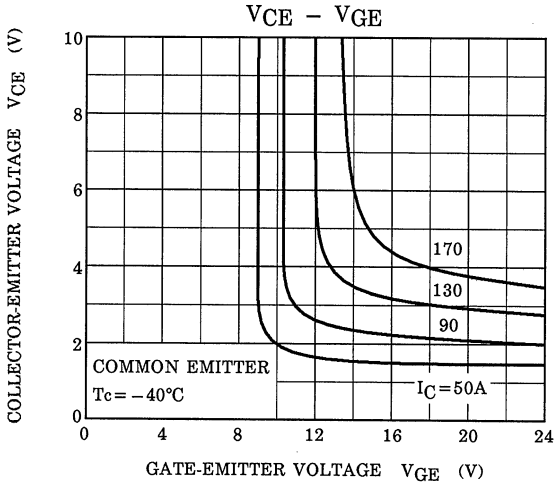
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ±25V, V_{CE} = 0	—	—	±100	nA
Collector Cut−off Current		I_{CES}	V_{CE} = 400V, V_{GE} = 0	—	—	10	μA
Gate−Emitter Cut−off Voltage		$V_{GE\ (OFF)}$	I_C = 1mA, V_{CE} = 5V	4	5	7	V
Collector−Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 170A, V_{GE} = 20V (Pulsed)	—	5	8	V
Input Capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	—	2000	—	pF
Switching Time	Rise Time	t_r		—	0.1	0.5	μs
	Turn−on Time	t_{on}		—	0.15	0.5	
	Fall Time	t_f		—	4.0	6.0	
	Turn−off Time	t_{off}		—	4.5	7.0	
Thermal Resistance		$R_{th\ (j-c)}$	—	—	—	1.66	°C / W

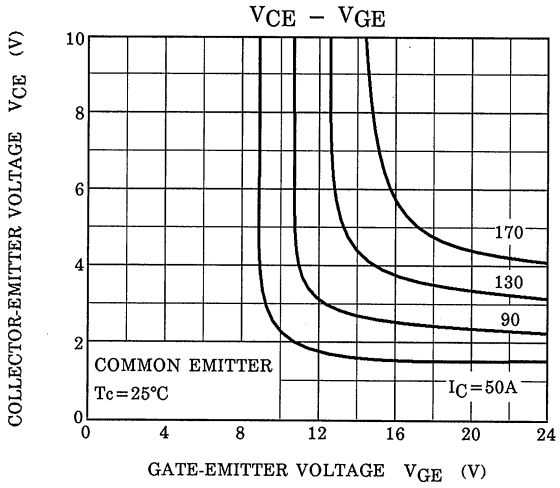
I_C – V_{CE}



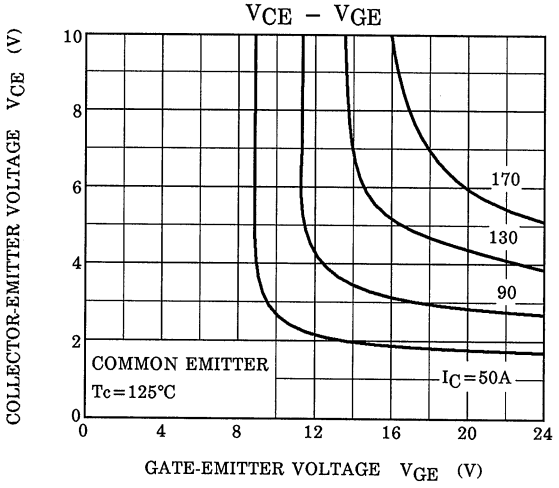
V_{CE} – V_{GE}



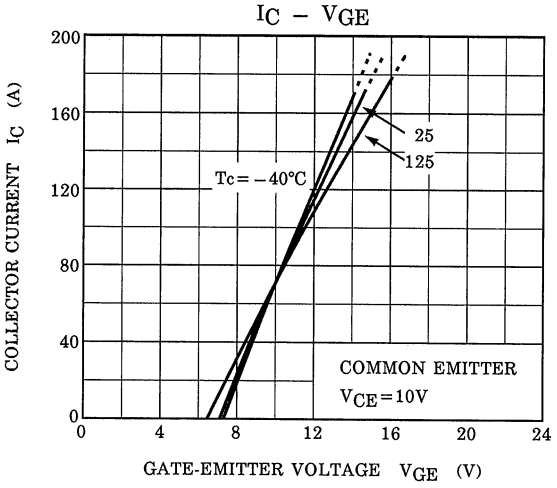
V_{CE} – V_{GE}



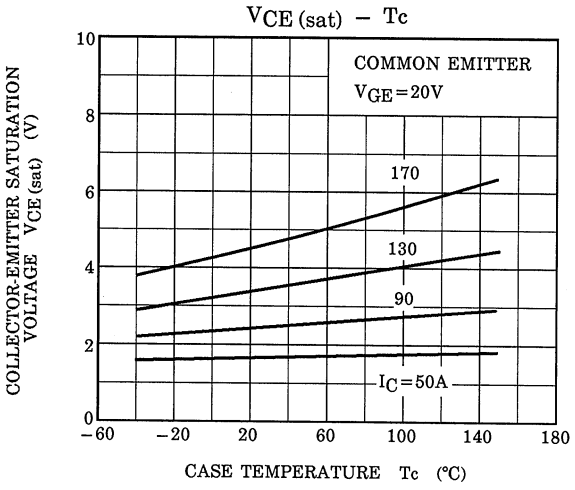
V_{CE} – V_{GE}



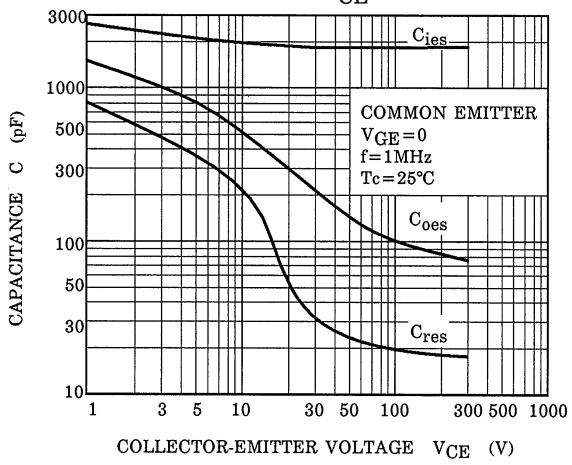
I_C – V_{GE}



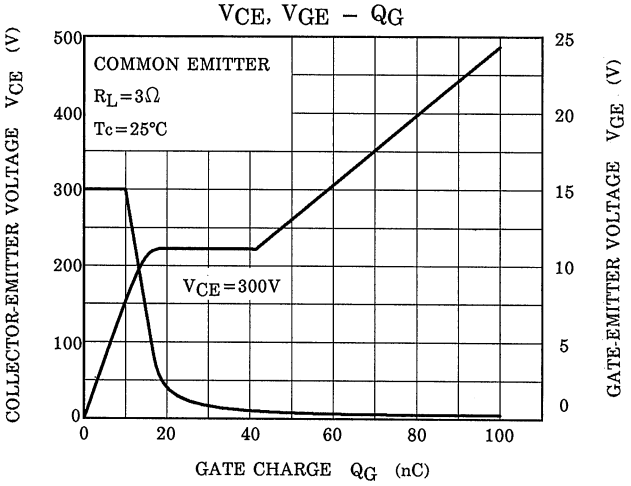
$V_{CE\,(sat)}$ – Tc



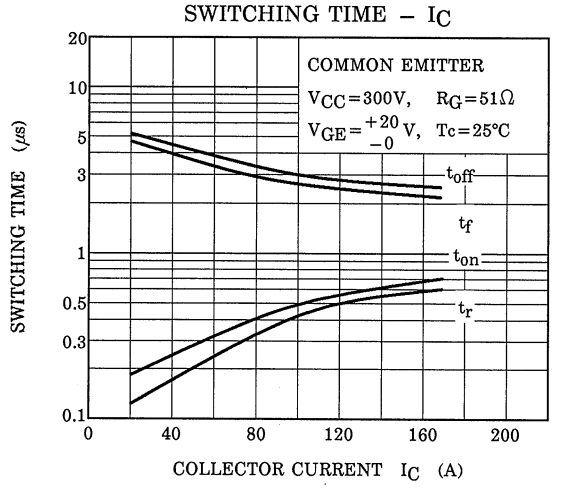
C – V_{CE}



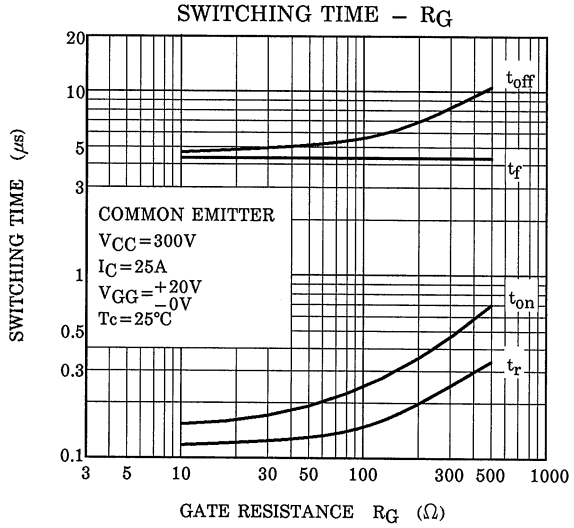
V_{CE}, V_{GE} – Q_G



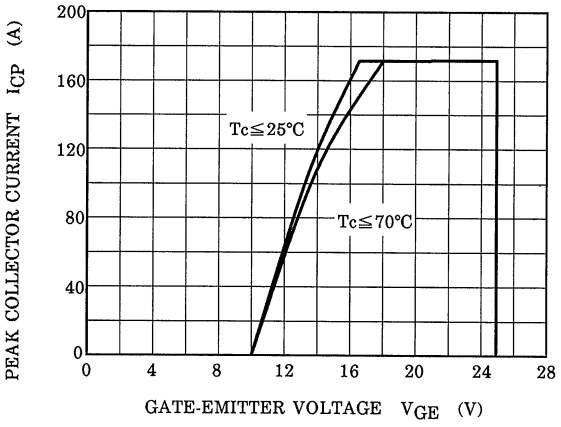
SWITCHING TIME – I_C



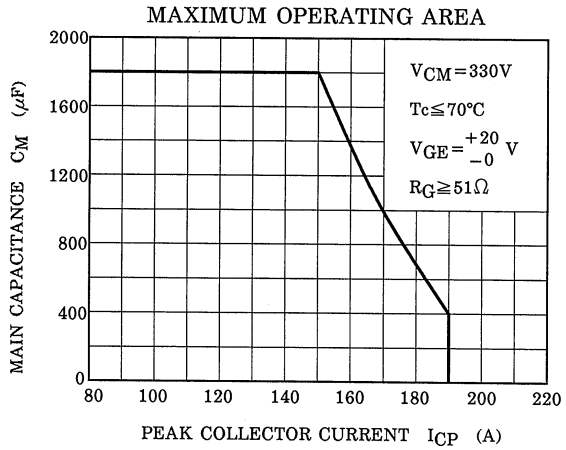
SWITCHING TIME – R_G



MINIMUM GATE DRIVE AREA



MAXIMUM OPERATING AREA



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