

# GTL2003

## 8-bit bidirectional low voltage translator

Rev. 2 — 3 July 2012

Product data sheet

### 1. General description

---

The Gunning Transceiver Logic - Transceiver Voltage Clamps (GTL-TVC) provide high-speed voltage translation with low ON-state resistance and minimal propagation delay. The GTL2003 provides eight NMOS pass transistors (Sn and Dn) with a common gate (GREF) and a reference transistor (SREF and DREF). The device allows bidirectional voltage translations between 0.8 V and 5.0 V without use of a direction pin. Voltage translation below 0.8 V can be achieved when properly biased. For more information, refer to application note [AN11127 \(Ref. 1\)](#).

When the Sn or Dn port is LOW, the clamp is in the ON-state and a low resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (SREF). When the Sn port is HIGH, the Dn port is pulled to  $V_{DD1}$  by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control.

All transistors have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the transistors is symmetrical. Because all transistors in the device are identical, SREF and DREF can be located on any of the other eight matched Sn/Dn transistors, allowing for easier board layout. The translator's transistors provide excellent ESD protection to lower voltage devices and at the same time protect less ESD-resistant devices.

### 2. Features and benefits

---

- 8-bit bidirectional low voltage translator
- Allows voltage level translation between 0.8 V, 0.9 V, 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V buses which allows direct interface with GTL, GTL+, LVTTTL/TTL and 5 V CMOS levels
- Provides bidirectional voltage translation with no direction pin
- Low  $6.5 \Omega$  ON-state resistance ( $R_{on}$ ) between input and output pins (Sn/Dn)
- Supports hot insertion
- No power supply required: will not latch up
- 5 V tolerant inputs
- Low standby current
- Flow-through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Packages offered: TSSOP20, DHVQFN20



### 3. Applications

- Any application that requires bidirectional or unidirectional voltage level translation from any voltage from 0.8 V to 5.0 V to any voltage from 0.8 V to 5.0 V
- The open-drain construction with no direction pin is ideal for bidirectional low voltage (for example, 0.8 V, 0.9 V, 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I<sup>2</sup>C-bus port translation to the normal 3.3 V and/or 5.0 V I<sup>2</sup>C-bus signal levels or GTL/GTL+ translation to LVTTL/TTL signal levels.

### 4. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
GTL2003BQ	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
GTL2003PW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

#### 4.1 Ordering options

Table 2. Ordering options

Type number	Topside mark	Temperature range
GTL2003BQ	2003	-40 °C to +85 °C
GTL2003PW	GTL2003	-40 °C to +85 °C

### 5. Functional diagram

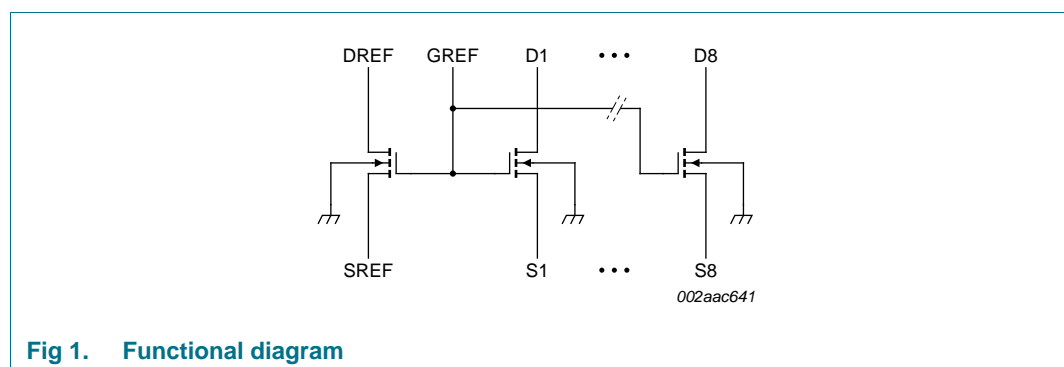


Fig 1. Functional diagram

## 6. Pinning information

### 6.1 Pinning

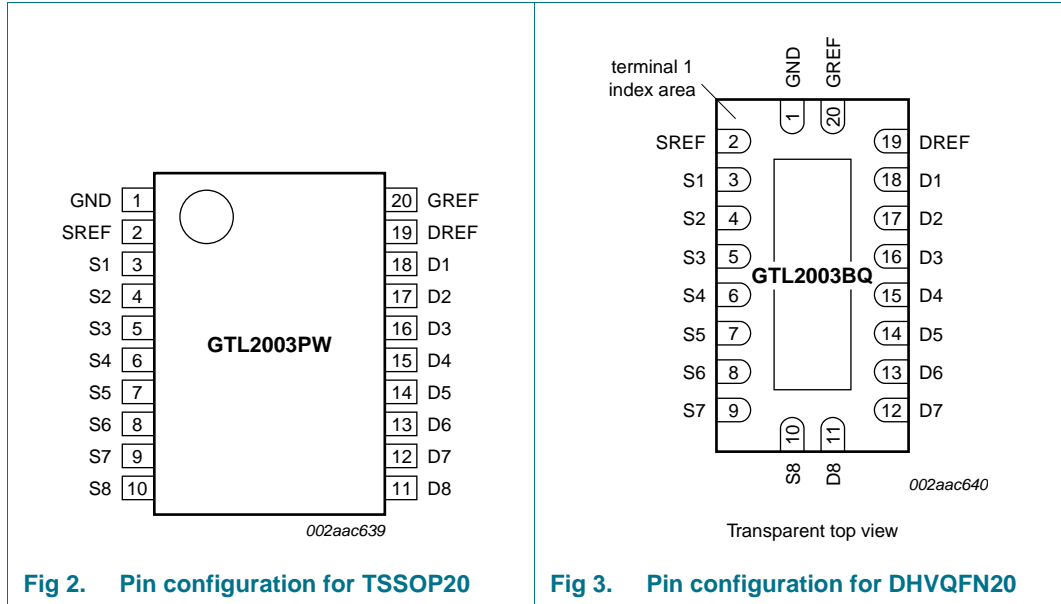


Fig 2. Pin configuration for TSSOP20

Fig 3. Pin configuration for DHVQFN20

### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1 <sup>[1]</sup>	ground (0 V)
SREF	2	source of reference transistor
S1 to S8	3, 4, 5, 6, 7, 8, 9, 10	Port S1 to Port S8
D1 to D8	18, 17, 16, 15, 14, 13, 12, 11	Port D1 to Port D8
DREF	19	drain of reference transistor
GREF	20	gate of reference transistor

[1] DHVQFN20 package die supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 7. Functional description

Refer also to [Figure 1 “Functional diagram”](#).

### 7.1 Function selection

**Table 4. Function selection, HIGH-to-LOW translation**

Assumes Dn is at the higher voltage level.

H = HIGH voltage level; L = LOW voltage level; X = Don't care

GREF <sup>[1]</sup>	DREF	SREF	Input Dn	Output Sn	Transistor
H	H	0 V	X	X	off
H	H	$V_T$ <sup>[2]</sup>	H	$V_T$ <sup>[2][3]</sup>	on
H	H	$V_T$ <sup>[2]</sup>	L	L <sup>[4]</sup>	on
L	L	$0\text{ V} - V_T$ <sup>[2]</sup>	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2]  $V_T$  is equal to the SREF voltage.

[3] Sn is not pulled up or pulled down.

[4] Sn follows the Dn input LOW.

**Table 5. Function selection, LOW-to-HIGH translation**

Assumes Dn is at the higher voltage level.

H = HIGH voltage level; L = LOW voltage level; X = Don't care

GREF <sup>[1]</sup>	DREF	SREF	Input Sn	Output Dn	Transistor
H	H	0 V	X	X	off
H	H	$V_T$ <sup>[2]</sup>	$V_T$ <sup>[2]</sup>	H <sup>[3]</sup>	nearly off
H	H	$V_T$ <sup>[2]</sup>	L	L <sup>[4]</sup>	on
L	L	$0\text{ V} - V_T$ <sup>[2]</sup>	X	X	off

[1] GREF should be at least 1.5 V higher than SREF for best translator operation.

[2]  $V_T$  is equal to the SREF voltage.

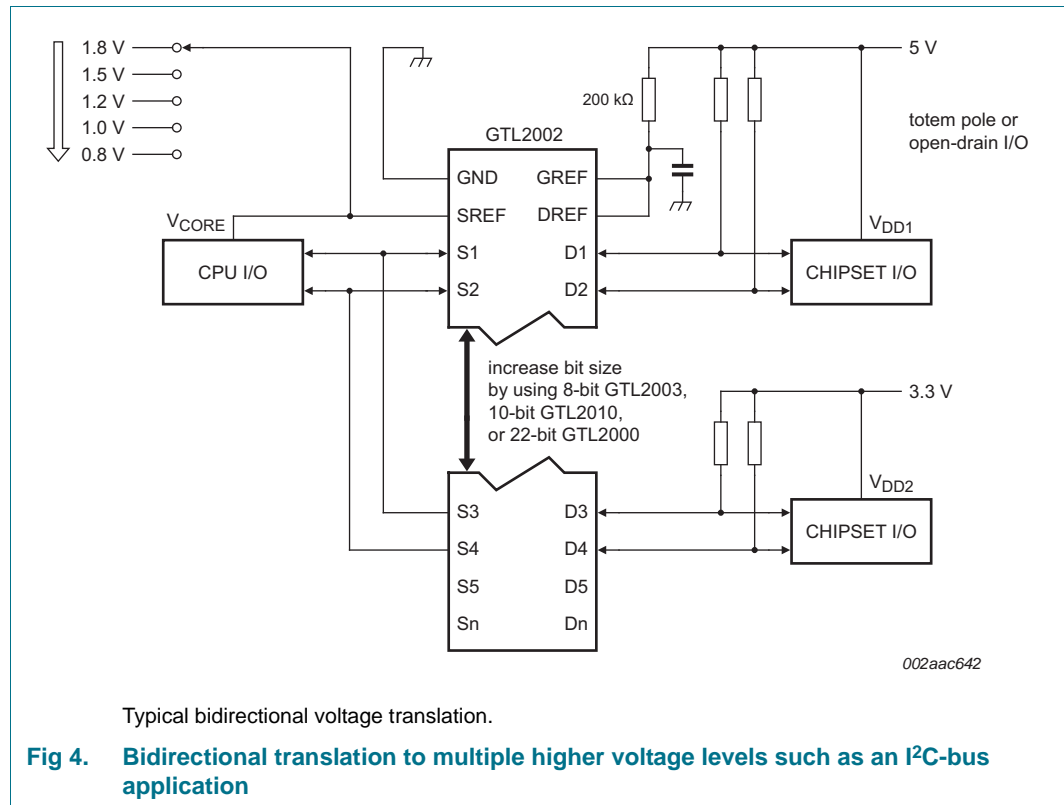
[3] Dn is pulled up to  $V_{DD1}$  through an external resistor.

[4] Dn follows the Sn input LOW.

## 8. Application design-in information

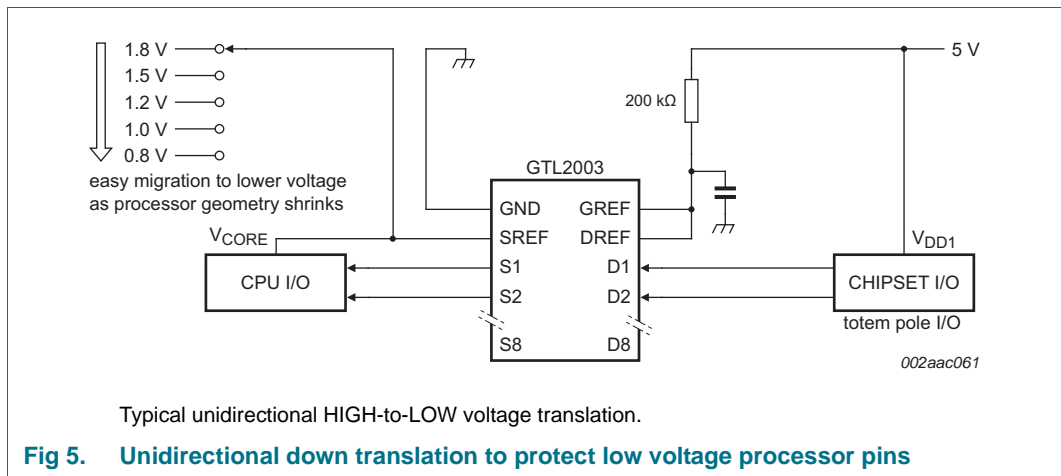
### 8.1 Bidirectional translation

For the bidirectional clamping configuration, higher voltage to lower voltage or lower voltage to higher voltage, the GREF input must be connected to DREF and both pins pulled to HIGH side  $V_{DD1}$  through a pull-up resistor (typically 200 k $\Omega$ ). A filter capacitor on DREF is recommended. The processor output can be totem pole or open-drain (pull-up resistors may be required) and the chip set output can be totem pole or open-drain (pull-up resistors are required to pull the Dn outputs to  $V_{DD1}$ ). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed. The opposite side of the reference transistor (SREF) is connected to the processor core power supply voltage. When DREF is connected through a 200 k $\Omega$  resistor to a 3.3 V to 5.5 V  $V_{DD1}$  supply and SREF can be set between 0.8 V to ( $V_{DD1} - 1.5$  V), without the need for pull-up resistors on the low voltage side. The output of each Sn will have a maximum output voltage equal to SREF and the output of each Dn has a maximum output voltage equal to  $V_{DD1}$ . It is recommended that  $V_{DD1}$  be greater than 1.5 V for proper operation.



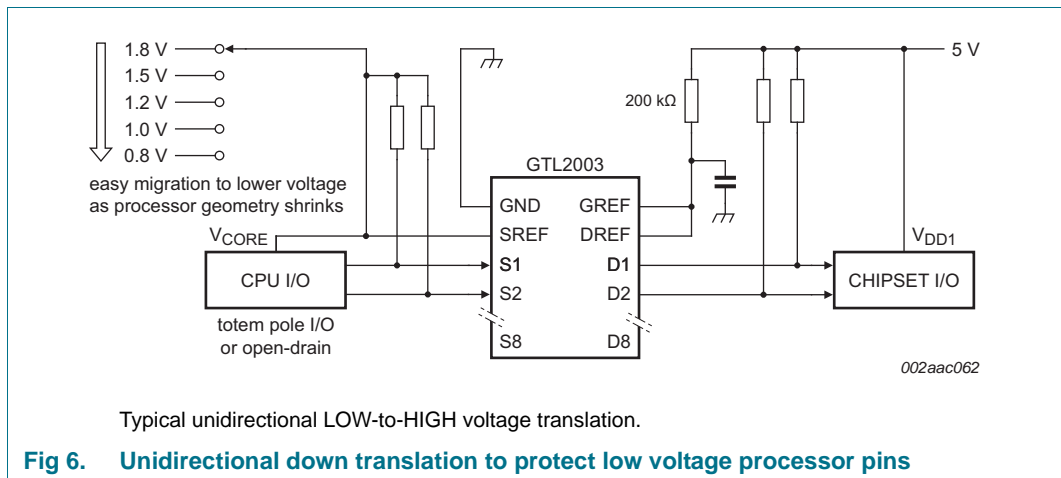
### 8.2 Unidirectional down translation

For unidirectional clamping, higher voltage to lower voltage, the GREF input must be connected to DREF and both pins pulled to the higher side  $V_{DD1}$  through a pull-up resistor (typically 200 k $\Omega$ ). A filter capacitor on DREF is recommended. Pull-up resistors are required if the chip set I/O are open-drain. The opposite side of the reference transistor (SREF) is connected to the processor core supply voltage. When DREF is connected through a 200 k $\Omega$  resistor to a 3.3 V to 5.5 V  $V_{DD1}$  supply and SREF can be set between 0.8 V to ( $V_{DD1} - 1.5$  V), without the need for pull-up resistors on the low voltage side. The output of each  $S_n$  will have a maximum output voltage equal to SREF. It is recommended that  $V_{DD1}$  be greater than 1.5 V for proper operation.



### 8.3 Unidirectional up translation

For unidirectional up translation, lower voltage to higher voltage, the reference transistor is connected the same as for a down translation. A pull-up resistor is required on the higher voltage side ( $D_n$  or  $S_n$ ) to get the full HIGH level, since the GTL-TVC device will only pass the reference source (SREF) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open-drain.



### 8.4 Sizing pull-up resistor

The pull-up resistor value needs to limit the current through the pass transistor when it is in the 'on' state to about 15 mA. This will guarantee a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage will also be higher in the 'on' state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as shown in [Equation 1](#):

$$resistor\ value\ (\Omega) = \frac{pull\text{-}up\ voltage\ (V) - 0.35\ V}{0.015\ A} \tag{1}$$

When using open-drain devices, it is always required to use pull-up resistors at D-side, and they must be sized so as not to overload the output. If  $V_{DD1} - V_{SREF} < 1.5\ V$ , then pull-up resistor is required on S-side to pull up the Sn outputs to  $V_{SREF}$ . It is important to note that if pull-up resistors are required on both the S-side and D-side, the equivalent pull-up resistor value becomes the parallel combination of the two resistors when pass transistor is ON. If  $V_{DD1} - V_{SREF} \geq 1.5\ V$ , then pull-up resistors on the S-side are not required.

[Table 6](#) summarizes resistor values for various reference voltages and currents at 15 mA and also at 10 mA and 3 mA for  $V_{DD1} - V_{SREF} \geq 1.5\ V$ . The resistor value shown in the +10 % column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL-TVC device at 0.175 V, although the 15 mA only applies to current flowing through the GTL-TVC device. See application note AN10145, "Bidirectional low voltage translators" ([Ref. 2](#)) for more information.

**Table 6. Pull-up resistor values**

Calculated for  $V_{OL} = 0.35\ V$ . Assumes output driver  $V_{OL} = 0.175\ V$  at stated current.

Pull-up resistor value ( $\Omega$ )						
Voltage	15 mA		10 mA		3 mA	
	Nominal	+ 10 % <sup>[1]</sup>	Nominal	+ 10 % <sup>[1]</sup>	Nominal	+ 10 % <sup>[1]</sup>
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312
1.1 V	50	55	75	83	250	275
1.0 V	44	48	65	72	217	239
0.95 V	40	44	60	66	200	220
0.9 V	37	41	55	61	183	201
0.85 V	34	37	50	55	167	184
0.8 V	30	33	45	50	150	165

[1] + 10 % to compensate for  $V_{DD}$  range and resistor tolerance.

## 9. Limiting values

**Table 7. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>SREF</sub>	voltage on pin SREF		-0.5 <sup>[2]</sup>	+7.0	V
V <sub>DREF</sub>	voltage on pin DREF		-0.5 <sup>[2]</sup>	+7.0	V
V <sub>GREF</sub>	voltage on pin GREF		-0.5 <sup>[2]</sup>	+7.0	V
V <sub>Sn</sub>	voltage on port Sn		-0.5 <sup>[2]</sup>	+7.0	V
V <sub>Dn</sub>	voltage on port Dn		-0.5 <sup>[2]</sup>	+7.0	V
I <sub>IK</sub>	input clamping current	SREF, DREF, GREF; V <sub>I</sub> < 0 V	-	-50	mA
		port Sn; V <sub>I</sub> < 0 V	-	-50	mA
		port Dn; V <sub>I</sub> < 0 V	-	-50	mA
I <sub>ch</sub>	channel current (DC)	channel in ON-state	-	±128	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## 10. Recommended operating conditions

**Table 8. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>I/O</sub>	voltage on an input/output pin	Sn, Dn	0	-	5.5	V
V <sub>Sn</sub>	voltage on port Sn	Sn	0	-	5.5	V
V <sub>SREF</sub>	voltage on pin SREF		<sup>[1]</sup> 0	-	5.5	V
V <sub>DREF</sub>	voltage on pin DREF		0	-	5.5	V
V <sub>GREF</sub>	voltage on pin GREF		0	-	5.5	V
I <sub>sw(pass)</sub>	pass switch current		-	-	64	mA
T <sub>amb</sub>	ambient temperature	operating in free-air	-40	-	+85	°C

[1] V<sub>SREF</sub> ≤ V<sub>DREF</sub> - 1.5 V for best results in level shifting applications.



## 11. Static characteristics

**Table 9. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{OL}$	LOW-level output voltage	$V_{DD} = 3.0\text{ V}$ ; $V_{SREF} = 1.365\text{ V}$ ; $V_{Sn}$ or $V_{Dn} = 0.175\text{ V}$ ; $I_{IK} = 15.2\text{ mA}$	-	260	350	mV
$V_{IK}$	input clamping voltage	$I_I = -18\text{ mA}$ ; $V_{GREF} = 0\text{ V}$	-	-	-1.2	V
$I_{LI(G)}$	gate input leakage current	$V_I = 5\text{ V}$ ; $V_{GREF} = 0\text{ V}$	-	-	5	$\mu\text{A}$
$C_{ig}$	input capacitance at gate	GREF; $V_I = 3\text{ V}$ or $0\text{ V}$	-	56	-	pF
$C_{io(off)}$	off-state input/output capacitance	$V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{GREF} = 0\text{ V}$	-	7.4	-	pF
$C_{io(on)}$	on-state input/output capacitance	$V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{GREF} = 3\text{ V}$	-	18.6	-	pF
$R_{on}$	ON-state resistance	$V_{Sn} = 0\text{ V}$ ; $I_O = 64\text{ mA}$	[2]			
		$V_{GREF} = 4.5\text{ V}$	-	3.5	5	$\Omega$
		$V_{GREF} = 3\text{ V}$	-	4.4	7	$\Omega$
		$V_{GREF} = 2.3\text{ V}$	-	5.5	9	$\Omega$
		$V_{GREF} = 1.5\text{ V}$	-	67	105	$\Omega$
		$V_{Sn} = 0\text{ V}$ ; $I_O = 30\text{ mA}$ ; $V_{GREF} = 1.5\text{ V}$	[2]	9	15	$\Omega$
		$V_{Sn} = 2.4\text{ V}$ ; $I_O = 15\text{ mA}$ ; $V_{GREF} = 4.5\text{ V}$	[2]	7	10	$\Omega$
		$V_{Sn} = 2.4\text{ V}$ ; $I_O = 15\text{ mA}$ ; $V_{GREF} = 3\text{ V}$	[2]	58	80	$\Omega$
		$V_{Sn} = 1.7\text{ V}$ ; $I_O = 15\text{ mA}$ ; $V_{GREF} = 2.3\text{ V}$	[2]	50	70	$\Omega$

[1] All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

## 12. Dynamic characteristics

### 12.1 Dynamic characteristics for translator-type application

**Table 10. Dynamic characteristics**

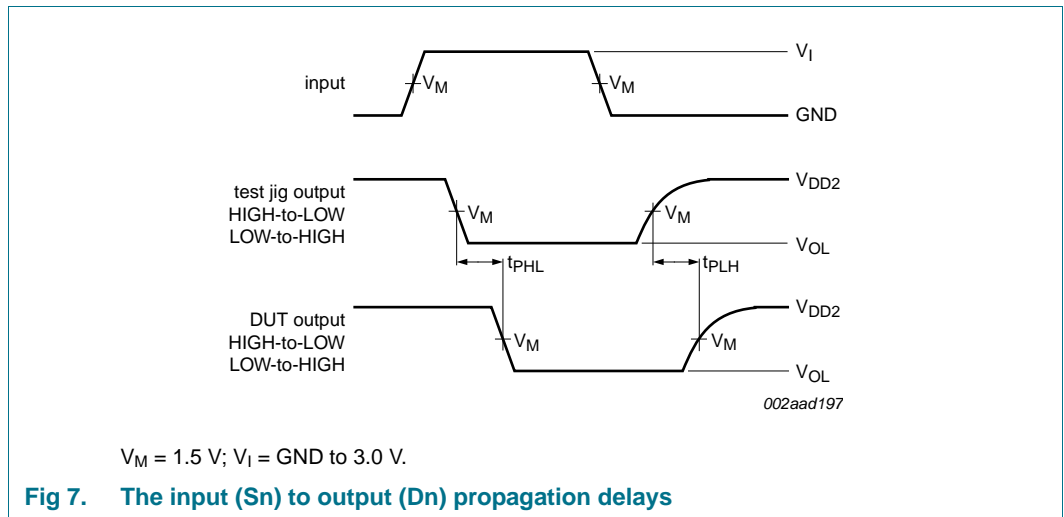
$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{ref} = 1.365\text{ V}$  to  $1.635\text{ V}$ ;  $V_{DD1} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  $V_{DD2} = 2.36\text{ V}$  to  $2.64\text{ V}$ ;  $GND = 0\text{ V}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ ; unless otherwise specified. Refer to [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$t_{PLH}$	LOW to HIGH propagation delay	Sn to Dn; Dn to Sn	<a href="#">[2]</a> <a href="#">[3]</a> 0.5	1.5	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	Sn to Dn; Dn to Sn	<a href="#">[2]</a> <a href="#">[3]</a> 0.5	1.5	5.5	ns

[1] All typical values are measured at  $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 2.5\text{ V}$ ,  $V_{ref} = 1.5\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Propagation delay is measured using [Figure 9](#) and is a difference measurement. It is not production tested and is guaranteed by ON-state resistance.

[3]  $C_{io(on)}$  maximum of 30 pF and  $C_{io(off)}$  maximum of 15 pF is guaranteed by design.



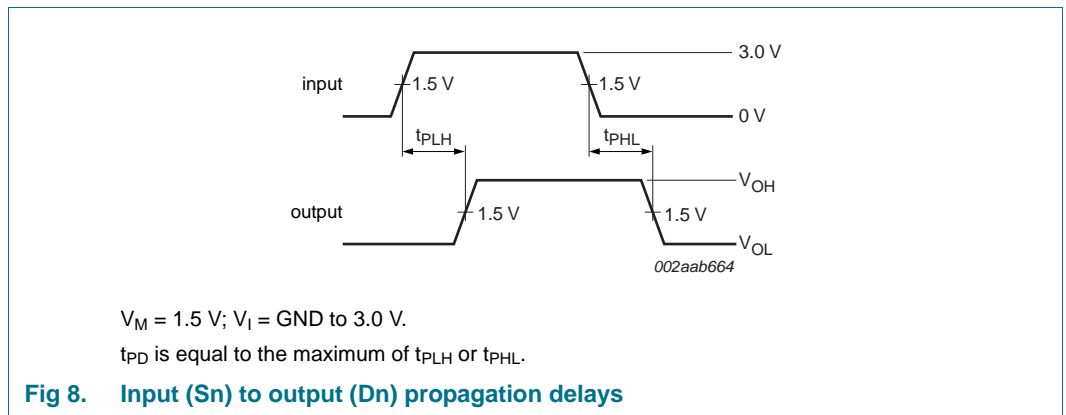
12.2 Dynamic characteristics for CBT-type application

Table 11. Dynamic characteristics

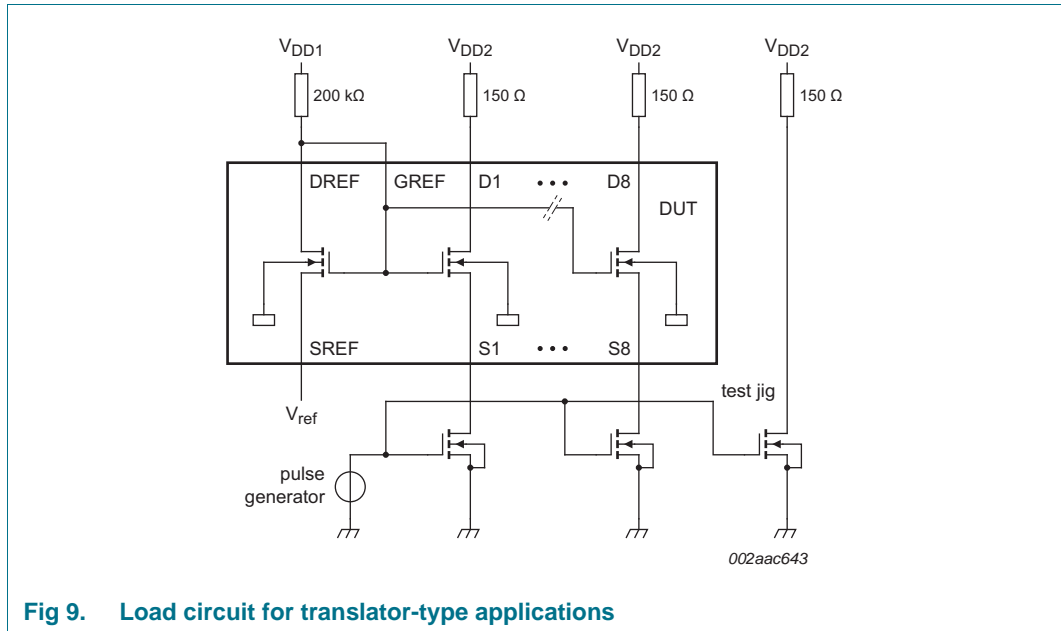
$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{GREF} = 5\text{ V} \pm 0.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ; unless otherwise specified. Refer to [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PD}$	propagation delay	[1]	-	-	250	ps

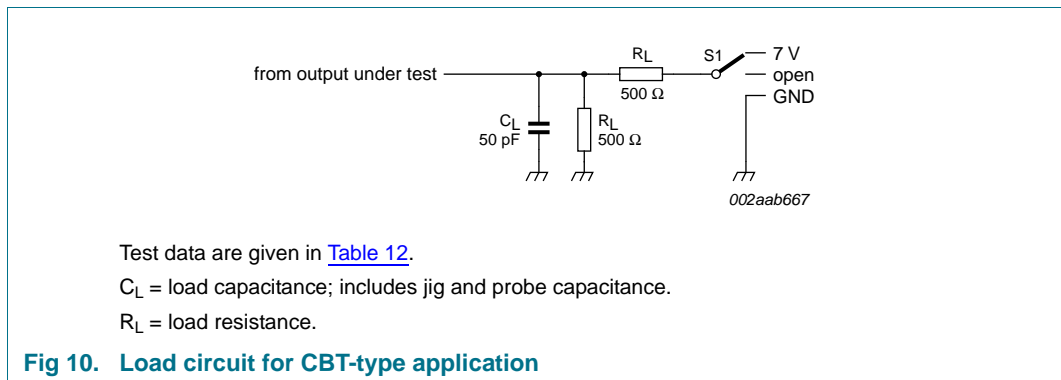
[1] This parameter is warranted by the ON-state resistance, but is not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).



**13. Test information**



**Fig 9. Load circuit for translator-type applications**



**Fig 10. Load circuit for CBT-type application**

**Table 12. Test data**

Test	Load		Switch
	$C_L$	$R_L$	
$t_{PD}$	50 pF	500 Ω	open
$t_{PLZ}, t_{PZL}$	50 pF	500 Ω	7 V
$t_{PHZ}, t_{PZH}$	50 pF	500 Ω	open

14. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

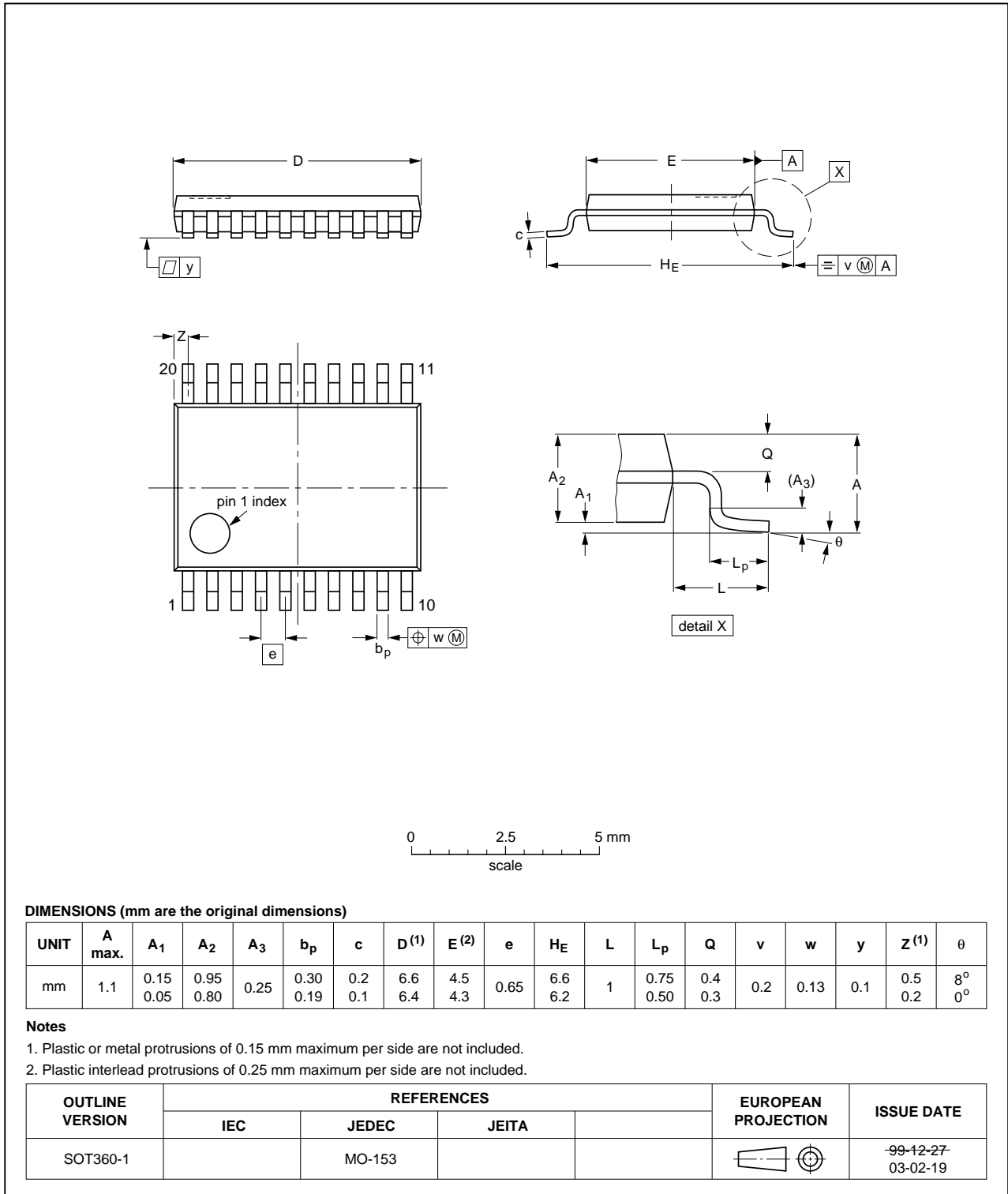


Fig 11. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

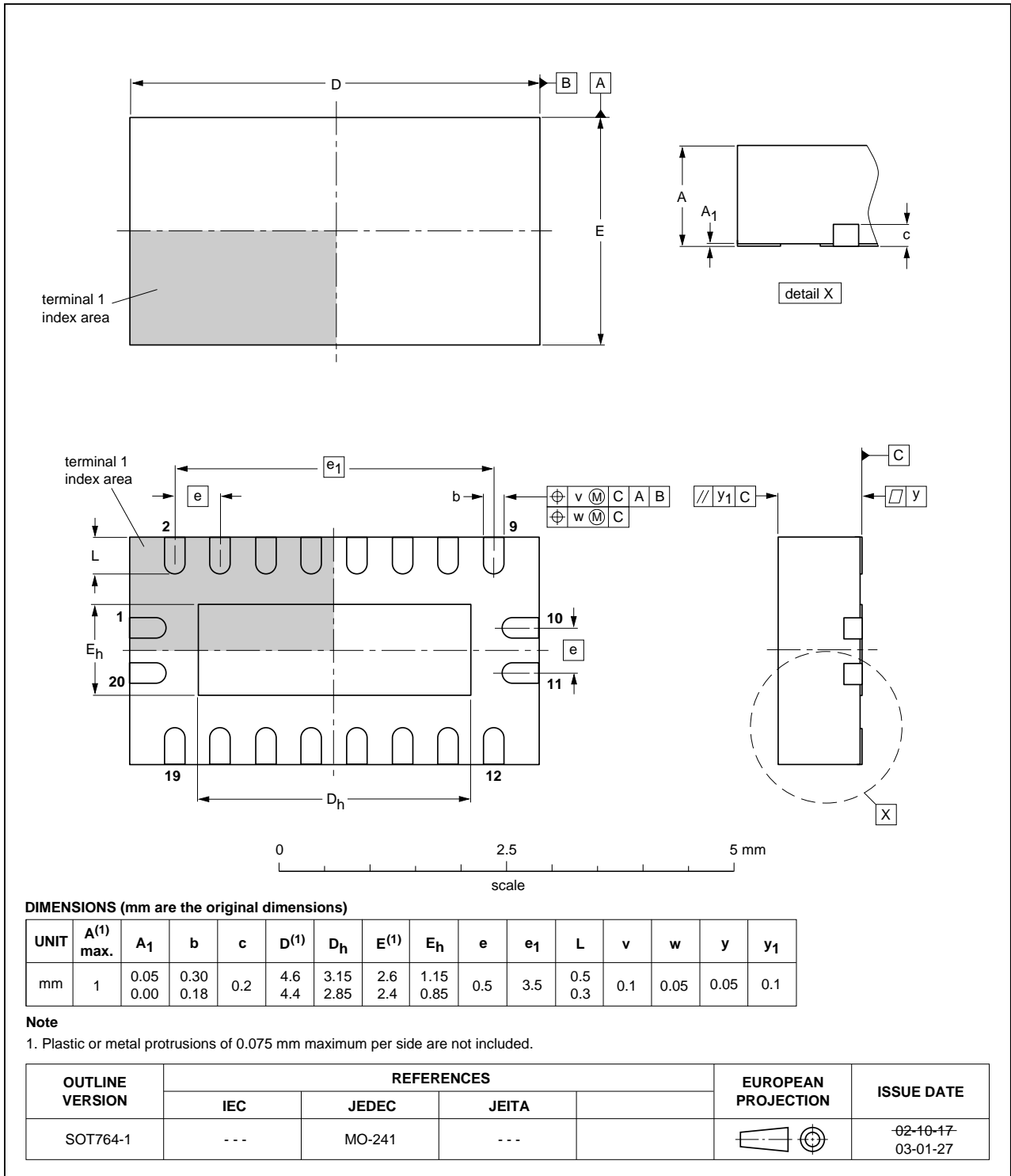


Fig 12. Package outline SOT764-1 (DHVQFN20)

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

**15.4 Reflow soldering**

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 13](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#) and [14](#)

**Table 13. SnPb eutectic process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

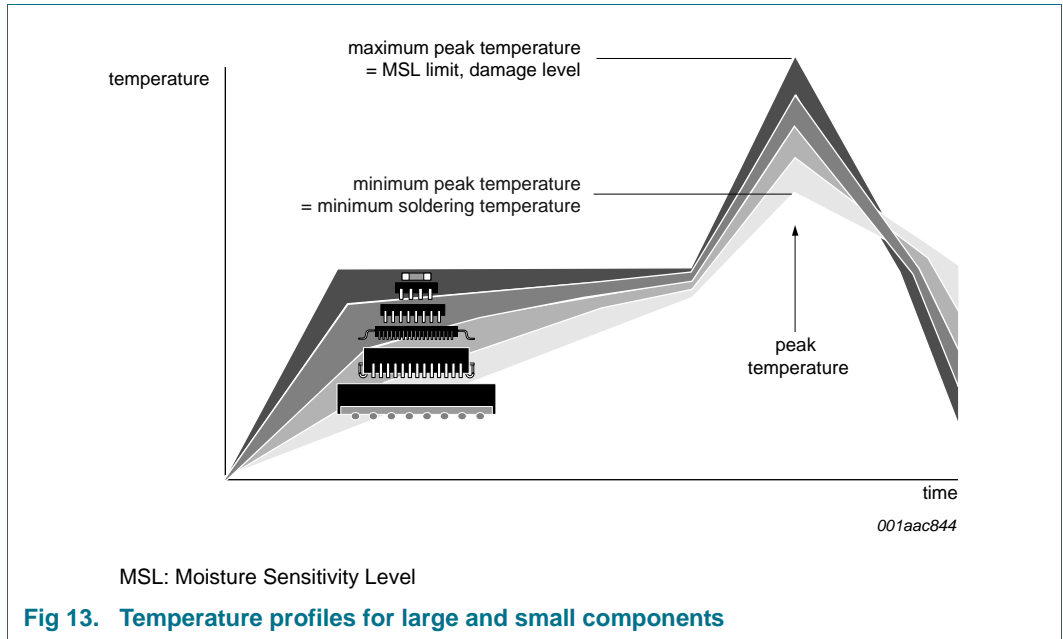
**Table 14. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 13](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

### 16. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP20 package

SOT360-1

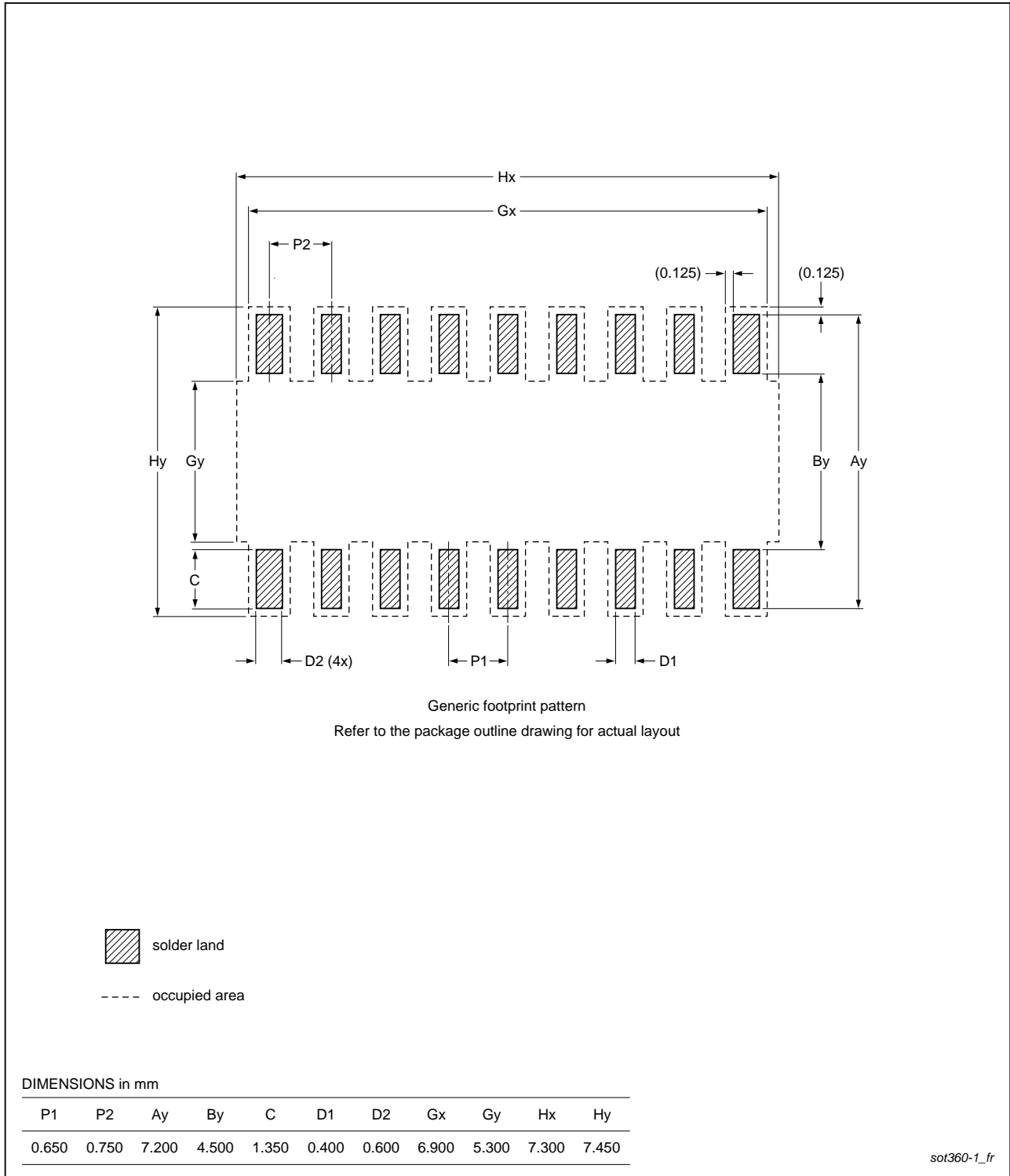


Fig 14. PCB footprint for SOT360-1 (TSSOP20); reflow soldering

Footprint information for reflow soldering of DHVQFN20 package

SOT764-1

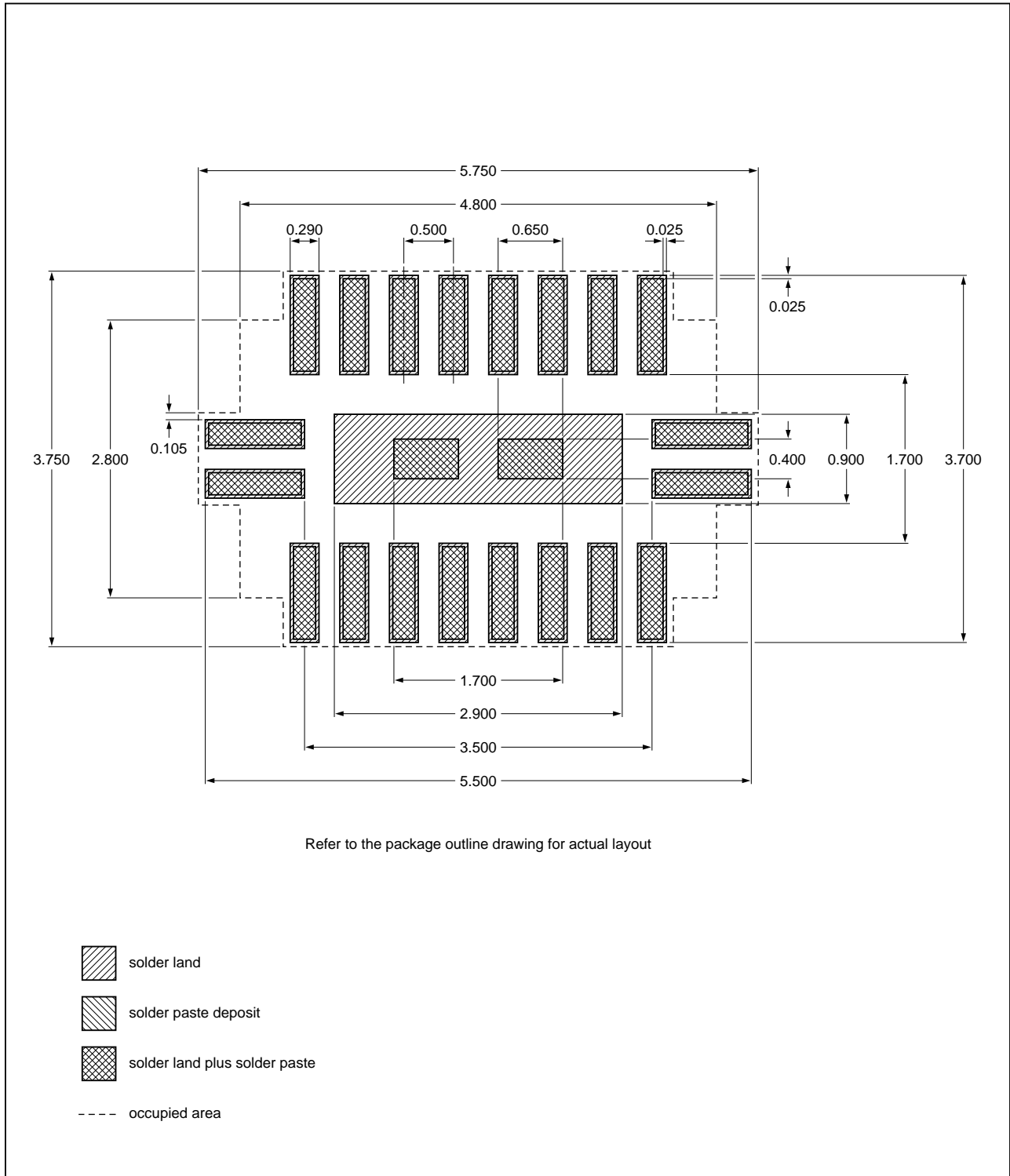


Fig 15. PCB footprint for SOT764-1 (TSSOP20); reflow soldering

## 17. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
LVTTL	Low Voltage Transistor-Transistor Logic
NMOS	Negative-channel Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic
TVC	Transceiver Voltage Clamps

## 18. References

- [1] AN11127, “Bidirectional voltage translators NVT2001/02/03/04/06/08/10, PCA9306, GTL2000/02/03/10” — application note; NXP Semiconductors; [www.nxp.com/documents/application\\_note/AN11127.pdf](http://www.nxp.com/documents/application_note/AN11127.pdf)
- [2] AN10145, “Bidirectional low voltage translators” — application note; NXP Semiconductors; [www.nxp.com/documents/application\\_note/AN10145.pdf](http://www.nxp.com/documents/application_note/AN10145.pdf)

## 19. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2003 v.2	20120703	Product data sheet	-	GTL2003 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1 “General description”</a>: <ul style="list-style-type: none"> <li>– first paragraph, third sentence changed from “between 1.0 V and 5.0 V” to “between 0.8 V and 5.0 V”</li> <li>– first paragraph: added (new) fourth sentence.</li> <li>– second paragraph, third sentence: changed from “V<sub>CC</sub>” to “V<sub>DD1</sub>”</li> </ul> </li> <li>• <a href="#">Section 2 “Features and benefits”</a>: <ul style="list-style-type: none"> <li>– second bullet: added “0.8 V, 0.9 V”</li> <li>– tenth bullet: deleted phrase “200 V MM per JESD22-A115”</li> </ul> </li> <li>• <a href="#">Section 3 “Applications”</a>: <ul style="list-style-type: none"> <li>– first bullet: changed from “1.0 V” to “0.8 V” (two places)</li> <li>– second bullet: added “0.8 V, 0.9 V”</li> </ul> </li> <li>• <a href="#">Table 5 “Function selection, LOW-to-HIGH translation”</a>, <a href="#">Table note [3]</a>: changed from “V<sub>CC</sub>” to “V<sub>DD1</sub>”</li> <li>• <a href="#">Section 8.1 “Bidirectional translation”</a>: <ul style="list-style-type: none"> <li>– first sentence: changed from “V<sub>CC</sub>” to “V<sub>DD1</sub>”</li> <li>– third sentence: changed from “V<sub>CC</sub>” to “V<sub>DD1</sub>”</li> <li>– seventh sentence re-written</li> <li>– eighth sentence re-written</li> <li>– added (new) ninth sentence</li> <li>– <a href="#">Figure 4 “Bidirectional translation to multiple higher voltage levels such as an I<sup>2</sup>C-bus application”</a> updated</li> </ul> </li> <li>• <a href="#">Section 8.2 “Unidirectional down translation”</a>: <ul style="list-style-type: none"> <li>– first sentence: changed from “V<sub>CC</sub>” to “V<sub>DD1</sub>”</li> <li>– fifth sentence re-written (split into fifth and sixth sentences)</li> <li>– added (new) seventh sentence</li> <li>– <a href="#">Figure 5 “Unidirectional down translation to protect low voltage processor pins”</a> updated</li> </ul> </li> <li>• <a href="#">Figure 6 “Unidirectional down translation to protect low voltage processor pins”</a> updated</li> <li>• <a href="#">Section 8.4 “Sizing pull-up resistor”</a>: <ul style="list-style-type: none"> <li>– added (new) second paragraph</li> <li>– third paragraph, first sentence: appended “for V<sub>DD1</sub> – V<sub>SREF</sub> ≥ 1.5 V”</li> <li>– <a href="#">Table 6 “Pull-up resistor values”</a>: added six rows, 1.1 V through 0.8 V</li> </ul> </li> <li>• <a href="#">Table 8 “Recommended operating conditions”</a>: added row V<sub>Sn</sub></li> <li>• <a href="#">Table 9 “Static characteristics”</a>: <ul style="list-style-type: none"> <li>– Conditions for R<sub>on</sub>: changed from “V<sub>I</sub>” to “V<sub>Sn</sub>”</li> </ul> </li> <li>• <a href="#">Figure 9 “Load circuit for translator-type applications”</a>: corrected resistors’ values from “150 kΩ” to “150 Ω” (3 places)</li> <li>• Added <a href="#">Section 16 “Soldering: PCB footprints”</a></li> <li>• Added <a href="#">Section 18 “References”</a></li> </ul>			
GTL2003_1	20070727	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 20.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 20.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 21. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 22. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>
4.1	Ordering options . . . . .	2
<b>5</b>	<b>Functional diagram</b> . . . . .	<b>2</b>
<b>6</b>	<b>Pinning information</b> . . . . .	<b>3</b>
6.1	Pinning . . . . .	3
6.2	Pin description . . . . .	3
<b>7</b>	<b>Functional description</b> . . . . .	<b>4</b>
7.1	Function selection . . . . .	4
<b>8</b>	<b>Application design-in information</b> . . . . .	<b>5</b>
8.1	Bidirectional translation . . . . .	5
8.2	Unidirectional down translation . . . . .	6
8.3	Unidirectional up translation . . . . .	6
8.4	Sizing pull-up resistor . . . . .	7
<b>9</b>	<b>Limiting values</b> . . . . .	<b>8</b>
<b>10</b>	<b>Recommended operating conditions</b> . . . . .	<b>8</b>
<b>11</b>	<b>Static characteristics</b> . . . . .	<b>9</b>
<b>12</b>	<b>Dynamic characteristics</b> . . . . .	<b>10</b>
12.1	Dynamic characteristics for translator-type application . . . . .	10
12.2	Dynamic characteristics for CBT-type application . . . . .	11
<b>13</b>	<b>Test information</b> . . . . .	<b>12</b>
<b>14</b>	<b>Package outline</b> . . . . .	<b>13</b>
<b>15</b>	<b>Soldering of SMD packages</b> . . . . .	<b>15</b>
15.1	Introduction to soldering . . . . .	15
15.2	Wave and reflow soldering . . . . .	15
15.3	Wave soldering . . . . .	15
15.4	Reflow soldering . . . . .	16
<b>16</b>	<b>Soldering: PCB footprints</b> . . . . .	<b>18</b>
<b>17</b>	<b>Abbreviations</b> . . . . .	<b>20</b>
<b>18</b>	<b>References</b> . . . . .	<b>20</b>
<b>19</b>	<b>Revision history</b> . . . . .	<b>21</b>
<b>20</b>	<b>Legal information</b> . . . . .	<b>22</b>
20.1	Data sheet status . . . . .	22
20.2	Definitions . . . . .	22
20.3	Disclaimers . . . . .	22
20.4	Trademarks . . . . .	23
<b>21</b>	<b>Contact information</b> . . . . .	<b>23</b>
<b>22</b>	<b>Contents</b> . . . . .	<b>24</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 3 July 2012

Document identifier: GTL2003