HA12062AMP

Data Strobe IC for R-DAT

The HA12062AMP is a data strobe IC developed for R-DAT (rotary head digital audio tape recorder).
It incorporates a PLL clock generator and automatic strobe point control (ASPC) circuit on one chip, and has the following features and functions.

HA12062AMP

(MP-28)

Functions

- Data strobe
- Clock generation
- Automatic strobe point correction

Features

- 5 V single power supply voltage
- Data discrimination between "0" and "1" by playback signal
- Generation of stable clock signal by PLL
- Automatic correction of strobe point around the eye pattern
- Interface with CMOS LSI is possible due to CMOS level output.

Ordering Information

Type No.	Package
HA12062AMP	MP-28

Block Diagram

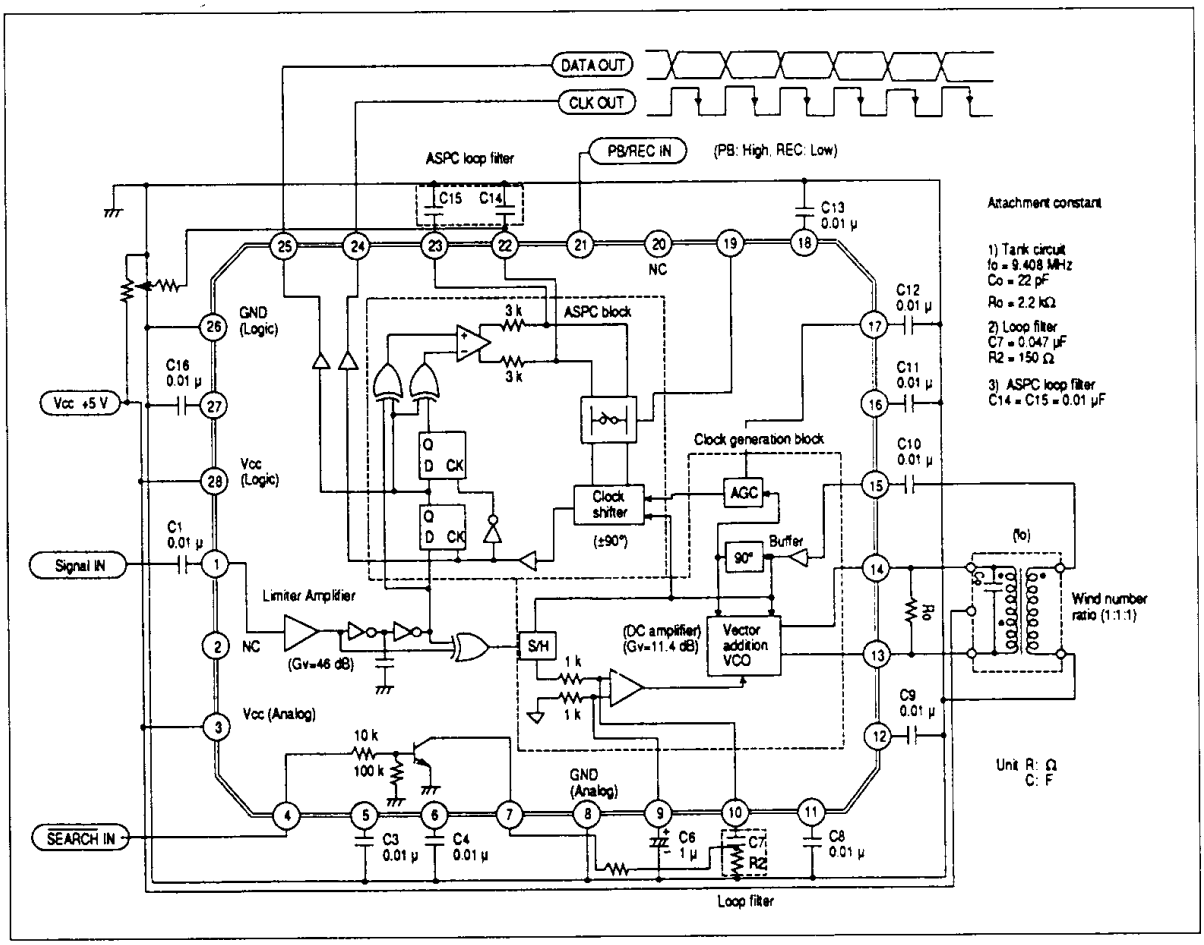


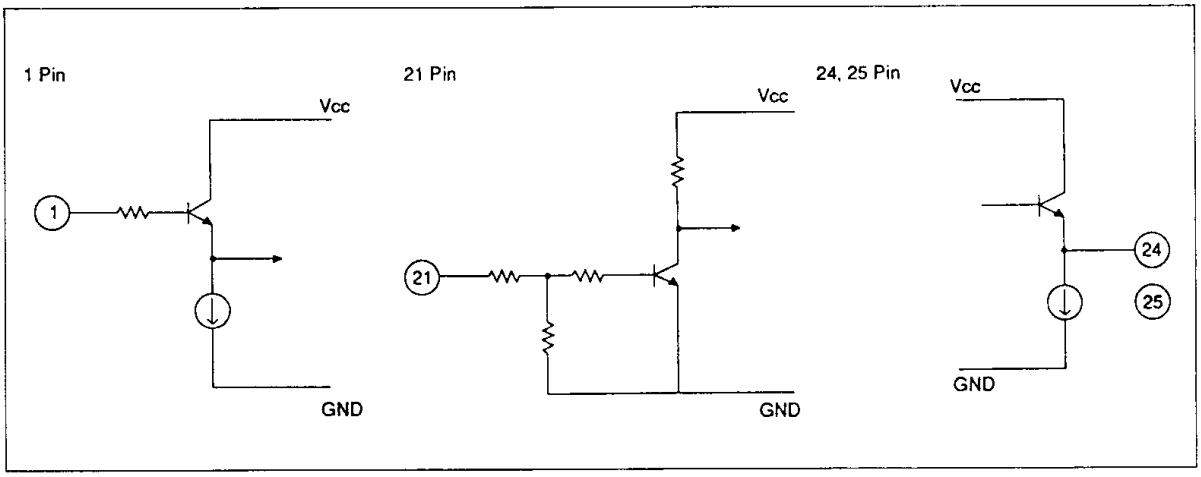
Table 1 Pin Description

Pin No.	Pin name	I/O	Pin function	Connecting Destination
1	LM1	I	Limiter amplifier input pin	HA12133MP
2	NC	—		
3	AVcc	Vcc	Analog power supply	
4	$\overline{\text{SRCHI}}$	—	Switching signal input pin for loop filter	μ-COM
5	TEST2	—	Test pin. Connect to GND through capacitor.	
6	BYP1	—	Bias supply bypass capacitor connection pin	
7	SRCHO	—	Switching signal output pin for loop filter	
8	AGND	GND	Analog GND	
9	CC1	—	DC amplifier bypass capacitor connection pin	
10	CC2	—	C and R connection pin for loop filter	
11	BYP3	—	Bias supply bypass capacitor connection pin	
12	BYP4	—	VCO bypass capacitor connection pin	
13	VCO1	O	VCO tank coil connection pin	
14	VCO2	O	VCO tank coil connection pin	
15	VCI	I	VCO tank coil (secondary) connection pin	
16	BYP5	—	Bias supply bypass capacitor connection pin	
17	AGC	—	Capacitor connection pin for AGC detection	
18	BYP6	—	AGC bypass capacitor connection pin	
19	TEST3	—	Test pin. Connect to GND.	
20	NC	—		
21	$\overline{\text{RPSEL}}$	I	Switching signal input pin for recording/playback	μ-COM
22	CC3	—	Capacitor connection pin for ASPC loop filter	
23	CC4	—	Capacitor connection pin for ASPC loop filter	

Pin Description (cont)

24	$\overline{\text{PDCK}}$	O	Clock output pin	Signal processing LSI
25	PDATA	O	Playback data output pin	Signal processing LSI
26	DGND	GND	Digital GND	
27	BYP7	—	Bias supply bypass capacitor connection pin	
28	DVCC	Vcc	Digital power supply	

I/O Equivalent Circuit



Functional Description

The HA12062AMP discriminates between data "0" and "1" by playback signal with equalized waveform, and outputs the data to the next signal processing LSI together with the clock signal.
The HA12062AMP is composed of a clock generation block and ASPC (automatic strobe point control) block as shown in the diagram.
These two blocks are explained below.

Clock Generation Block

The clock generation block is composed of a PLL circuit using a sample hold type phase comparator. The sample hold circuit executes VCO output sample hold using edge pulse (sampling pulse) which has playback signal phase data created by edge detection circuit, and compares phases between the playback and VCO output signals.
The VCO controls phase shift caused by temperature change by using a vector addition LC oscillator of small temperature drift.

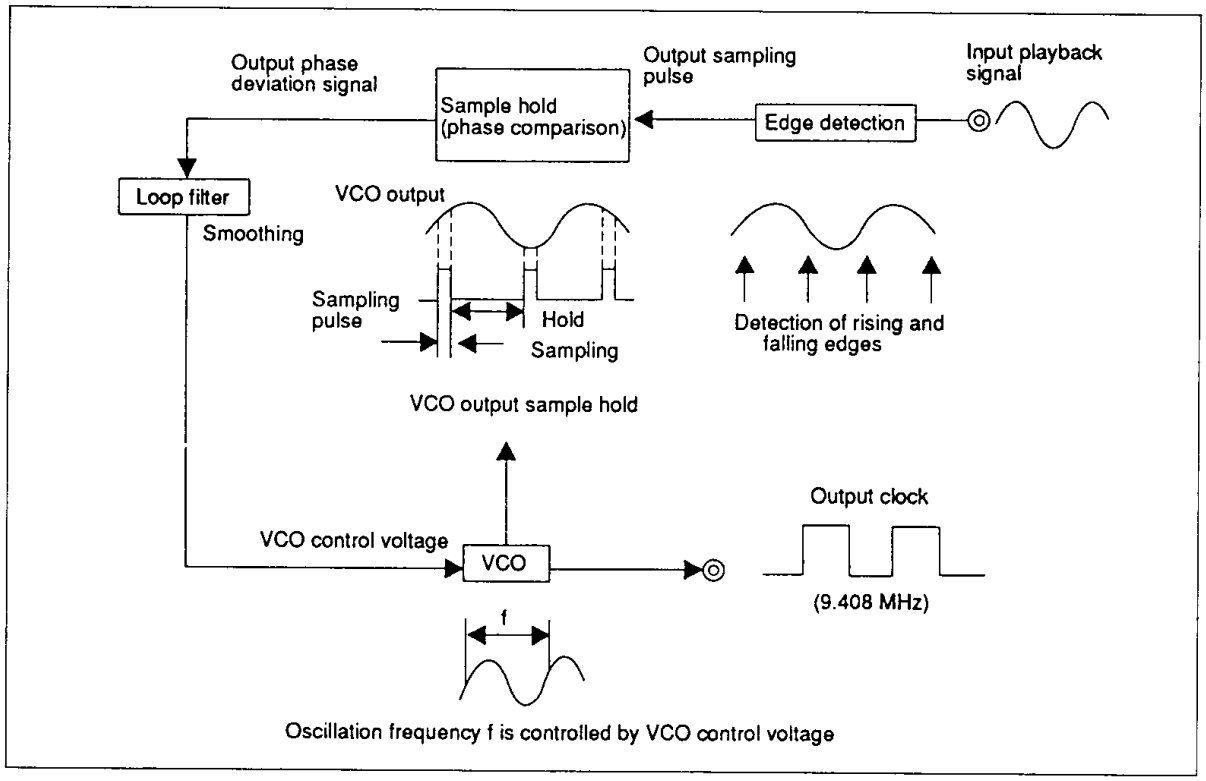


Figure 1 Clock Generation Block Structure

Sample hold circuit: The sample hold circuit executes sample hold of the VCO output waveform by a sampling pulse and outputs a phase deviation signal between the playback and VCO output signals.

The sample hold I/O waveform is shown in figure 2.

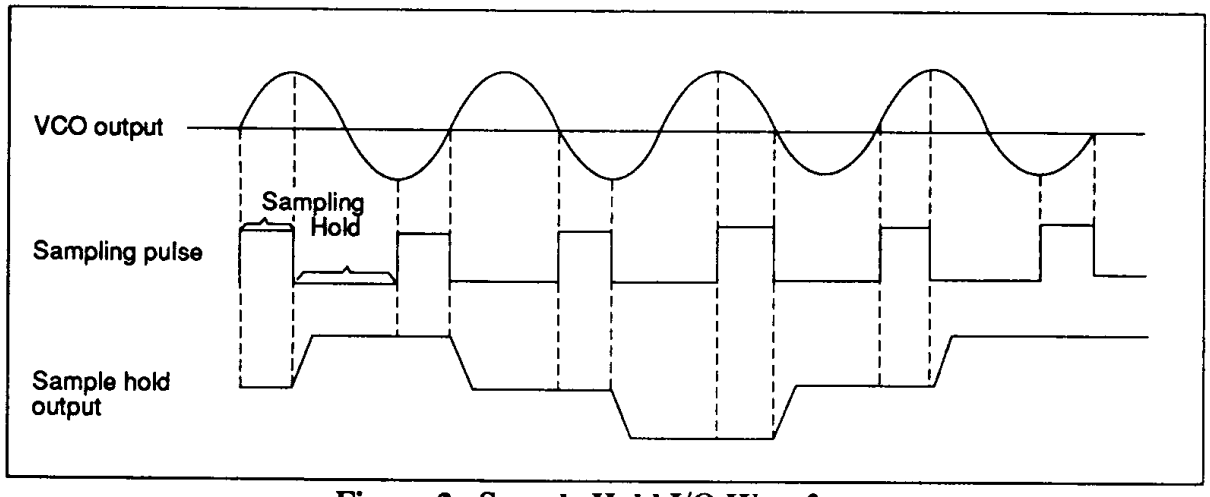


Figure 2 Sample Hold I/O Waveform

Loop filter: The output signal from the sample hold circuit is smoothed by a loop filter. The external loop filter constants are the values of C and R in figure 3.

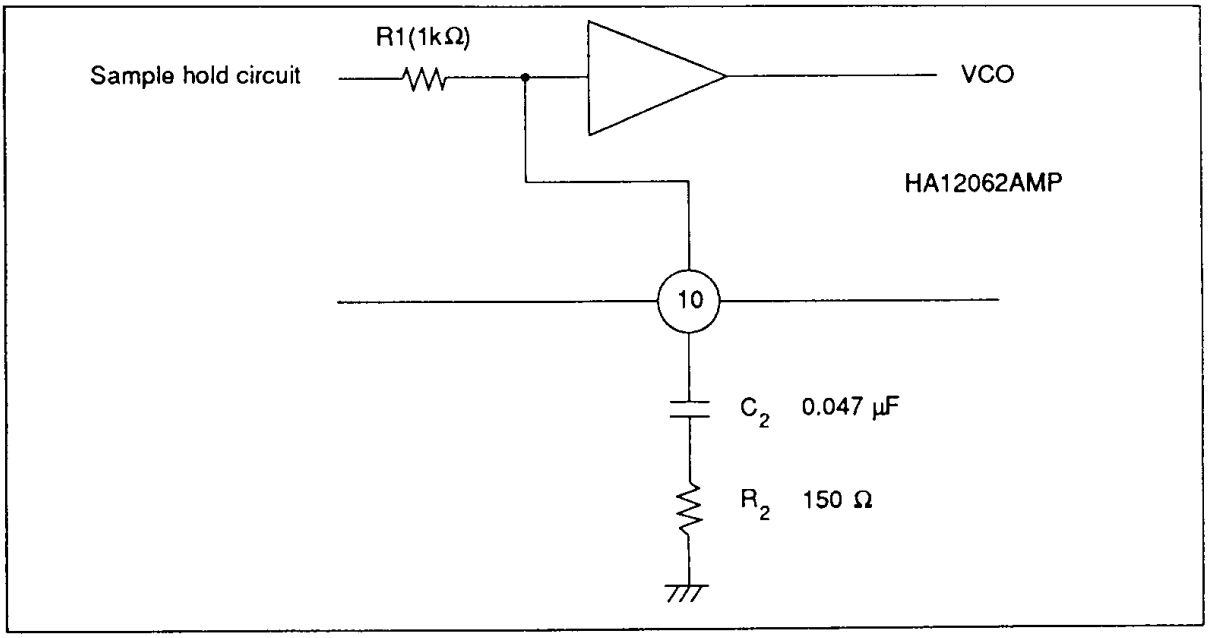


Figure 3 Loop Filter Structure

VCO: A vector addition LC oscillator is employed for the VCO.
To adjust the tank circuit, taking the C and R constants as in figure 4, refer to VCO fo adjustment in electrical characteristics measuring method.
The VCO operating principle is as shown in figure 5. First, vector addition of vector $\dot{a}$ and $\dot{b}$ creates $\dot{c}$ from which basic wave component D is extracted by the tank circuit. It is then oscillated after positive feedback.
The change of oscillation frequency is done by controlling the vector adder addition ratio.

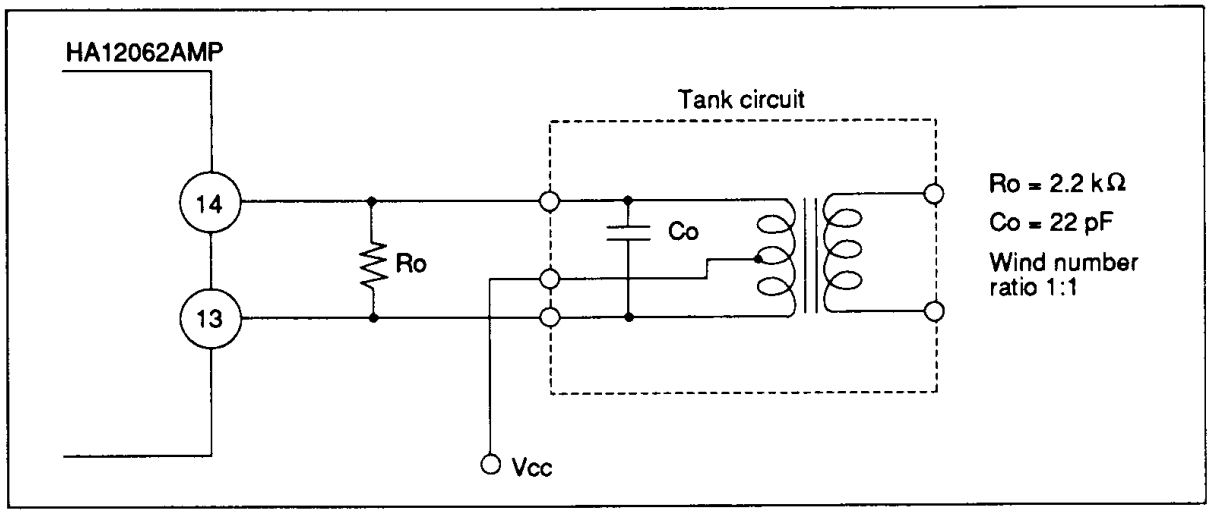


Figure 4 Tank Circuit Structure

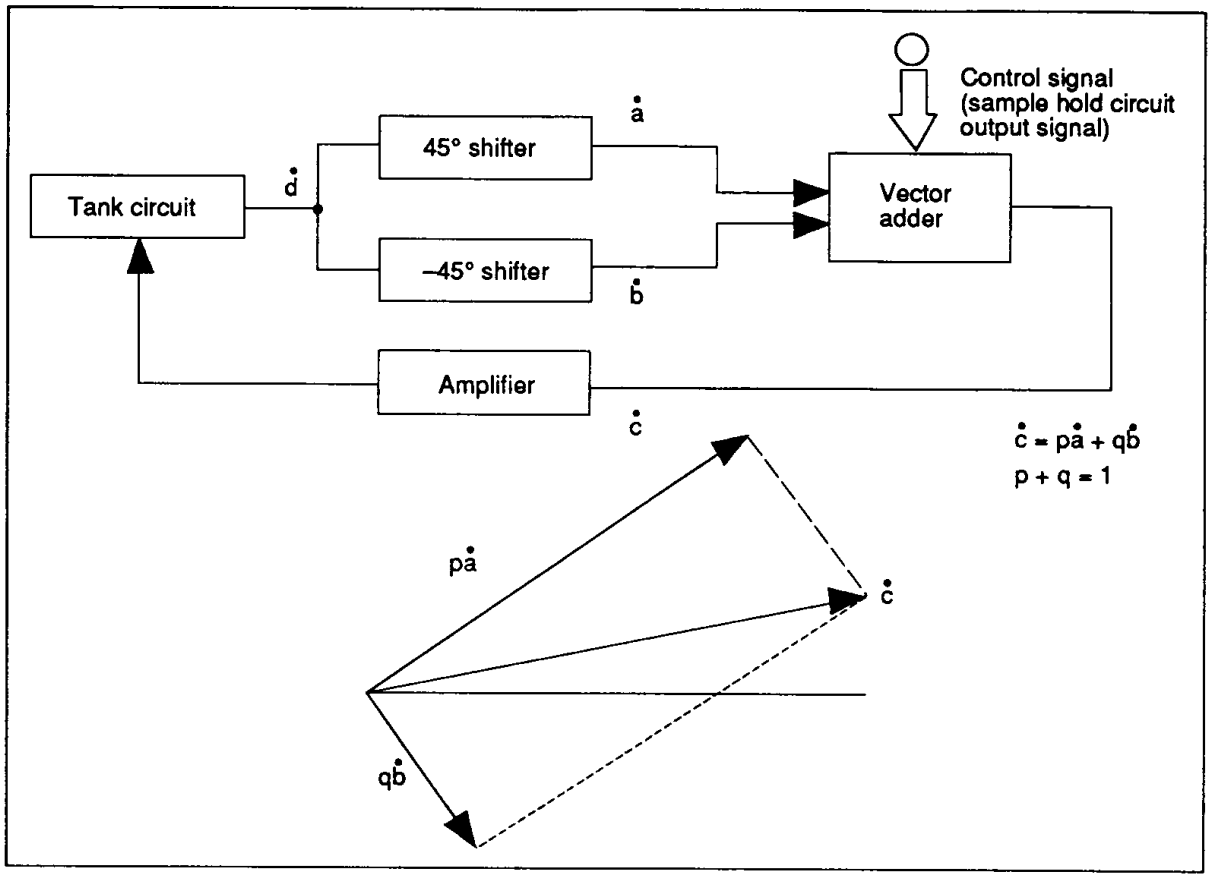


Figure 5 VCO Structure

ASPC Block

The ASPC block is composed of a strobe point deviation detection circuit and clock shift circuit. The clock shift circuit shifts the phase of the generated clock signal according to detected deviation data.

The strobe point should be controlled to appear in the center of the eye pattern as shown in figure 7.

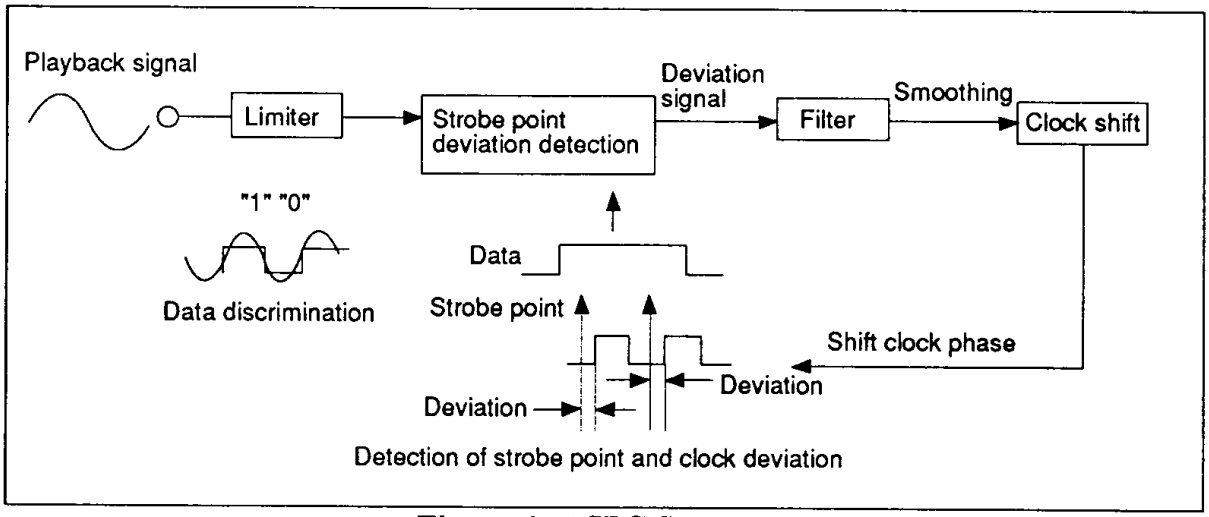


Figure 6 ASPC Structure

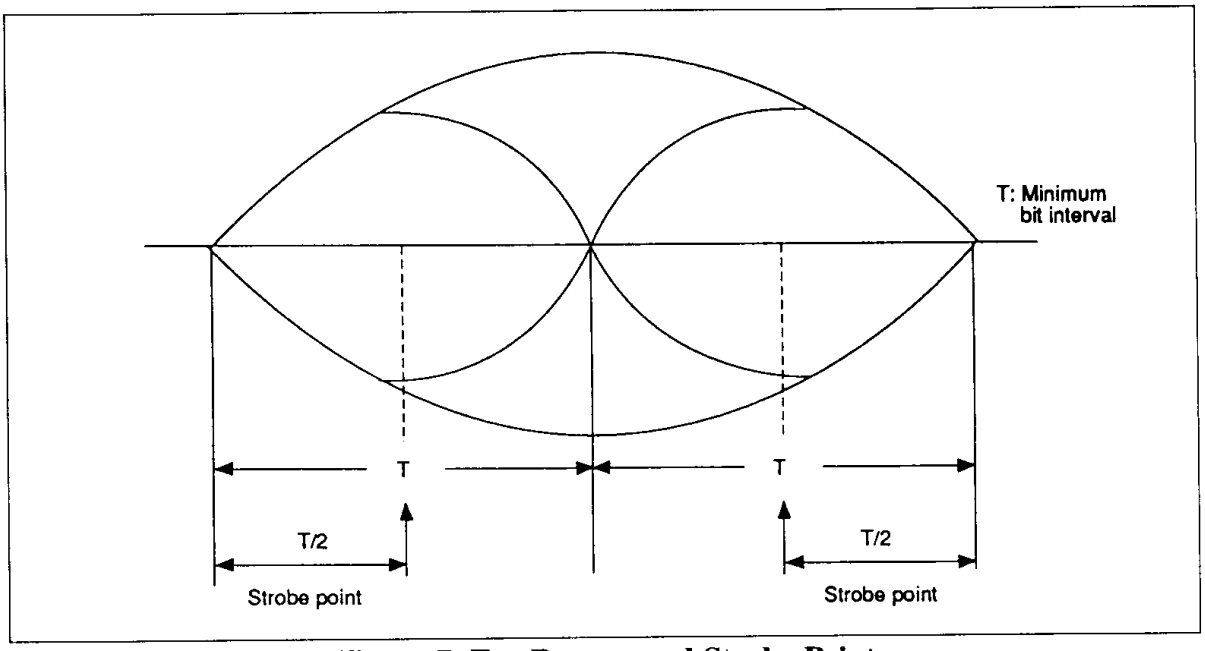


Figure 7 Eye Pattern and Strobe Point

Deviation detection of strobe point: Strobe point deviation data is created by using output pulse width obtained by taking the XOR of D-F/F I/O signals as shown in figure 8.
Figure 9-1 shows the case where the strobe point is in the center of the eye pattern, figure 9-2 shows the case where it is delayed, and figure 9-3 shows the case where it precedes the center of eye pattern.
However, signal E data can not be used as a strobe point control signal, because it changes according to input data ("1" or "0"). To remove this I/O data influence, subtraction between signal G and deviation signal E should be executed. As a result, the subtraction output signal H becomes the control signal of the strobe point.

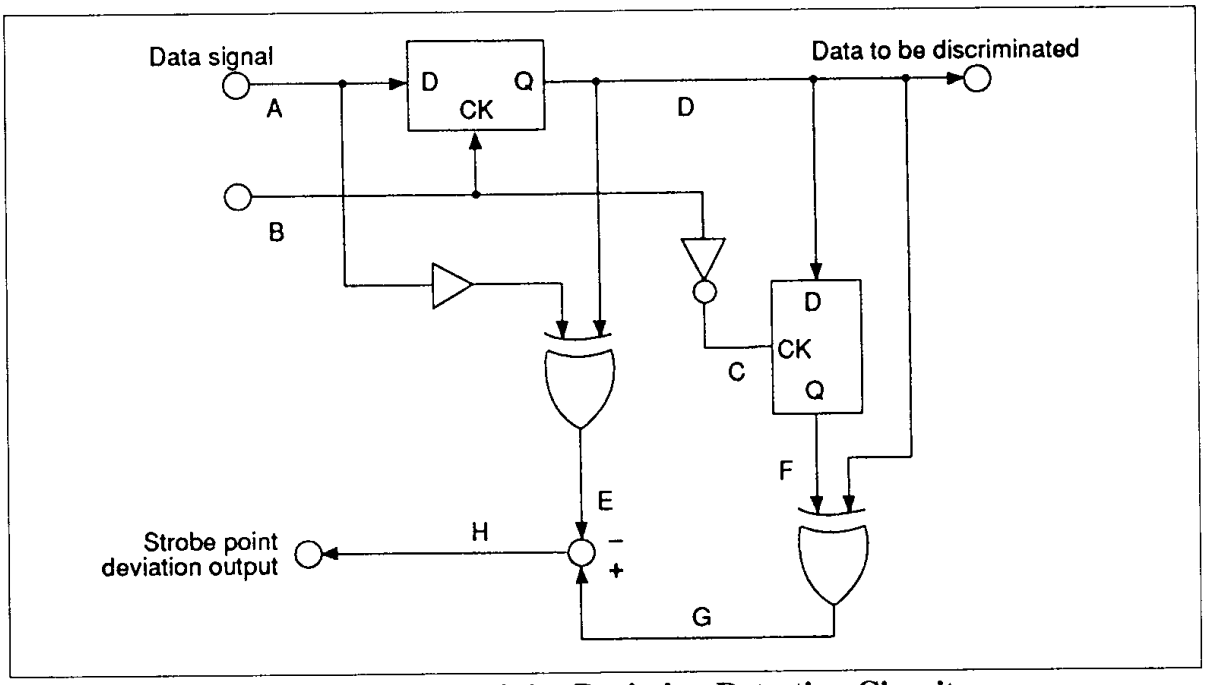


Figure 8 Strobe Point Deviation Detection Circuit

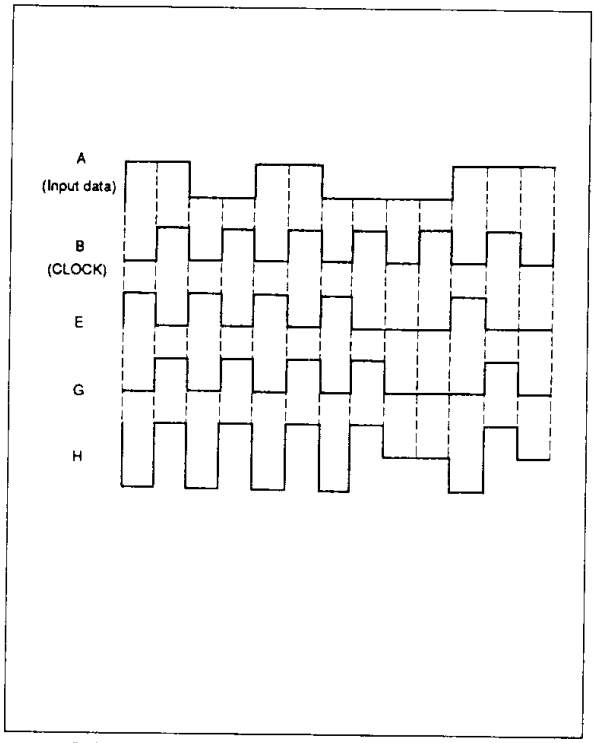


Figure 9-1 Best-fit Strobe Point

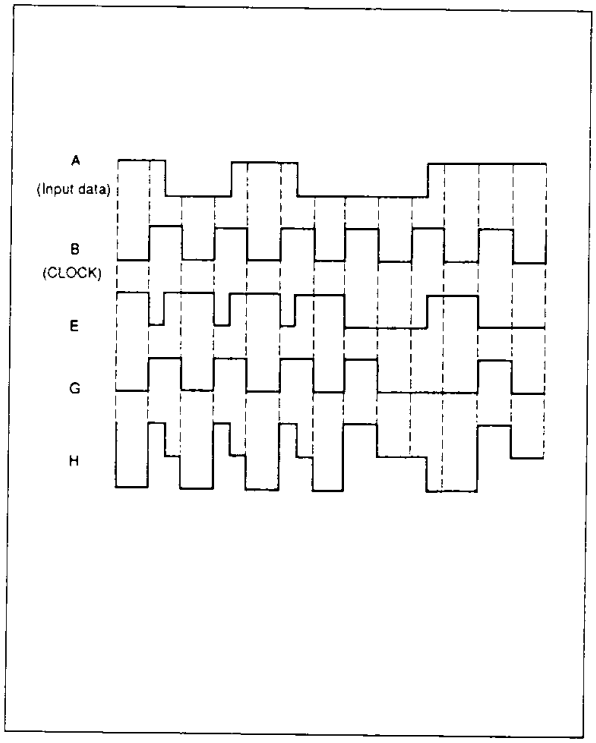


Figure 9-2 Late Strobe Point

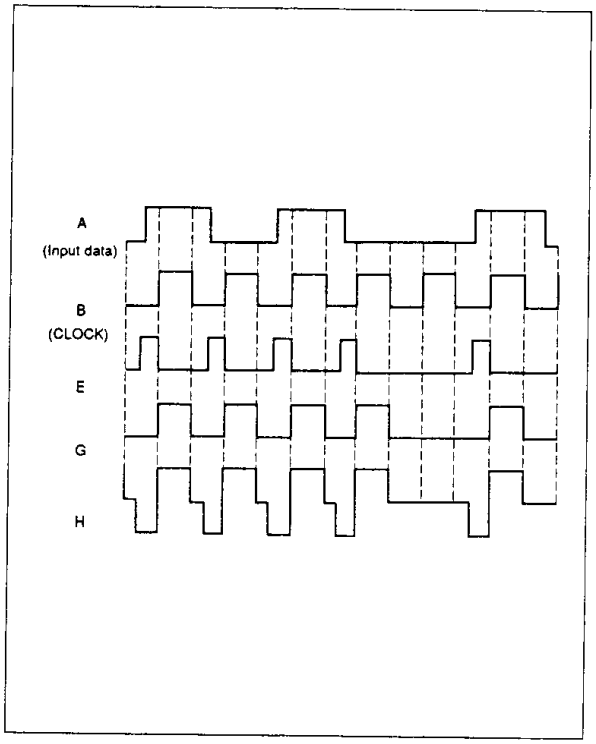


Figure 9-3 Early Strobe Point

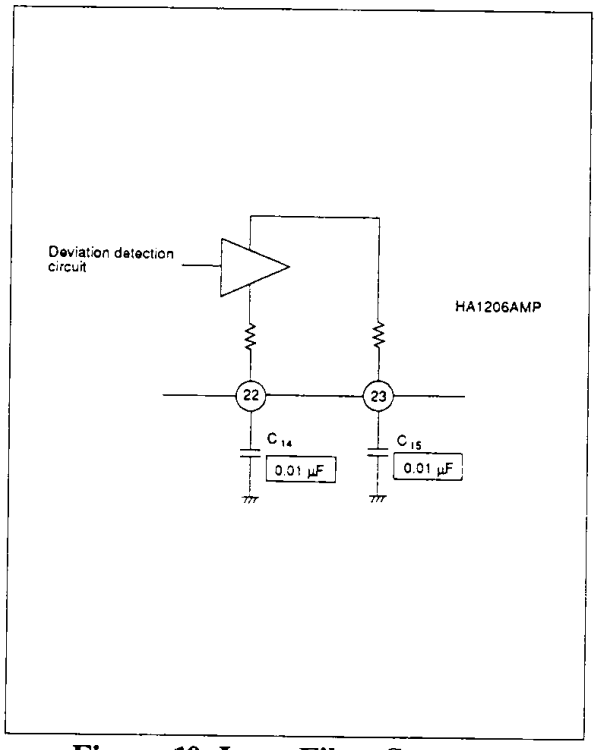


Figure 10 Loop Filter Structure

Loop filter: Output of the strobe point deviation detection circuit is smoothed through the loop filter. As an external capacitor, the 0.01 μF in figure 10 is recommended.

Clock shifter: The clock shifter inputs a signal to a shift circuit through a filter to restrain pulsation of strobe point deviation detection signal.

The shift circuit executes clock shift by changing the vector composite ratio of ±180° and ±90°. The control characteristic of the composite ratio is shown in figure 12. The shift operation is possible in the range of ±90°.

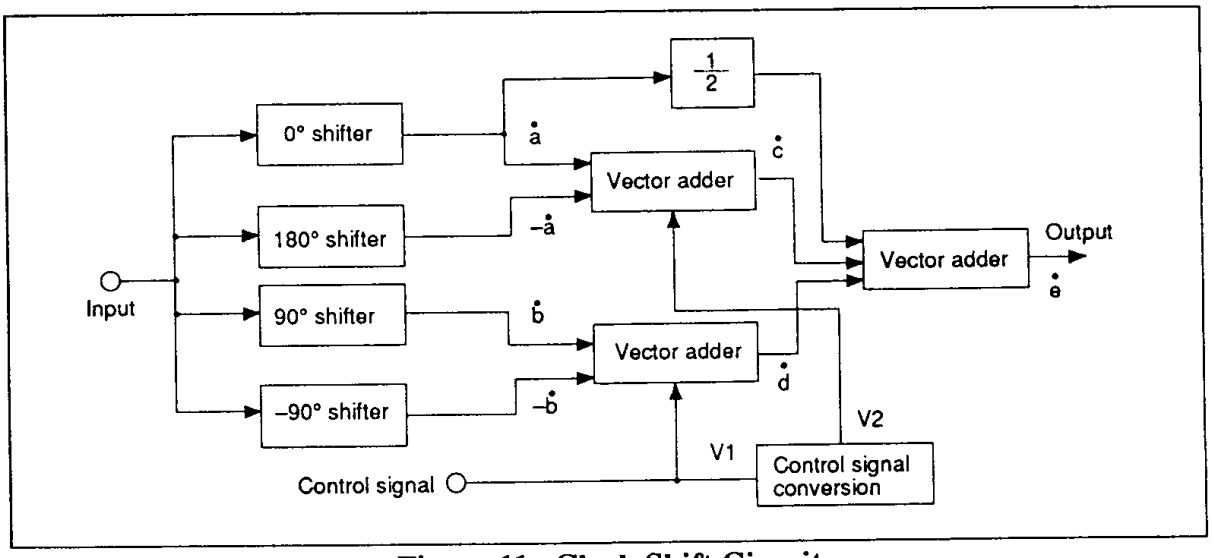


Figure 11 Clock Shift Circuit

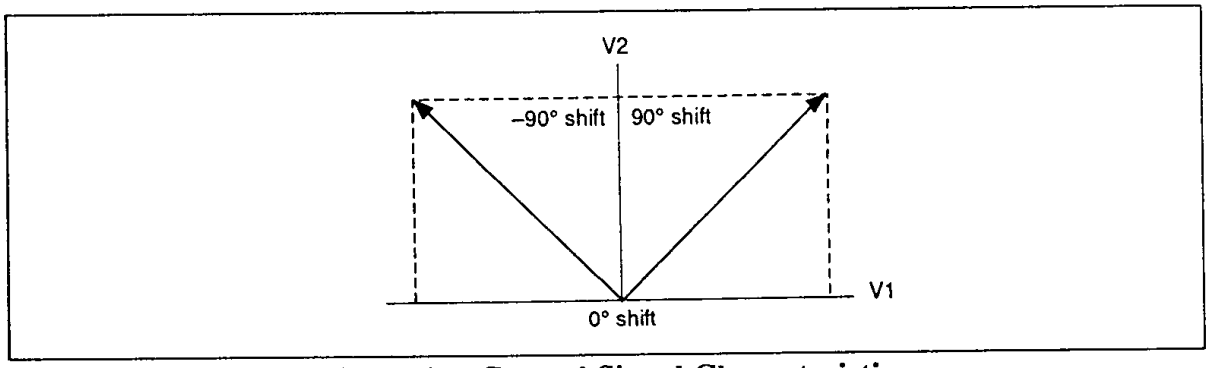


Figure 12 Control Signal Characteristic

Data Strobe Timing

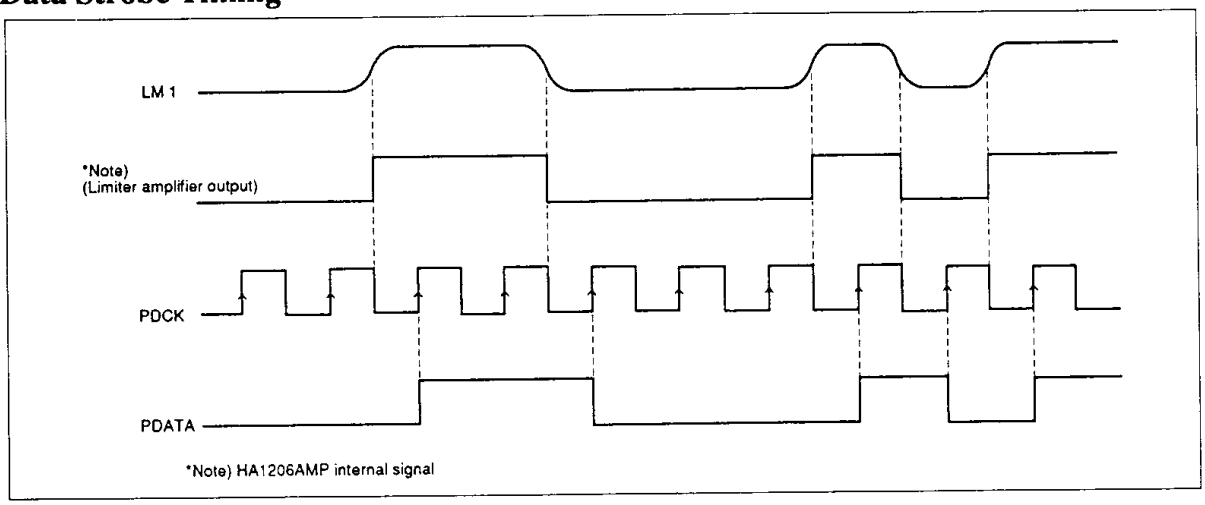


Table 2 Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	Vcc	+6.0	V	
Power dissipation	PT	550	mW	(Ta = 75 °C)
Operation temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Table 3 Electrical Characteristics (Ta = 25 °C, Vcc = +5.0 V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Pin no.
Supply voltage	Vcc	4.75	5.0	5.5	V	Standard operation	
Supply current	$I_{Q(1)}$	21.0	40.0	60.0	mA	No signal (PLAY MODE)	
PLL lock range	$f_{H(1)}$	±0.95	±1.2	±1.5	MHz	f = 4.704 MHz, Vin = 0.5 Vpp	
PLL lock range	$f_{H(2)}$	±0.95	±1.2	±1.5	MHz	f = 2.352 MHz, Vin = 0.5 Vpp	
PLL capture range	$f_{P(1)}$	±0.75	±1.1	±1.5	MHz	f = 4.704 MHz, Vin = 0.5 Vpp	
PLL capture range	$f_{P(2)}$	±0.75	±1.1	±1.5	MHz	f = 2.352 MHz, Vin = 0.5 Vpp	
ASPC detection sensitivity	$K_{(1)}$	15	29	60	mV/ns	f = 4.704 MHz, Vin = 0.5 Vpp	
ASPC detection sensitivity	$K_{(2)}$	7	14.1	28	mV/ns	f = 2.352 MHz, Vin = 0.5 Vpp	
ASPC offset	$T_{(1)}$	—	4.7	15	ns	f = 4.704 MHz, Vin = 0.5 Vpp	
ASPC offset	$T_{(2)}$	—	9.5	30	ns	f = 2.352 MHz, Vin = 0.5 Vpp	
Logic out duty	$D_{(1)}$	30	50	70	%	f = 4.704 MHz, Vin = 0.5 Vpp	24, 25
Input "Low" level	V_{IL}	—	—	1.0	V		21
Input "High" level	V_{IH}	4.0	—	—	V		21

Electrical Characteristics (Ta = 25 °C, Vcc = +5.0 V) (cont)

Output "Low" level	V_{OL}	—	—	1.5	V	f = 4.704 MHz, Vin = 0.5 Vpp	24, 25
Output "High" level	V_{OH}	3.5	—	—	V	f = 4.704 MHz, Vin = 0.5 Vpp	24, 25
Input current "Low"	I_{IL} 21	−10	0	—	μA	Vin = 0 V	21
Input current "High"	I_{IH} 21	—	130	350	μA	Vin = 5 V	21
Input current "Low"	I_{IL} 4	−10	0	—	μA	Vin = 0 V	4
Input current "High"	I_{IH} 4	—	430	650	μA	Vin = 5 V	4
Output leakage current	I_L	—	—	10	μA	4 Pin = 0.3 V 7 Pin = 5 V	
Output ON resistance	R_{ON}	—	10	15	Ω	4 Pin = 4.6 V 7 Pin I_{ON} = 1 mA	

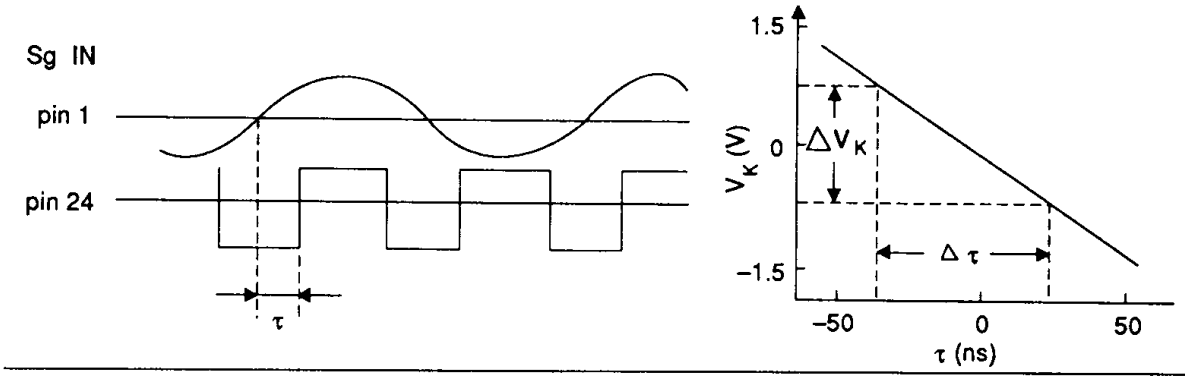
Electrical Characteristics Testing

Electrical characteristics are measured according to test circuit I, II, and the switch matrix table as follows.

Item	Measuring method and judging standard
VCOfo	Adjust the tank coil to acquire an M3 frequency of fo = 8.35 MHz.
$I_{Q(1)}$	Measure total current of pins 3 and 28 when there is no signal in PLAY mode.
$f_{H(1)}$	1) Sg1: f_1 = 4.704 MHz, Vin = 0.5 Vpp 2) Regard as $f_{H(1)}$ the point where f_3 (M3 frequency) is not f_1 x 2, sweeping f_1 to (+) and (−) sides around 4.704 MHz. $f_{H(1)} = (f_1 \times 2 - 9.408\ MHz)$
$f_{H(2)}$	1) Sg1: f1 = 2.352 MHz, Vin = 0.5 Vpp 2) Regard as $f_{H(2)}$ the point where f_3 (M3 frequency) is not f1 x 4, sweeping f1 to (+) and (−) sides around 2.352 MHz. $f_{H(2)} = (f_1 \times 4 - 9.408\ MHz)$
$f_{P(1)}$	1) Sg1: f_1 = 3.4 MHz, V_{in} = 0.5 Vpp 2) Regard as $f_{P(1)}$ the point where f_3 (M3 frequency) is f_1 x 2, sweeping f_1 from (−) side to 4.704 MHz. $f_{P(1)} = (f_1 \times 2 - 9.408\ MHz)$ 3) Sg1: f_1 = 5.9 MHz, V_{in} = 0.5 Vpp 4) Regard as $f_{P(1)}$ the point where f_3 (M3 frequency) is f_1 x 2, sweeping f_1 from (+) side to 4.704 MHz. $f_{P(1)} = (f_1 \times 2 - 9.408\ MHz)$

Electrical Characteristics Testing (cont)

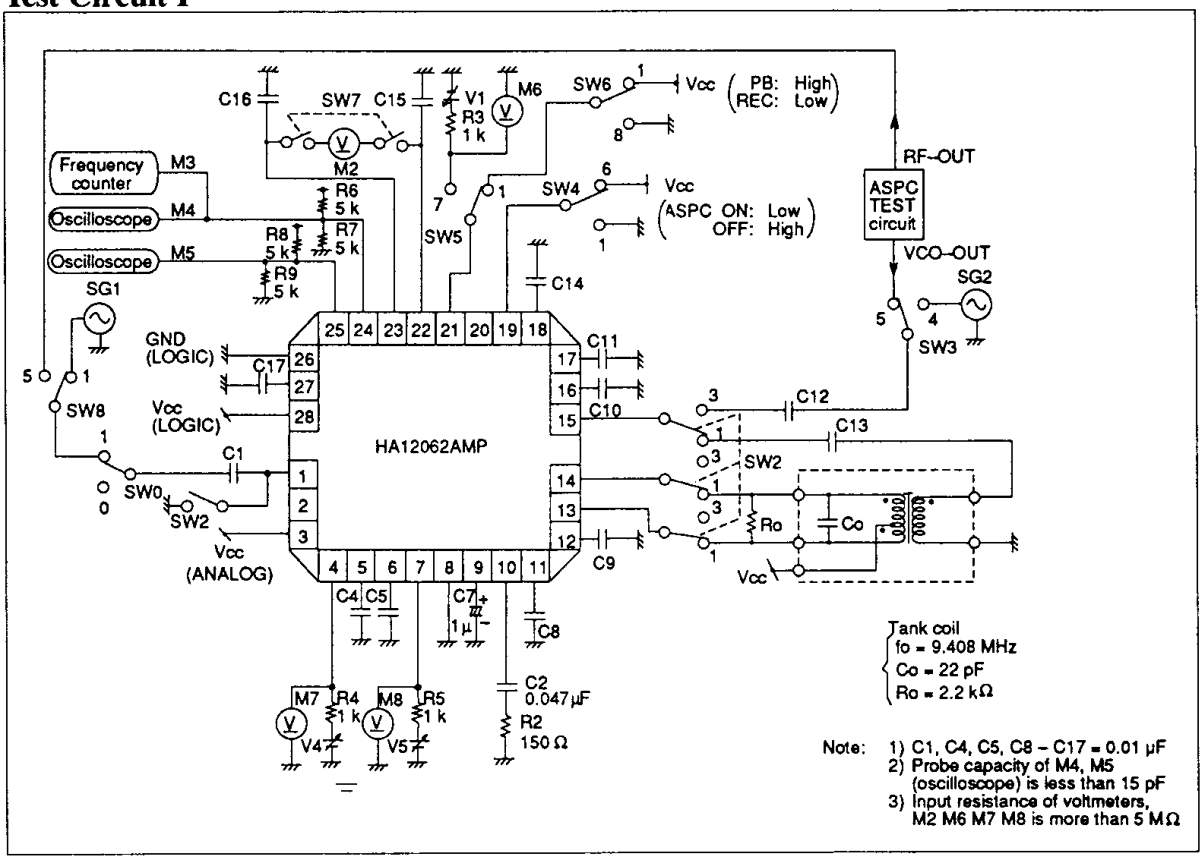
$f_{P(2)}$	1) Sg1: f_1 = 1.7 MHz, Vin = 0.5 Vpp 2) Regard as $f_{P(2)}$ the point where f_3 (M3 frequency) is f_1 x 4, sweeping f_1 from (–) side to 2.352 MHz. $f_{P(2)} = (f_1 \times 4 - 9.408\ MHz)$ 3) Sg1: f_1 = 3.3 MHz, V_{in} = 0.5 Vpp 4) Regard as $f_{P(2)}$ the point where f_3 (M3 frequency) is f_1 x 4, sweeping f_1 from (+) side to 2.352 MHz. $f_{P(2)} = (f_1 \times 4 - 9.408\ MHz)$
$K_{(1)}$ $K_{(2)}$	1) Sg3: f_2 = 18.816 MHz, Vin = 0.5 Vpp 2) Measure the M2 voltage V_{K1}, combining SW9 and SW10 and shifting strobe point offset by τ. 3) Calculate $K_{(1)}$ and $K_{(2)}$ using $\frac{\Delta Vk}{\Delta \tau}$



$T_{(1)}$ $T_{(2)}$	1) Adjust the SW9 and SW10 to acquire an M_2 voltage of V_M = 0 V and strobe point offset is ± 30 ns. 2) Set SW4 to 1. 3) Measure the M_2 voltage. $V_{M2(1)}$, $V_{M2(2)}$ 4) Calculate $T_{(1)}$, $T_{(2)}$ using. $T_{(1)} = \left\lvert \frac{V_{M2(1)}}{k_{(1)}} \right\rvert$ or $T_{(2)} = \left\lvert \frac{V_{M2(2)}}{k_{(2)}} \right\rvert$
$D_{(1)}$	1) Sg1: f_1 = 4.704 MHz, Vin = 0.5 Vpp 2) Measure duty of M4 and M5 at Vth = 2.5 V
V_{IL} V_{IH}	Measure the V1 voltage setting M4 to "High" when CLK is output and to "Low" when CLK is extinguished.
V_{OL} V_{OH}	Measure the "High" and "Low" level of M4 and M5 inputting Sg1: f = 4.704 MHz and Vin = 0.5 Vpp
$-I_{IL}21$ $I_{IH}21$	Measure the $-I_{IL}21$ when V21 = 0 V Measure the $I_{IH}21$ when V21 = 5 V
$-I_{IL}4$ $I_{IH}4$	Measure the $-I_{IL}4$ when V4 = 0 V Measure the $I_{IH}4$ when V4 = 5 V

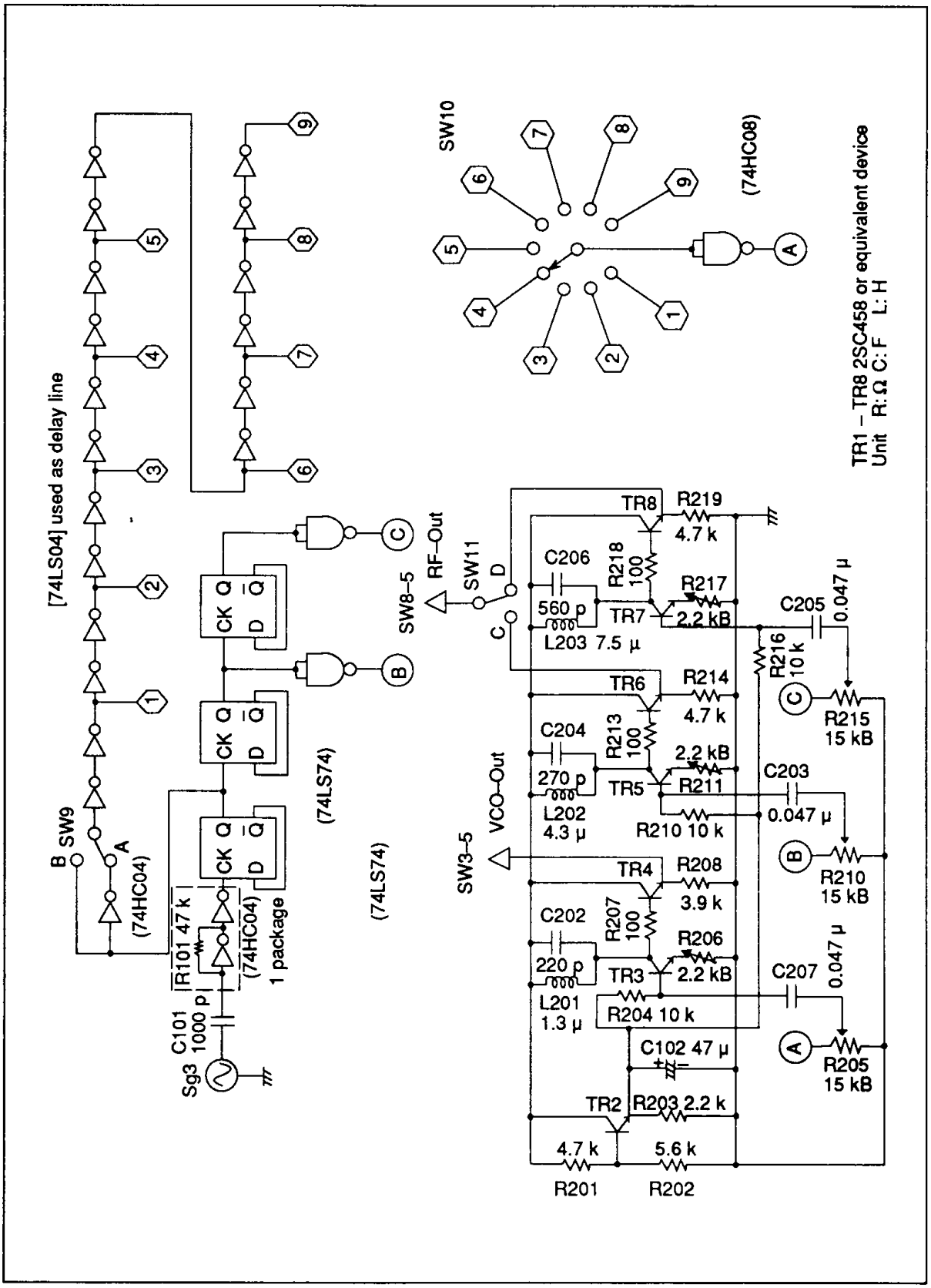
I_L	1) V4 = 0.3 V, V7 = 5 V 2) Measure the V5 current.
R_{ON}	1) V4 = 4.6 V 2) Measure the M8 voltage $V_{(1)}$ when I_S = 0 3) Measure the M8 voltage $V_{(2)}$ when I_S = 1 mA 4) Calculate R_{ON} using $R_{ON} = \frac{V_{(2)} - V_{(1)}}{1\ mA}$

Test Circuit I



Note: 1) C1, C4, C5, C8 – C17 = 0.01 µF
2) Probe capacity of M4, M5 (oscilloscope) is less than 15 pF
3) Input resistance of voltmeters, M2 M6 M7 M8 is more than 5 MΩ

Test Circuit II (ASPC Test Circuit)



Switch Matrix Table

	Switch No.									
Item	**SW0**	**SW2**	**SW3**	**SW4**	**SW5**	**SW6**	**SW7**	**SW8**	**SW11**	**SW12**
$I_{Q(1)}$	0	1	—	1	1	1	OFF	1	—	OFF
$f_{H(1)}$	1	↓	—	↓	↓	↓	↓	↓	—	↓
$f_{H(2)}$	↓	↓	—	↓	↓	↓	↓	↓	—	↓
$f_{P(1)}$	↓	↓	—	↓	↓	↓	↓	↓	—	↓
$f_{P(2)}$	↓	↓	—	↓	↓	↓	↓	↓	—	↓
$K_{(1)}$	↓	3	5	6	↓	↓	ON	5	C	↓
$K_{(2)}$	↓	↓	↓	↓	↓	↓	↓	↓	D	↓
$T_{(1)}$	↓	↓	↓	6→1	↓	↓	↓	↓	C	↓
$T_{(2)}$	↓	↓	↓	6→1	↓	↓	↓	↓	D	↓
$D_{(1)}$	↓	1	—	1	↓	↓	OFF	1	—	↓
V_{IL}	1	↓	—	↓	7	—	↓	↓	—	↓
V_{IH}	↓	↓	—	↓	↓	—	↓	↓	—	↓
V_{OL}	↓	↓	—	↓	1	1	↓	↓	—	↓
V_{OH}	↓	1	—	↓	↓	↓	↓	↓	—	↓
$-I_{IL21}$	↓	↓	—	↓	7	—	↓	↓	—	↓
I_{IH21}	↓	↓	—	↓	↓	—	↓	↓	—	↓
I_{IL4}	↓	↓	—	↓	1	1	↓	↓	—	↓
I_{IH4}	↓	↓	—	↓	↓	↓	↓	↓	—	↓
I_L	↓	↓	—	↓	↓	↓	↓	↓	—	↓
R_{ON}	↓	↓	—	↓	↓	↓	↓	↓	—	↓
VCO ADJ	0	↓	—	↓	↓	↓	↓	↓	—	ON

Application

A system package circuit example is shown in figure 13, and its adjusting method and specs are shown in table 4.

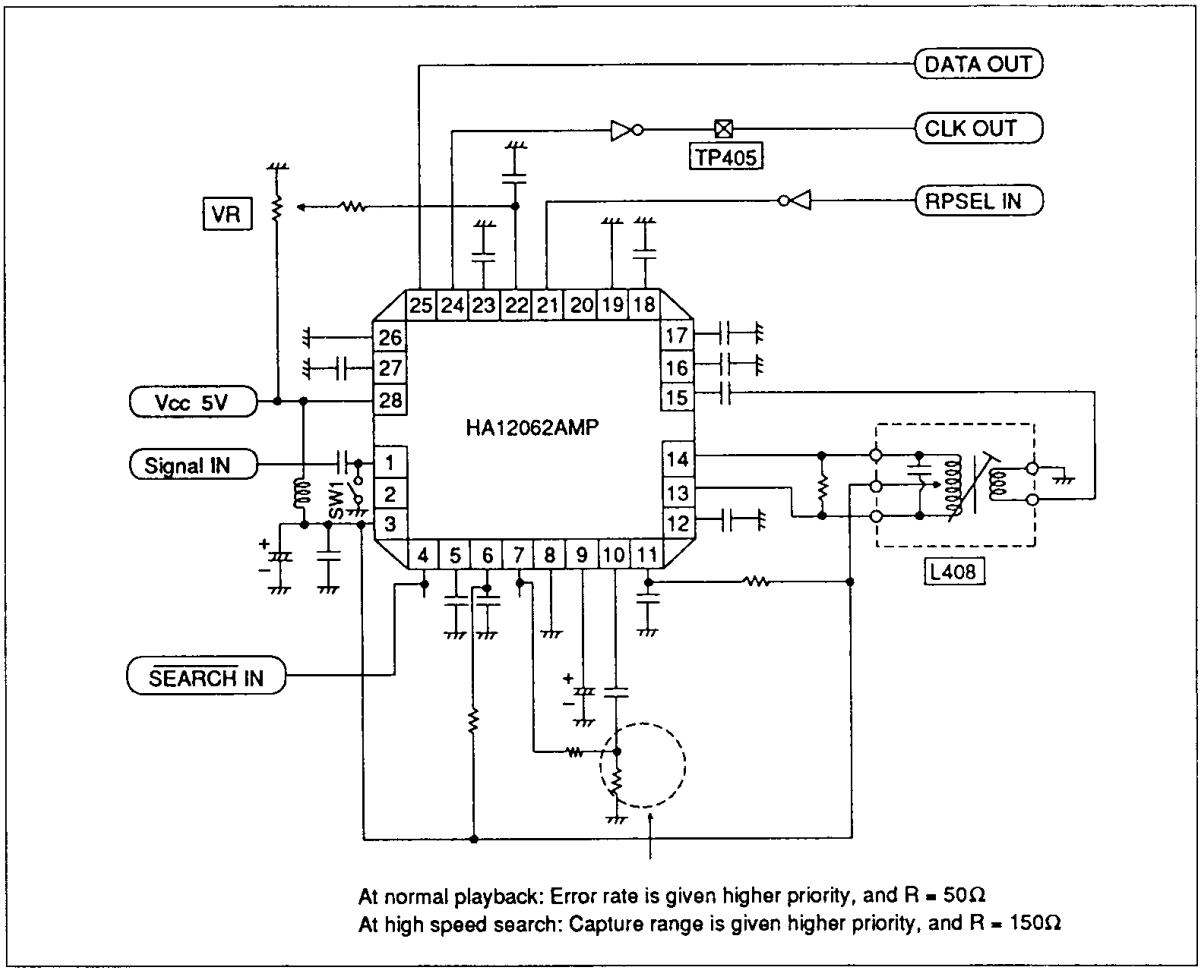


Figure 13 Adjusting Method and Specs

Table 4 Package Circuit

No.	Item	Adjusting method	Specs	Remarks
1	PLL free running frequency	• Operation mode: stop • Point to be adjusted: L408 • Point to be measured: TP405 • Measuring apparatus: frequency counter	8.35 MHz ±10 kHz	SW1 ON
2	ASPC phase error	• Operation mode: playback • Point to be adjusted: VR • Measuring apparatus: error counter	Best-fit error rate	