
HA13566AF

Combo (Spindle & VCM) Driver

HITACHI

ADE-207-250 (Z)
1st Edition
December 1997

Description

The HA13566AF is combination of Spindle and VCM Driver designed for HDD and have following functions and features.

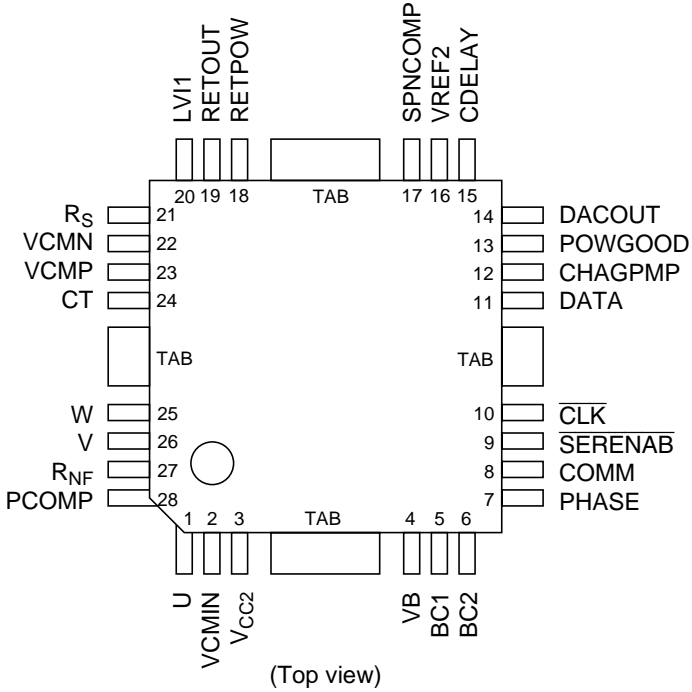
Functions

- 1.0 A max/3-phase spindle motor driver
- 400 mA max VCM driver
- 100 mA max retract driver
- 11 bit serial interface
- 9 bit DAC for VCM control
- Commutation logic for sensor-less motor
- Center tap pull-up driver for half wave driver
- Soft switching matrix
- Charge pump
- Booster
- Power monitor
- OTSD

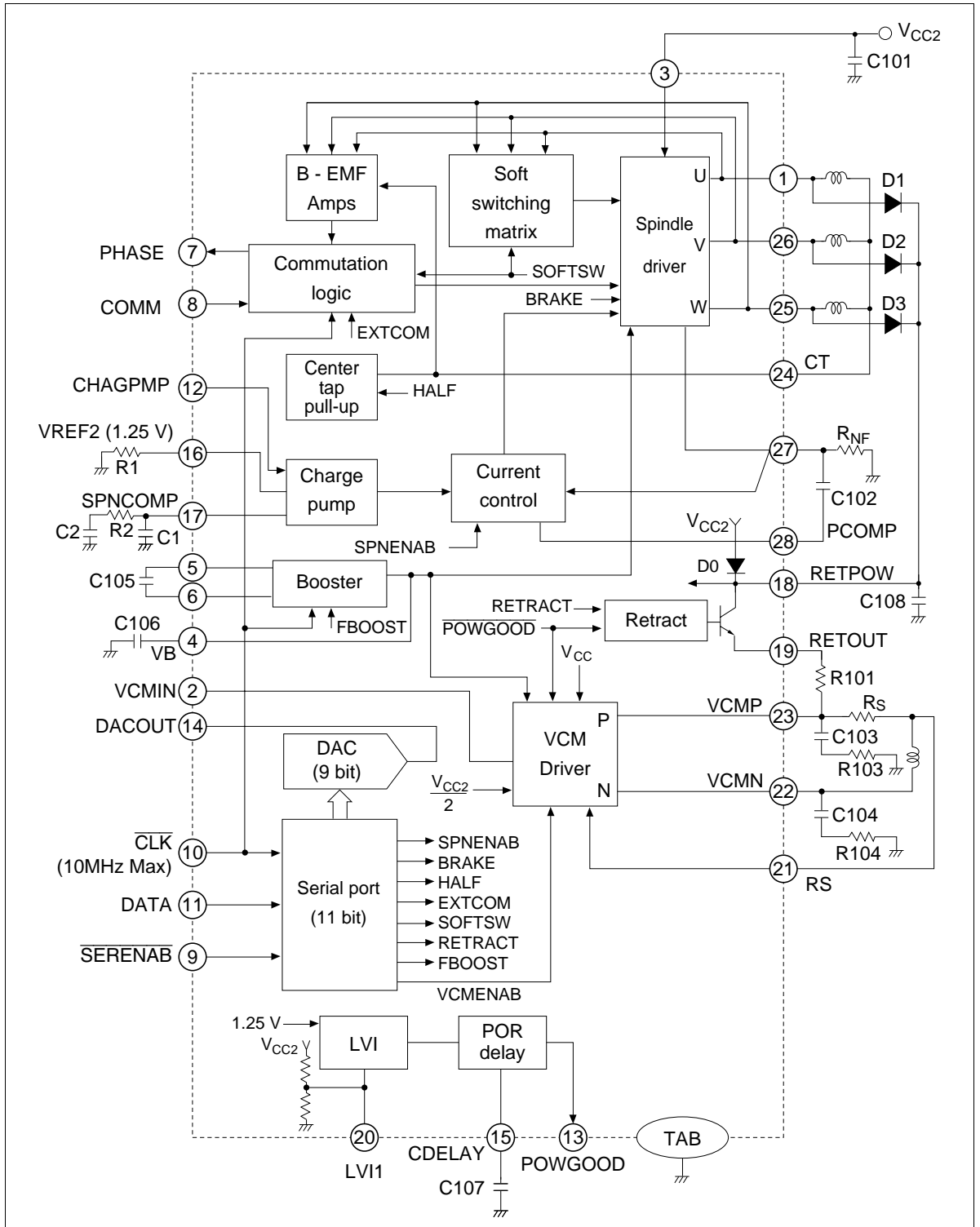
Features

- Low output saturation voltage
 - Spindle driver 1.0 V typ (@0.8 A)
 - 0.2 V typ (@0.1 A)
 - VCM driver 1.0 V typ (@400 mA)
- Soft switching drive
- Minimum surface mount package
body size 7×7 mm

Pin Arrangement



Block Diagram



Serial Port

Construction

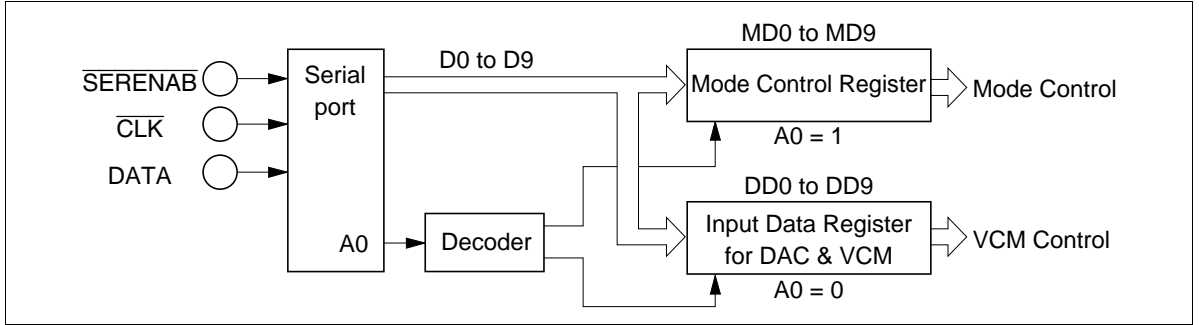


Figure 1 Serial Port

Data construction

Input Data Construction

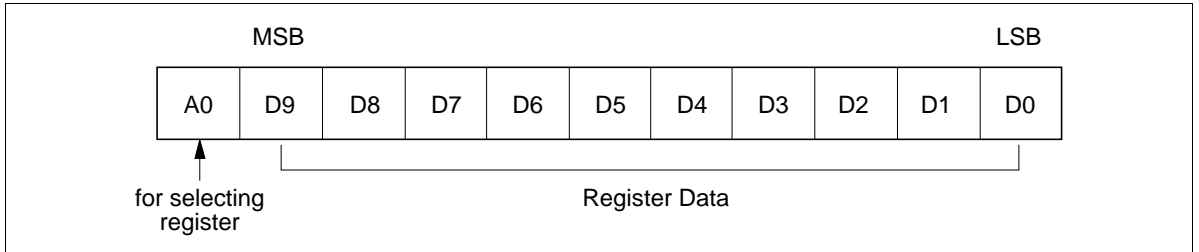


Figure 2 Input Data (1)

The serial port is required the 11 bit data (D0 to D9 and A0). Address bit A0 is used to select the register as follows. When the data length is less than 11 bits, the internal register will not be up dated. And when the data length is more than 11 bits, this register will take late 10 bits and ignore the faster bit.

A0	Register
0	Input data register of DAC & VCMGAIN
1	Mode control register

Mode Control Register (A0 = 1)

Bit	Symbol	1	0	Note
MD0	SPNENAB	Spindle enable	Spindle disable	1
MD1	BRAKE	Brake enable	Brake disable	1
MD2	Not use	—	—	
MD3	HALF	Half wave drive	Full wave drive	
MD4	EXTCOM	External commutation	Internal commutation	2
MD5	SOFTSW	Soft switching	Switching	
MD6	VCMENAB	VCM enable	VCM disable	
MD7	RETRACT	Retracting	Not retracting	
MD8	POLESEL	for 12 poles motor	for 8 poles motor	3
MD9	FBOOST	Low frequency	High frequency	4

- Notes:
1. The spindle motor is independently winding to the value of the MD2, during the MD1 is true.
 2. The bit MD4 select a commutation mode at driving by B-EMF sensing. (See Commutation timing)
 3. In order to prevent the misdetection of back-EMF amplifier, the bit MD8 should be chosen as shown above table.
 4. The bit MD9 determine the operating frequency of Booster Circuit. According to the frequency of Input CLK at pin 10, the value of MD9 should be chosen as shown below.

CLK (at pin 10)	MD9
7.1 MHz to 10 MHz	0
4.0 MHz to 7.0 MHz	1

Input Data Register (A0 = 0)

Bit / DD0 to DD9: These input data are used to control the output current at VCM driver as shown follows.

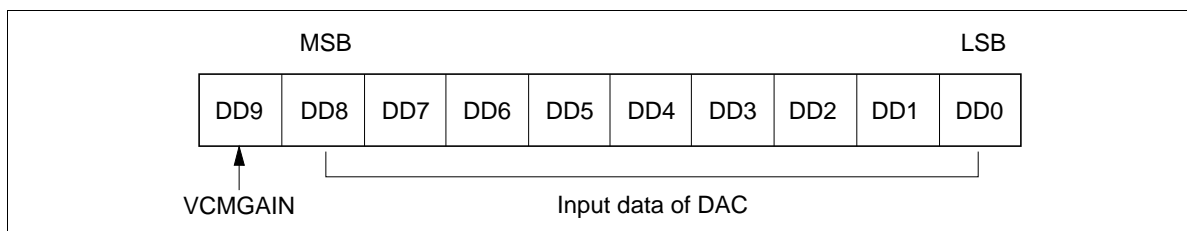


Figure 3 Input Data (2)

The data bit DD9 determine the transfer gain G_{VCM} which is specified as the relationship between the input data at the input data register and the output current at VCM amplifier. (See the under table)

DD9	DATA	I_o [mA]
1	1FF	$+199.2/R_s$
1	100	0.000
1	000	$-200.0/R_s$
0	1FF	$+24.9/R_s$
0	100	0.000
0	000	$-25.0/R_s$

Data Input Timing

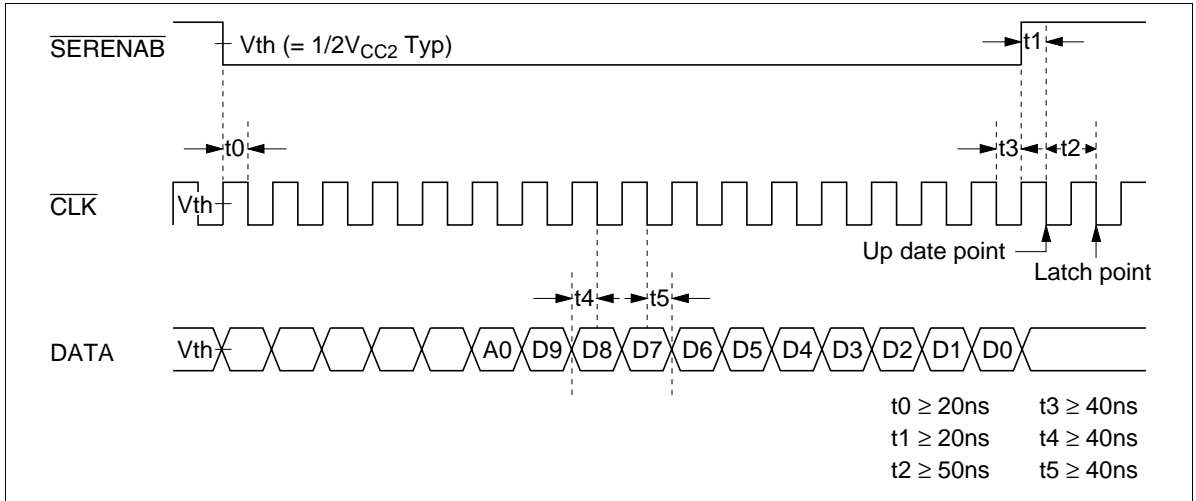


Figure 4 Input Timing on Serial Port

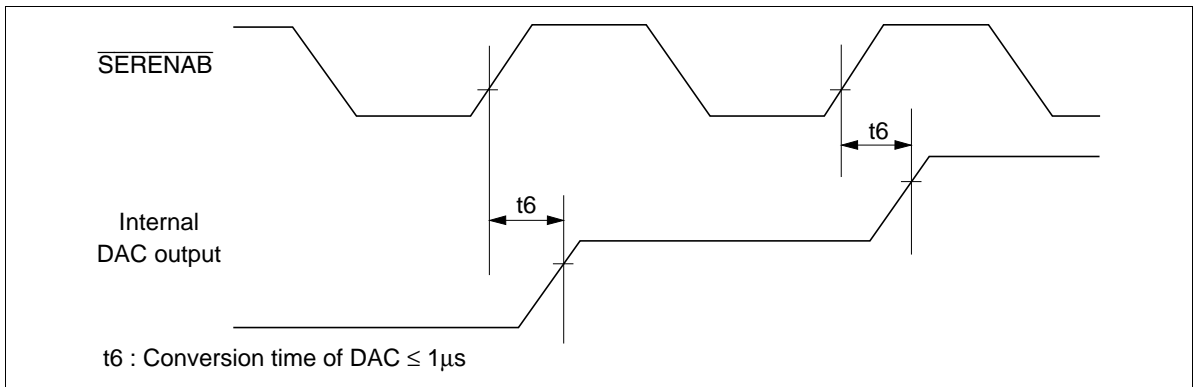
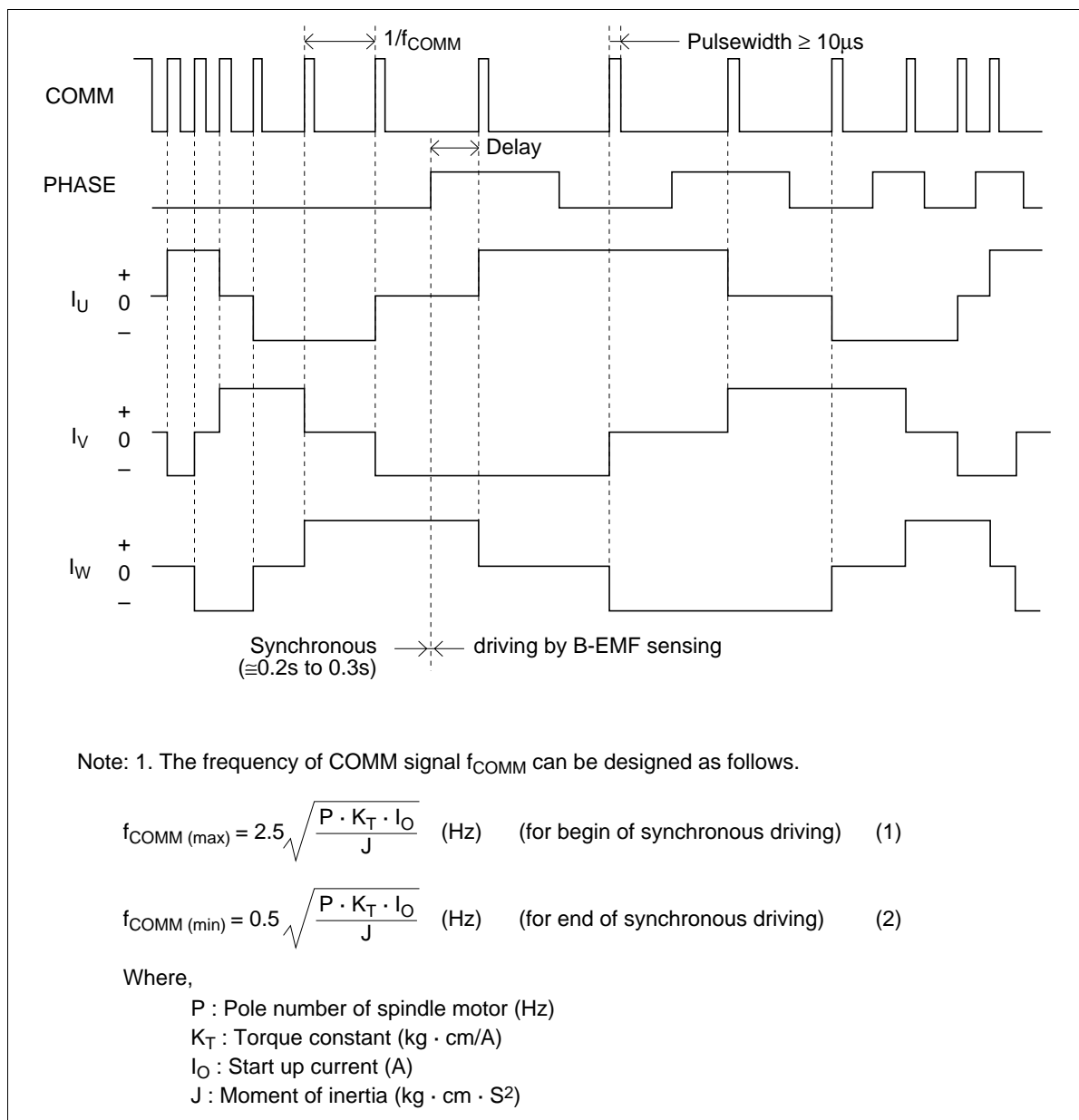


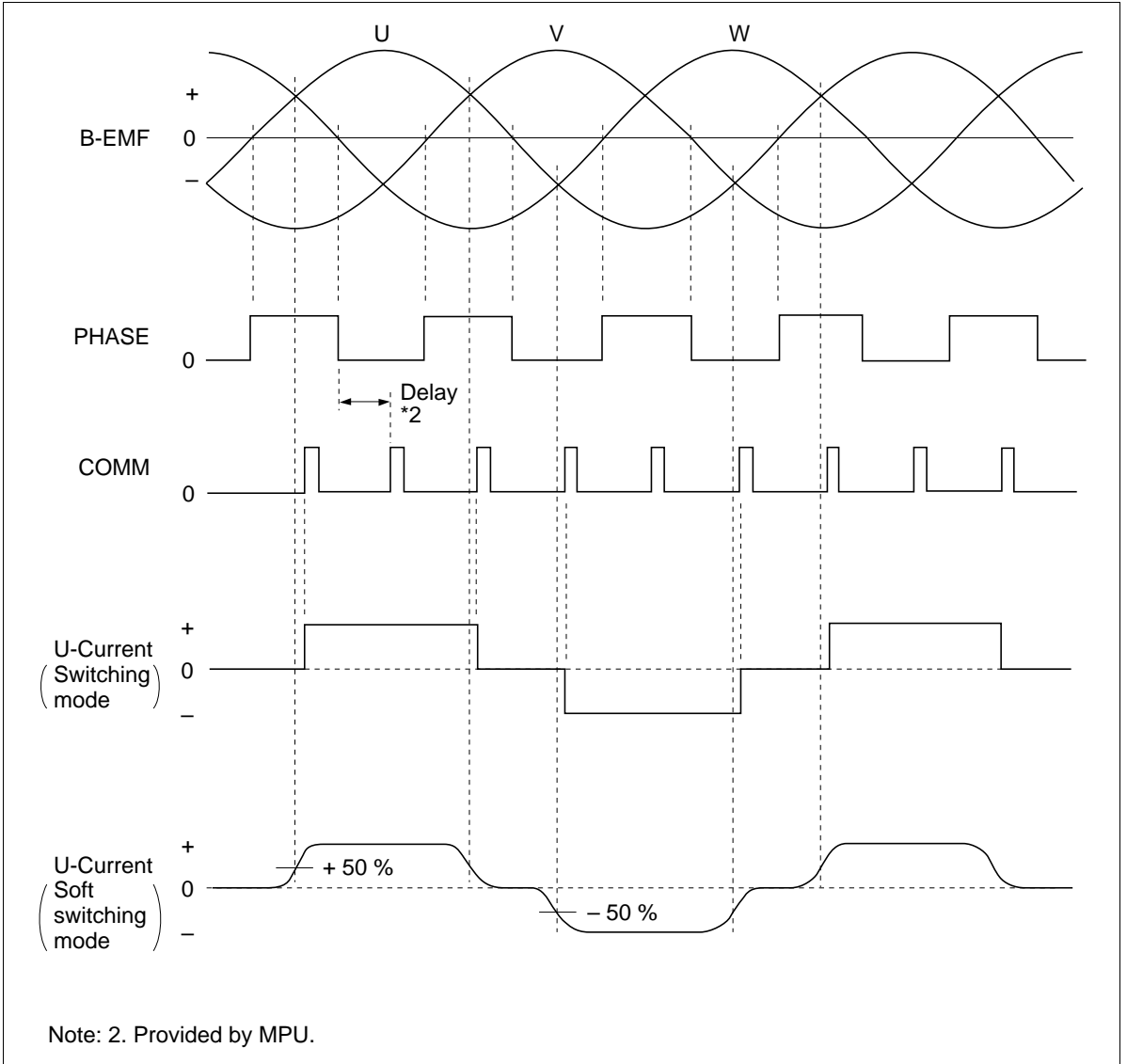
Figure 5 Conversion Timing on DAC

Commutation Timing

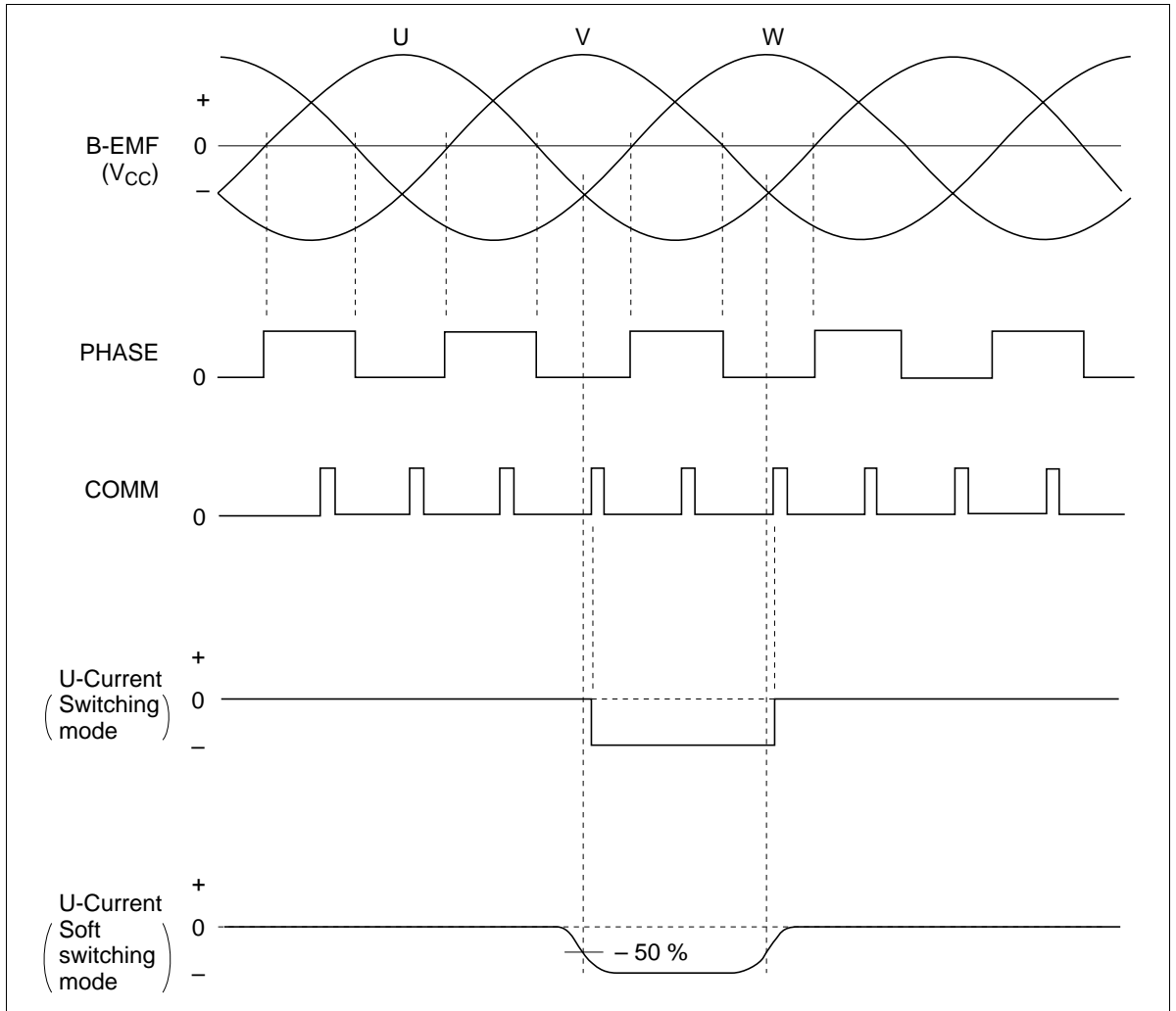
Commutation for starting up



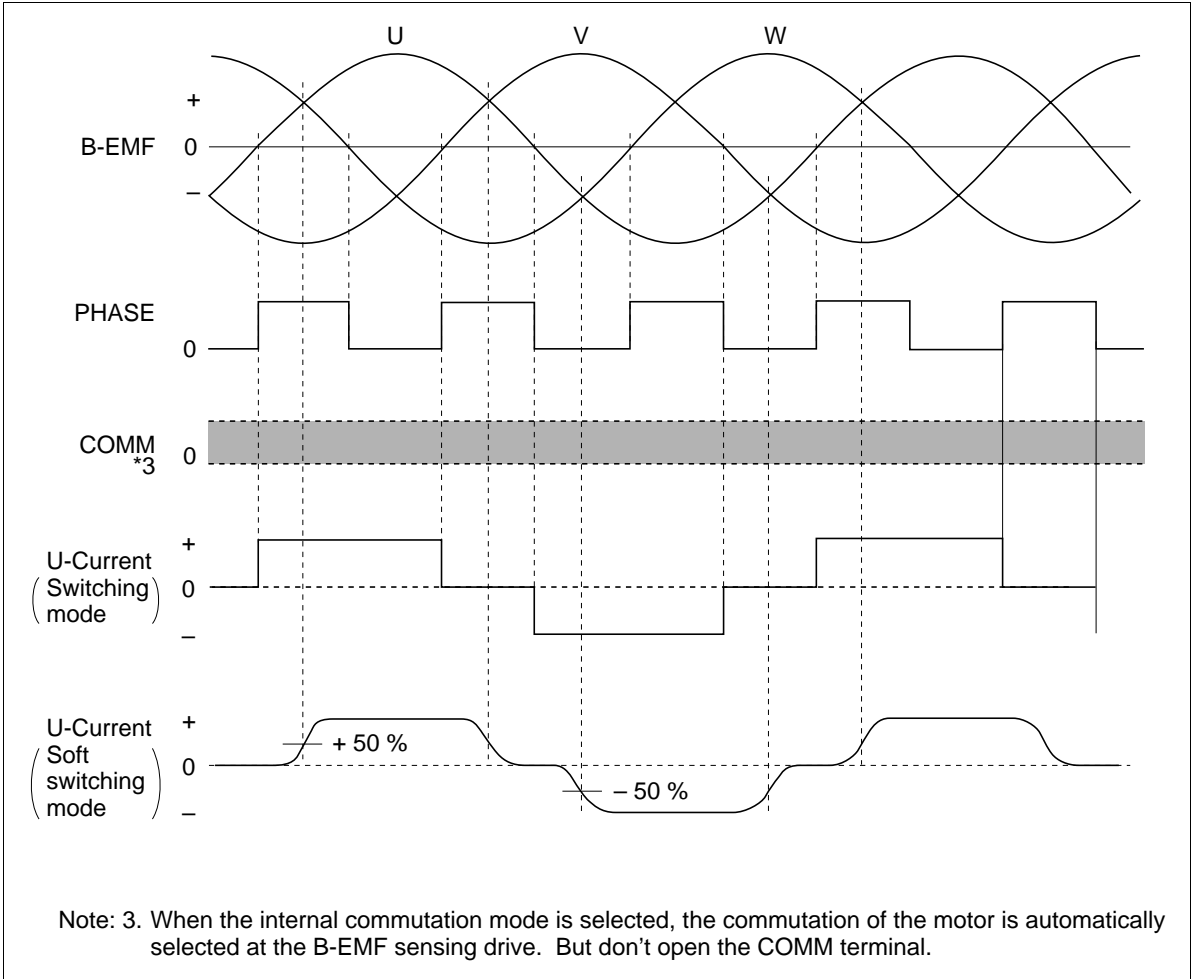
External Commutation Mode (Full Wave Drive)



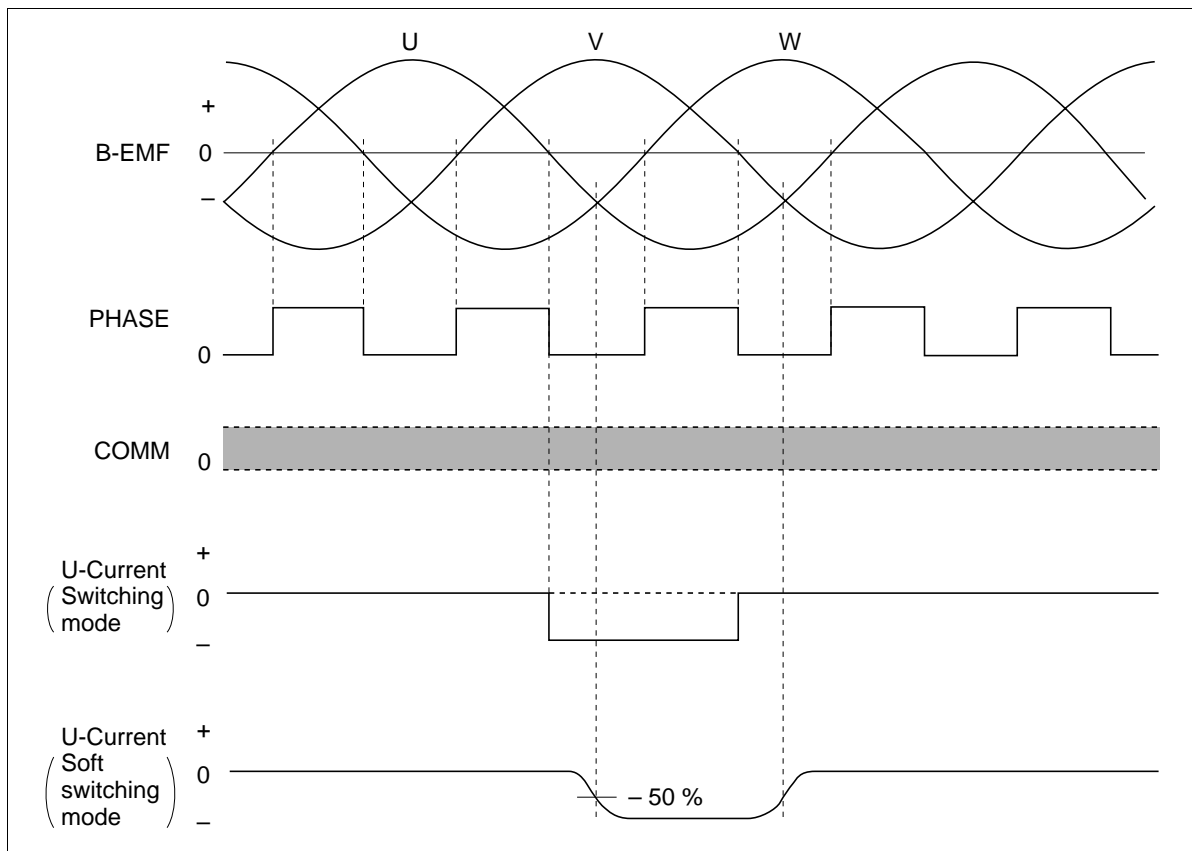
External Commutation Mode (Half Wave Mode)



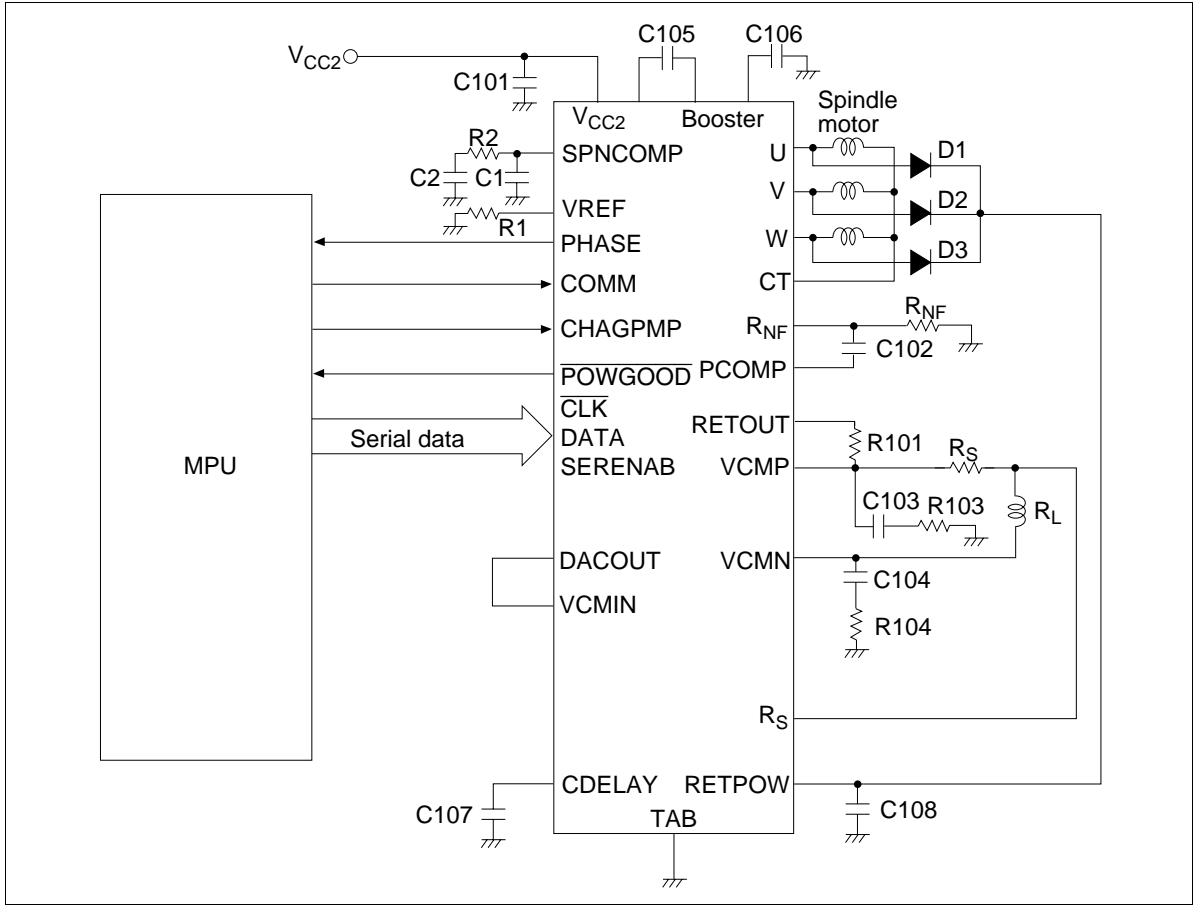
Internal Commutation Mode (Full Wave Mode)



Internal Commutation Mode (Half Wave Mode)



Application



External Component

Parts No.	Recommended Value	Purpose	Notes
R ₁	≤ 47 kΩ	Integral constant	1
R ₂	—	Integral constant	1
R ₁₀₁	—	Set retract current	2
R ₁₀₃ , R ₁₀₄	2.2 Ω	For stability	
R _{NF}	≥ 0.2 Ω	Spindle current sense	3
R _S	0.47 Ω	VCM current sense	
C ₁ , C ₂	—	Integral constant	1
C ₁₀₁	0.1 μF	Power supply bypass	
C ₁₀₂	0.1 μF	Phase compensation for spindle driver	
C ₁₀₃ , C ₁₀₄	0.1 μF	For stability	
C ₁₀₅	0.47 μF	For booster	
C ₁₀₆	4.7 μF	For booster	
C ₁₀₇	—	POR delay	4
C ₁₀₈	—	Retpower filter	
D1, D2, D3	—	For retract	

Notes: 1. This integral constants can be designed as follows.

$$\omega_0 = \frac{2\pi N_0}{600} \quad (3)$$

$$\frac{R_2}{R_1} = \frac{J \omega_0 N_0 R_{NF}}{9.55Kt Gctl Vref2} \quad (4)$$

$$C_1 = \frac{1}{\sqrt{10} \omega_0 R_2} \quad (5)$$

$$C_2 = 10C_1 \quad (6)$$

Where,

ω_0 = Time constant of servo loop

N_0 = Rotation number (rpm)

J = Moment of inertia (kg cm•s²)

R_{NF} = Current sense resistor (Ω)

$Gctl$ = Control gain (see electrical characteristics)

$Vref2$ = Internal reference voltage (See electrical characteristics)

2. The retract current is determined as follows.

$$I_{ret} = \frac{V_{retpow} - V_{satret}}{R_{101} + R_L + R_S} \quad (7)$$

where,

R_L = VCM coil Resistor.

V_{satret} = Retout saturation voltage (See electrical characteristics)

3. The motor start up current I_O is determined as follows.

$$I_O = \frac{V_{ref1}}{R_{NF}} \quad (A) \quad (8)$$

Where, V_{ref1} = Current limiter reference voltage

(See electrical characteristics)

4. The power on reset delay time is determined as follows.

$$t_{POR} = 10^5 \cdot C_{107} \quad (\text{See electrical characteristics}) \quad (9)$$

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Value	Units	Notes
Power supply voltage	V_{CC2}	7.0	V	1
Spindle current	I_{spn}	1.0	A	2
VCM current	I_{vcm}	400	mA	2
Retract current	I_{ret}	100	mA	2
Input voltage	V_{in}	0 to V_{CC}	V	
Power dissipation ($T_a = 65^\circ\text{C}$)	P_{T1}	1.0	W	3
Power dissipation ($T_c = 100^\circ\text{C}$)	P_{T2}	2.0	W	3
Junction temperature	T_j	150	$^\circ\text{C}$	4
Storage temperature range	T_{stg}	-55 to +125	$^\circ\text{C}$	

- Notes: 1. Operating voltage range is 4.25 V to 5.75 V.
 2. ASO of each output transistor is shown below. Operating locus must be within the ASO.
 3. Thermal resistance is shown below.
 $\theta_{j-c} \leq 25^\circ\text{C/W}$
 $\theta_{j-a} \leq 80^\circ\text{C/W}$
 4. Operating junction temperature range is 0 to +125 $^\circ\text{C}$.

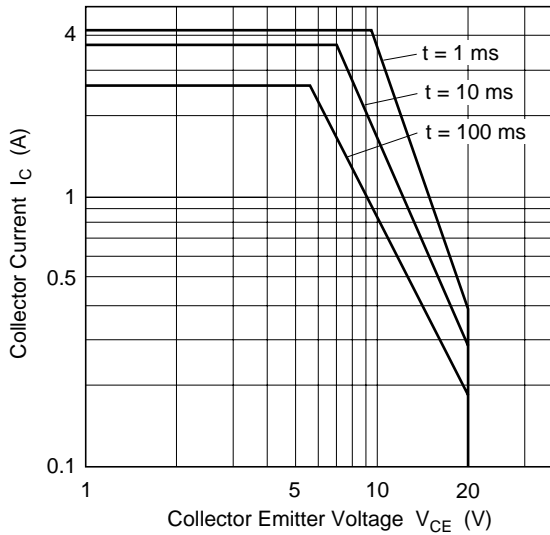


Figure 6 ASO of Output Transistor (Spindle Driver)

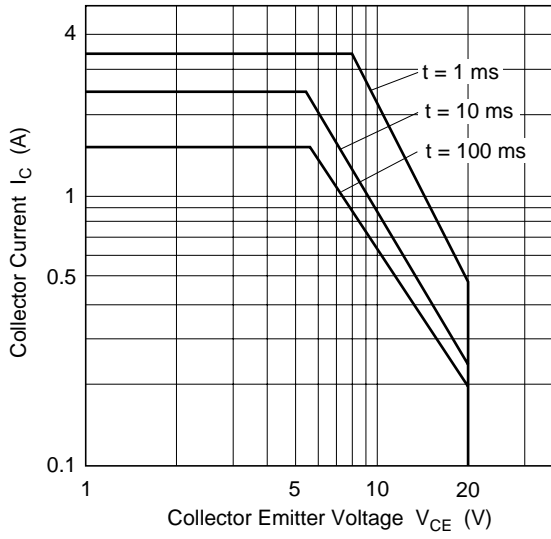


Figure 7 ASO of Output Transistor (VCM Driver)

Electrical Characteristics (Ta = 25°C, V_{CC} = 5 V)

Item	Symbol	Min	Typ	Max	Units	Test Conditions	Applicable Terminal	Note		
Supply current	I _{CC1}	—	15	20	mA	Enablemode	3			
Logic input	Input low current	I _{IL}	—	0	±10	μA	V _{IL} =0V	8, 9, 10, 11		
	Input high current	I _{IH}	—	—	±10	μA	V _{IH} =5V			
	Input low voltage	V _{IL}	—	—	1.5	V				
	Input high voltage	V _{IH}	3.5	—	—	V				
	Clock frequency	f _{CLK}	—	—	10	MHz				
Logic output	Output high voltage	V _{OH}	4.4	—	—	V	I _{OH} =1mA	7, 13		
	Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} =1mA			
Spindle driver	Total saturation voltage	Vsatspn	—	1.0	1.4	V	I _{spn} =0.8A	1, 25, 26		
			—	0.2	0.3	V	I _{spn} =100mA			
	Output leak current	I _{cer1}	—	—	5	mA	MD3=1, V _O =V _{CC} +3V			
	Current limiter reference voltage	V _{ref1}	139	155	171	mV	R _{NF} =1.0Ω			
	Current control gain	G _{ctl}	-14	-12	-10	dB				
B-EMF amps	Input sensitivity	V _{min}	—	50	—	mVp-p	1, 25, 26	1		
Charge pump	Input high voltage	V _{IHCP}	3.5	—	—	V		12		
	Input low voltage	V _{ILCP}	—	—	1.5	V				
	Input high current	I _{IHCP}	—	150	200	μA	V _{IHCP} =5V			
	Input dead current	I _{IDCP}	—	—	±10	μA				
	Input low current	I _{ILCP}	—	-150	-200	μA	V _{ILCP} =0V			
	Output current	Charge current		+44	+54	+64	μA		R1=24kΩ	17
		Discharge current		-64	-54	-44	μA		R1=24kΩ	
	Output cutoff current	I _{off}	—	—	±50	nA				
	Reference voltage	V _{ref2}	1.32	1.39	1.46	V	R1=24kΩ	16		
VCM driver	VCM input resistor	R _{in}	42	60	78	kΩ		2		
	Output quiescent voltage	V _q	V _{CC2} /2	V _{CC2} /2 +5%	V _{CC2} /2 +10%	V		22, 23		
	Output leak current	I _{cer2}	—	—	±5	mA				
	Total output saturation voltage	V _{satvcm}	—	1.0	1.35	V	I _{vcm} =400mA			
			—	0.8	1.0	V	I _{vcm} =200mA			

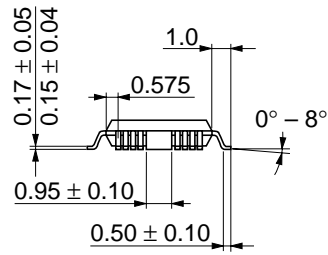
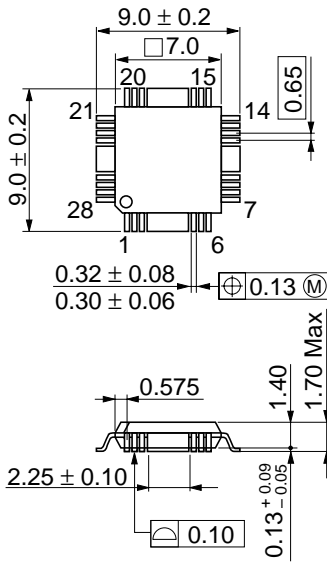
Electrical Characteristics (Ta = 25°C, V_{CC} = 5 V) (cont)

Item		Symbol	Min	Typ	Max	Units	Test Conditions	Applicable Terminal	Note
VCM	Resolution	I _{res}	—	1/512	—	—		21, 22, 23	1
driver	DAC output resistor	R _{out}	—	—	50	Ω		14	
	Output current full scale	I _{FS1}	345	385	425	mA	DD9=1, R _S =	2, 14	2
		I _{FS2}	45	50	55	mA	1Ω, R _L =14Ω		
	Gain ratio	I _{FS1} / I _{FS2}	7.5	8.0	8.5	—			
	Offset	I _{off1}	—	—	±15	LSB	DD9=1, R _S =	21, 22, 23	
		I _{off2}	—	—	±20	LSB	1Ω, R _L =14Ω		
		I _{off3}	—	—	±80	LSB	I _{off1} ×8–I _{off2}		
Linearity	I _{LIN}	—	—	±1	LSB				
Gain Bandwidth	B		—	40	—	kHz	DD9=1, R _S = 1Ω, R _L =14Ω		1
			—	95	—	kHz	DD9=0, R _S = 1Ω, R _L =14Ω		
Retract driver	Retpow voltage	V _{retpow}	1.4	—	—	V	R _S =1.0Ω, R _L =14Ω I _{ret} =100mA	18	
	Retout saturation voltage	V _{satret}	—	1.0	1.2	V	I _{ret} =100mA	19	
LVI	Operating voltage	V _{sd}	3.55	3.85	4.15	V		3	
	Recovery voltage	V _{rec}	3.9	4.2	4.5	V			1
POR	Power on reset delay time	POR	5	10	20	ms	C ₁₀₇ =0.1μF	13	
OTSD	Operating temperature	T _{sd}	125	150	—	°C			1
	Hysteresis	Thys	—	25	—	°C			

- Note: 1. Design guide only
 2. Specified by shorting between VCMIN and DACOUT.

Package Dimensions

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-28T
JEDEC	—
EIAJ	—
Weight (reference value)	0.2 g

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