HA13563, HA13563V

Three-Phase Brushless Motor Driver

HITACHI

ADE-207-218A (Z) 2nd Edition December 1998

Description

The HA13563/V are 3-phase brushless motor driver ICs with digital speed control. It is designed for use as a PPC or LBP drum motor driver and provides the functions and features listed below.

Functions

- Three-phase brushless motor driver
- Direct PWM drive
- Digital discriminator plus PLL speed control
- Speed monitor
- Stuck rotor protection
- Current limiter
- Thermal protection (OTSD)
- Low voltage inhibit (LVI)

Features

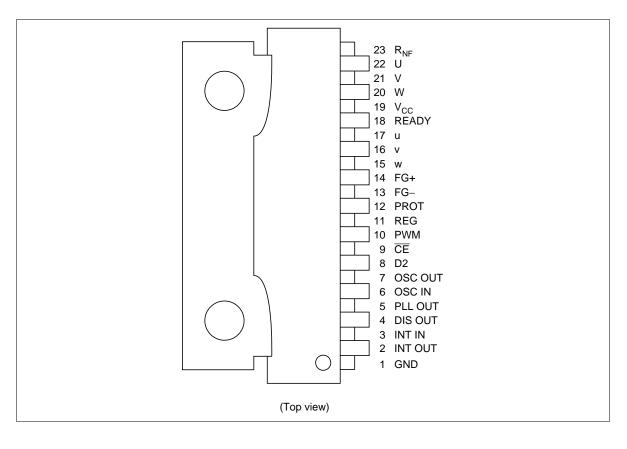
- Low saturation voltage
- Fly wheel diodes built-in
- FG signal digital filter built-in

Ordering Information

Product No.	Package
HA13563	SP-23TA
HA13563V	SP-23TB



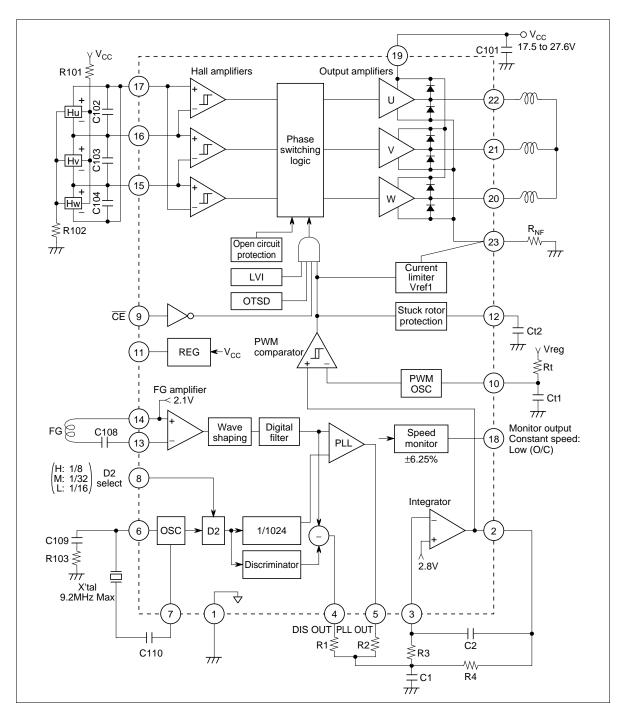
Pin Arrangement



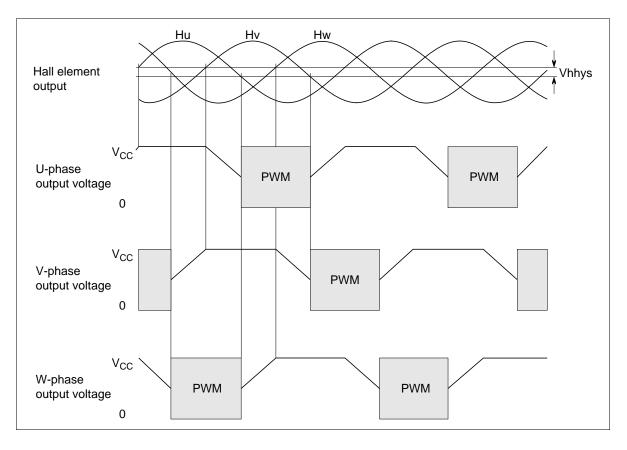
Pin Functions

Pin No.	Pin Name	Function
1	GND	Ground
2	INT OUT	Integrator output
3	INT IN	Integrator input
4	DIS OUT	Speed discriminator output
5	PLL OUT	PLL output
6	OSC IN	Clock oscillator input. Apply the external clock signal to this pin.
7	OSC OUT	Clock oscillator output. Use this pin to monitor the oscillator waveform.
8	D2	Clock divider selector input High: 1/8, Middle or Open: 1/32, and Low: 1/16.
9	CE	Chip enable input High or Open: stop, Low: drive on.
10	PWM	PWM carrier oscillator. An external capacitor to charge and discharge, and an external resistor must be provided.
11	REG	5 V fixed voltage output. Always output regardless of the state of the \overline{CE} input.
12	PROT	An external capacitor sets the time until the stuck rotor protection circuit operates. If this pin is shorted to ground, the protection circuit will not operate. After the stuck rotor protection circuit operates, the IC can be reset by turning the power off and then on again, or switching \overline{CE} from low to high.
13	FG–	FG amplifier – input.
14	FG+	FG amplifier + input. This pin is used for temperature monitoring. See the reference data.
15	W	The w+ and v– Hall amplifier input
16	V	The v+, u– Hall amplifier input
17	u	The u+, w– Hall amplifier input
18	READY	Speed monitor output. Outputs a low level during fixed speed drive. This is an open collector output.
19	V _{cc}	Power supply
20	W	W-phase output
21	V	V-phase output
22	U	U-phase output
23	R _{NF}	Current detector. Connect a current detection resistor to this pin.

Block Diagram



Timing Chart



External Components

Part No.	Recommended Value	Purpose	Note
R1 to R4	_	Integration constant	1
R101, R102	—	Hall element bias	2
R103	1 kΩ	Clock oscillator stabilization	9
R _{NF}	—	Current detection	3
Rt	—	PWM carrier oscillator time constant	6
C1, C2	_	Integration constant	1
C101	≥ 0.1 μF	Power supply bypass	4
C102, C103, C104	0.047 μF	Stabilization	4
C108	_	FG coupling	5
C109	0.047 μF	Clock oscillator stabilization	9
C110	10 pF	Crystal coupling	9
Ct1	1000 pF	PWM carrier oscillator time constant	6
Ct2	_	Stuck rotor protection circuit time constant	7
X'tal	_	Reference oscillator	8

Notes: 1. Determine the component values using the following as a guidline: First determine the angular frequency of ω_P for DIS OUT and PLL OUT.

$$\omega_{\rm P} = 2\pi \cdot \text{ffg} \text{ [rad/sec]}$$

(1)

Determine the the angular frequency of $\omega_{\!\scriptscriptstyle P}$ for motor.

 $\omega_{M} \approx \frac{9.55}{N_{O}} \cdot \frac{1}{J} \left(K_{T} \cdot \frac{Vref1}{R_{NF}} - T_{L} \right) \text{ [rad/sec]}$ (2)

Determine the ω_o .

$$\omega_{\rm O} = \sqrt{\omega_{\rm P} \cdot \omega_{\rm M}} \quad [\rm rad/sec] \tag{3}$$

Determine the integrator's DC gain G_(E).

$$G_{(E)} = \frac{J \cdot \omega_{O}}{9.55 \cdot K_{T} \cdot A} \cdot \frac{1}{\frac{Z}{60} \cdot 2\pi \cdot \frac{K \emptyset}{\omega_{O}}}$$
(4)

where, k ϕ : PLL gain = 0.4 (V/rad/sec) A = $\frac{2 V_{CC} - 0.83 \cdot V_E - V_{Sat}}{Rm \cdot V_{OSC}}$

- Z : FG pulse per round (P/R)
- N_{o} : Motor speed (min⁻¹)

ω_o : Control loop angular frequency (rad/sec)

ffg : FG frequency (Hz)

J : Moment of inertia of the motor (kg m²)

Rm : Motor coil resistance ($\Omega/T-T$)

(5)

K_τ : Torque constant (N•m/A) T, : Rated load torque (N•m) : PWM carrier oscillator amplitude (V_{PP}, See the Electrical Charasteristics) Vosc VF : Motor back EMF (V_{PP}/T–T) : Current detection resistor (Ω) R_{NF} Vref1 : Current limiter reference voltage (See the Electrical Charasteristics) Vsat : Saturation voltage (See the Electrical Charasteristics) Set C2 and derive the integration constants from the following formulas. $R4 = \frac{1}{\omega_P \cdot C2}$

$$R2 = \frac{R4}{G_{(E)}}$$
(6)

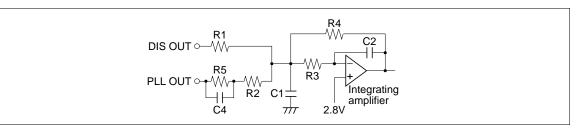
$$C1 = \frac{1}{2 \cdot R2 \cdot \omega_0}$$
(7)

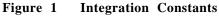
Next, determine R1 to match the phase of PLL output.

$$R1 = \frac{1.89 \cdot R4}{1.6 - 0.33 \cdot R4 / R2}$$
(9)

When log $\omega_{\rm e}/\omega_{\rm M}$ is greater than 2, a phase advance to compensate for this phenomenon is required. Use the following formula to set the phase advance:

$$\frac{1}{C4 \cdot R5} < \frac{\omega_{P}}{20 \cdot 2} \tag{10}$$





- 2. The Hall output bias voltage is determined by R101 and R102.
- 3. The output current is controlled according to the following formula:

 $lomax = \frac{Vref1}{2}$ R_{NF}

Where, Vref1 is the current limiter reference voltage. (See the Electrical Charasteristics) Mount this resistor as close as possible to the IC and use a resistor with a small inductance component.

4. Connect these components as close to the IC as possible.

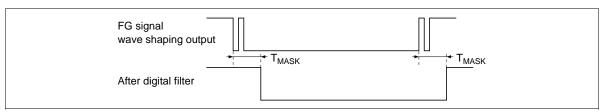
5. Determine the component value using the following formula as a guideline:

C108 (μ F) = $\frac{220}{\text{ffg (Hz)}}$

Digital filter time T_{MASK} of FG signal is determined as follows.

 $T_{MASK} (sec) = \frac{1}{CLK \times D2} \sim \frac{2}{CLK \times D2}$

where, CLK : The reference frequency. D2 : CLK frequency dividing ratio.

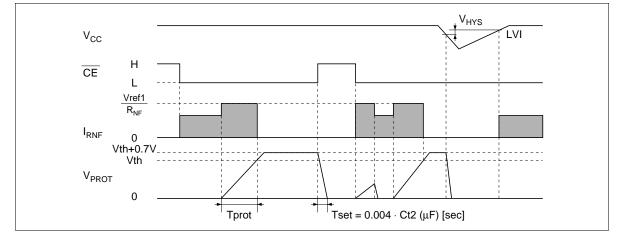


6. The PWM carrier frequency is determined roughly by the following formula:

 $f_{\text{PWM}} = \frac{1180}{\text{Rt} (\text{k}\Omega) \text{ Ct1 (pF)}} \times 10^3$

7. The formula shown below roughly determines the time, Tprot (s), until the stuck rotor protection circuit operates. Figure 2 shows the operating waveforms. The latched state can be cleared by either CE or V_{cc}. Note that a capacitor with a leakage current sufficiently smaller than the charging current lct+ must be used.

Tprot = 0.24 Ct2 (μ F)





8. The reference frequency CLK (Hz) and the FG frequency ffg (Hz) are related by the following formula:

 $\mathsf{CLK} = \frac{1024 \text{ ffg}}{\mathsf{D2}}$

Also note that the value of the resistor (Rosc) inserted between the external clock and pin 6 when an external clock is used can be calculated from the following formulas:

 $Rosc ≥ 2 (V_{IH} - 2.1) - 1.5 (kΩ)$

Rosc ≤ 6 (2.1 – V_{IL}) – 1.5 (kΩ)

where, V_{IH} : The clock driver high-level voltage.

 V_{IL} : The clock driver low-level voltage.

If an external clock signal is input to pin 6 through a capacitor (Cosc), we recommend using a 10 pF capacitor for Cosc.

9. The relationship with CLK crystal oscillator frequency refer to the following.

Oscillator	fc	C110	C109	R103
Crystal	6.0 to 9.2 MHz	10 pF	0.047 μF	1 kΩ
	2.0 to 6.0 MHz	10 pF	Uselessness	Uselessness

Absolute Maximum Ratings (Ta = 25°C)

ltem	Symbol	Rating	Unit	Note
Power supply voltage	V _{cc}	30	V	1
Instantaneous output current	Іор	3.0	А	2
Steady-state output current	I _o	2.0	А	2
Input voltage	Vi	–0.3 to 7	V	3
Allowable power dissipation	P _T	10	W	4
Junction temperature	Tj	150	°C	1
Storage temperature Tstg		–55 to +125	° C	

Notes: 1. The operating ranges are as follows:

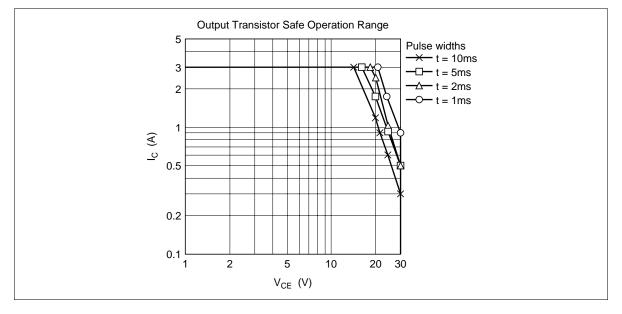
 V_{cc} = 17.5 to 27.6 V

Tjop = −20 to +125°C

- 2. See the safe operating range data.
- 3. Applies to the logic input pins.
- 4. The allowable value when the TAB temperature, Ttab, is 120°C. However, the thermal resistance is as follows:

 θj -c $\leq 3^{\circ}C/W$

 θ j-a $\leq 40^{\circ}$ C/W



Electrical Characteristics (Ta = 25° C, V_{CC} = 24 V)

ltem		Symbol	Min	Тур	Max	Unit	Test Conditions	Applicable Pins
Current	Standby current	I _{cco}	_	8	11	mA	$\overline{\text{CE}}$ = H, V _{CC} = 30 V	19
drain	Current drain with outputs off	I _{cc}	_	32	44	mA	$\overline{\text{CE}}$ = L, Pin 3 = H, V _{CC} = 30 V, output OFF	-
Logic	Low-level voltage	Vil1	_	_	0.8	V		9
input 1	High-level voltage	Vih1	2.0	_	_	V		-
	Low-level current	lil1	_	-0.25	-0.35	mA	Vil = 0 V	-
	High-level current	lih1	-0.1	0	0.1	mA	Vih = 7 V	-
Logic	Low-level voltage	Vil2	_	_	1.0	V		8
input 2	Middle-level voltage	Vim	2.0	2.5	3.0	V		-
	High-level voltage	Vih2	4.0	_	_	V		-
	Low-level current	lil2	_	-0.25	-0.35	mA	Vil = 0 V	-
	Middle-level current	lim	_	—	±35	μΑ	Vi = 2.5 V	-
	High-level current	lih2	—	0.5	0.7	mA	Vih = 7 V	-
Logic	Low-level voltage	Vol1	_	0.2	0.4	V	lol = 2 mA	18
output	Leakage current	loh1	_	_	±10	μΑ	Voh = 30 V	
Hall amplifier	Commonmode input voltage range	Vh	2.0	_	V _{cc} -2	V		15, 16, 17
	Differentialmode input voltage range	Vd	60	_	V _{cc} /2	mV		-
	Hysteresis *1	Vhhys	—	20	_	mV	$Rh = 400 \Omega$	-
Output	Leakage current	lcer	_	_	±100	μΑ	Vce = 30 V	20, 21, 22
amplifier	Output drive current	I _{B1}	_	49	64	mA	I ₀ = 2 A	-
		I _{B2}	—	35	46	mA	I ₀ = 1 A	-
	Saturation voltage *2	Vsat1	_	1.8	2.7	V	$I_0 = 2 A$	-
		Vsat2	—	1.35	1.7	V	I ₀ = 1 A	-
	Impulse response	tphl	—	_	2	μs		-
	time	tplh	_	_	2	μs		-
		tr	_	—	0.5	μs		-
		tf	_	_	0.5	μs		-
	Current limiter reference voltage	Vref1	0.45	0.5	0.55	V		23
Flywheel	Forward voltage	V _F	_	1.15	1.4	V	I _F = 1 A	19, 20, 21,
diode	Substrate current	Isub	_	6.5	10	%		22

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V) (cont)

ltem		Symbol	Min	Тур	Max	Unit	Test Conditions	Applicable Pins
PWM oscillator	Oscillator frequency range	f _{PWM}	2.0	—	30	kHz		10
and PWM comparator	Oscillator frequency precision	ferr	11.7	13	14.3	kHz	Rt1 = 91 kΩ, Ct1 = 1000 pF	_
	Oscillator high-level voltage	Vosch	2.7	3.0	3.3	V		_
	Oscillator low-level voltage	Voscl	1.0	1.1	1.2	V		_
	Oscillator amplitude	Vosc	1.7	1.9	2.1	V _{PP}	Vosch – Voscl	
	Comparator hysteresis *1	Vchys	_	20	_	mV		2
Integrator	Input current	lin	_	_	±250	nA		2, 3
	High-level voltage	Voh2	3.2	3.5	_	V	I _o = -0.5 mA	
	Low-level voltage	Vol2	—	0.9	1.1	V	l _o = 0.5 mA	
	Voltage gain *1	Gi	—	60	—	dB		
	Gainbandwidth produc t *1	Bi	_	0.5	_	MHz		
	Reference voltage	Vp	2.65	2.8	2.95	V		
FG amplifier and	Input sensitivity	vfg	15	_	1000	$\mathrm{mV}_{\mathrm{PP}}$		13, 14
waveform shaping	Noise margin	nd	_	_	4.0	$\mathrm{mV}_{\mathrm{PP}}$		
		nc	—	—	1.0	V _{PP}		
PLL, DIS	Ouput high-level voltage	Voh3	4.3	4.5	_	V	I _o = -0.1 mA	4, 5
	Ouput low-level voltage	Vol3	_	—	0.25	V	l _o = 0.1 mA	_
OSC	Oscillator frequency range	f _{osc}	2	—	9.2	MHz		6, 7
	Oscillator frequency error *1	$\Delta f_{\rm OSC}$	—	_	±0.01	%	X'tal	_
Speed discriminator and monitor	Number of counts	Ν	_	1023	_	Count		
	Operating frequency range	CLK	—	—	1.15	MHz		
	Lock range	LR	_	±6.25	_	%		18

Electrical Characteristics (Ta = 25°C, V_{CC} = 24 V) (cont)

ltem		Symbol	Min	Тур	Max	Unit	Test Conditions	Applicable Pins
REG	Output voltage	Vreg	4.65	5.0	5.35	V	Ireg = 20 mA, \overline{CE} = L	11
	Power supply regulation	$\Delta Vreg1$	—	20	100	mV	$V_{CC} = 17.5 \text{ to } 27.6 \text{ V},$ $\overline{OE} = \text{L}$	
	Load regulation	∆Vreg2	_	10	100	mV	Ireg = 0 to 20 mA, $\overline{OE} = L$	
Stuck rotor protection circuit	Ct2 charge current	lct+	18.5	23	27.5	μΑ	V _{PROT} = 2.5 V	12
	Ct2 discharge current	lct-	1.0	1.4	_	mA		
	Threshold voltage	Vth	4.5	5.0	5.5	V		
LVI	Operation cleaning voltage *3	VLVI	12.5	14.7	16.9	V		19
	Hysteresis	Vhys	0.75	1.1	1.45	V		
OTSD	Operating temperature *1	Tsd	125	150	175	°C		
	Hysteresis *1	Thys	_	20	_	°C		

Note: 1. These are design target values and only checked during development.

2. Stipulated ad the sum of the source and sink values.

3. See figure 3.

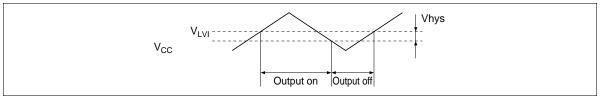
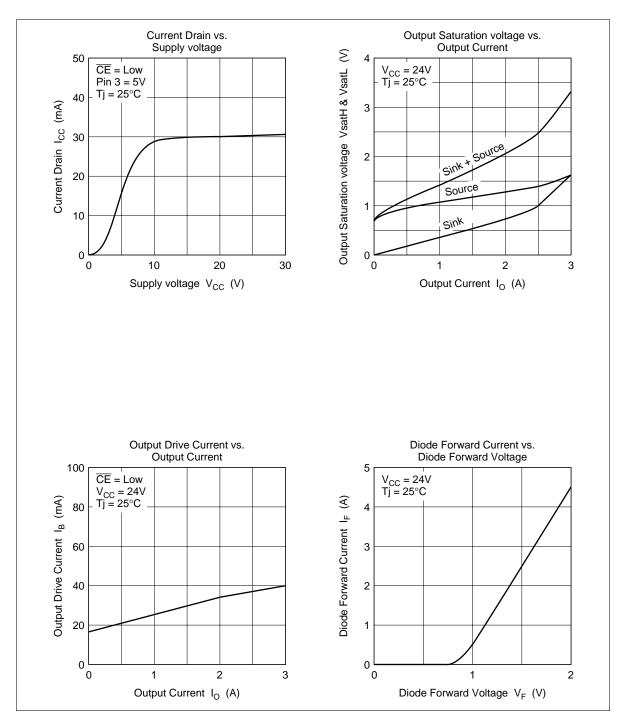
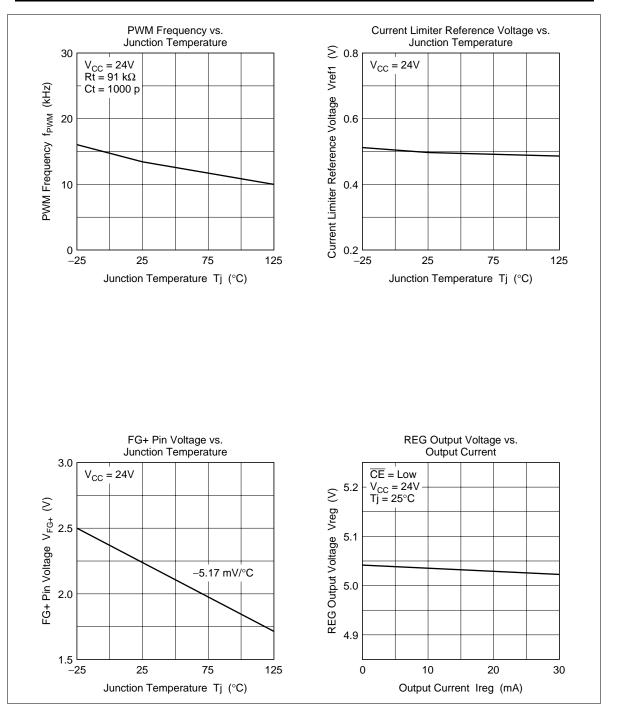


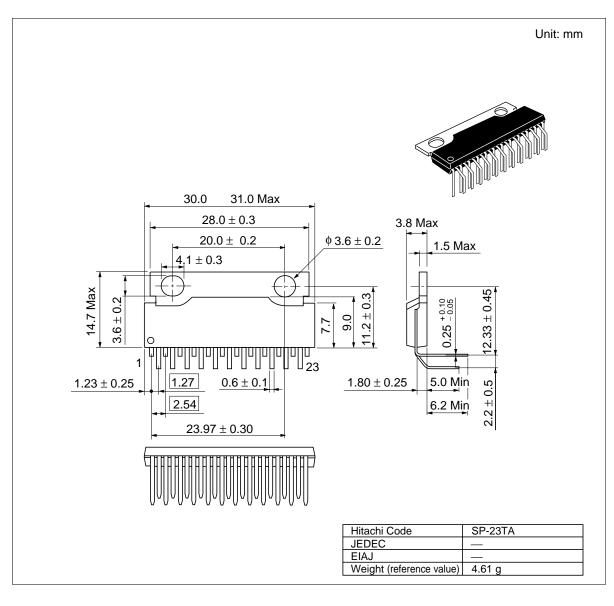
Figure 3

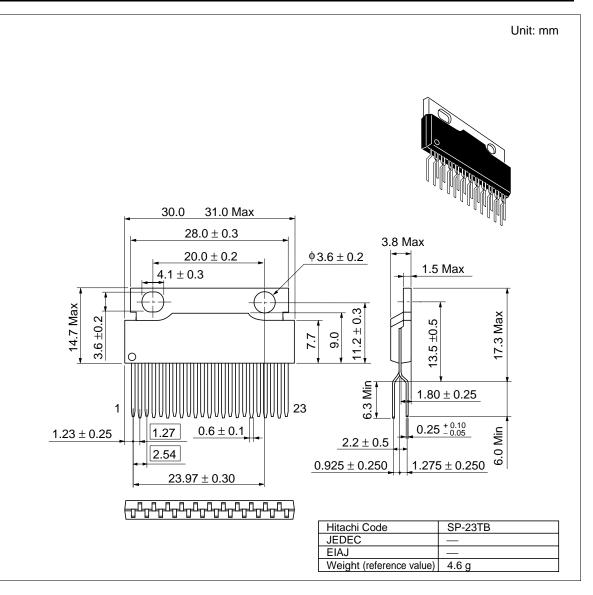
Reference Data





Package Dimensions





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