
HA13568AT

CD-ROM Combo Driver

HITACHI

ADE-207-261A (Z)
2nd Edition
December 1998

Description

The HA13568AT is combination of Spindle, Focus, Tracking, Slide, Tray designed for CD-ROM and have following functions and features.

Features

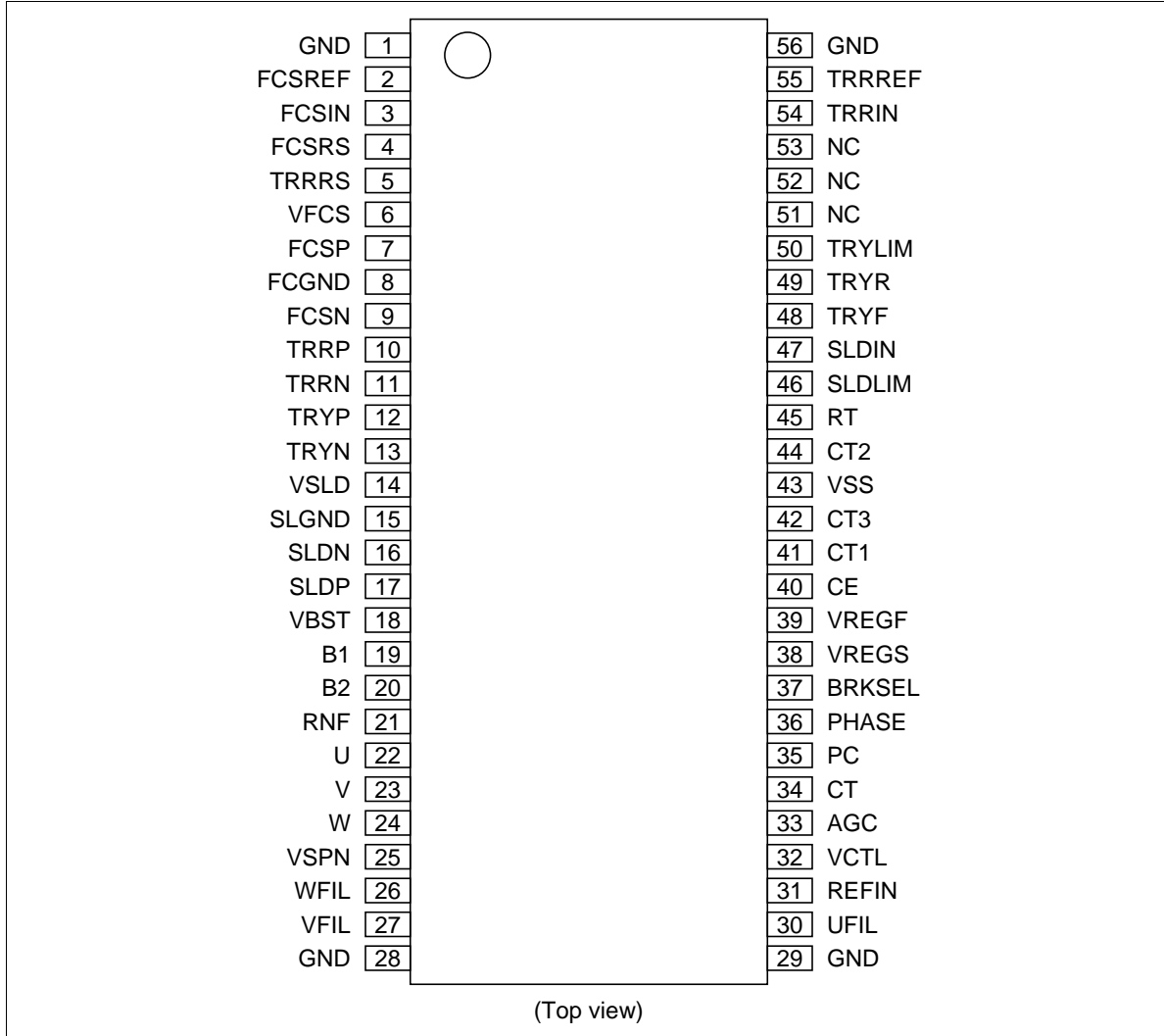
- 1.5 A sensorless spindle driver
- 0.5 A BTL focus driver
- 0.5 A BTL tracking driver
- 1.5 A H bridge slide motor driver
- 0.5 A H bridge tray motor driver
- Over temperature shut down (OTSD)
- Voltage regulator control circuit

Functions

- Sensorless driver with self start
- Soft switching drive
- Snubberless
- Low output saturation voltage
- Direct PWM slide driver

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Pin Arrangement



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Pin Description

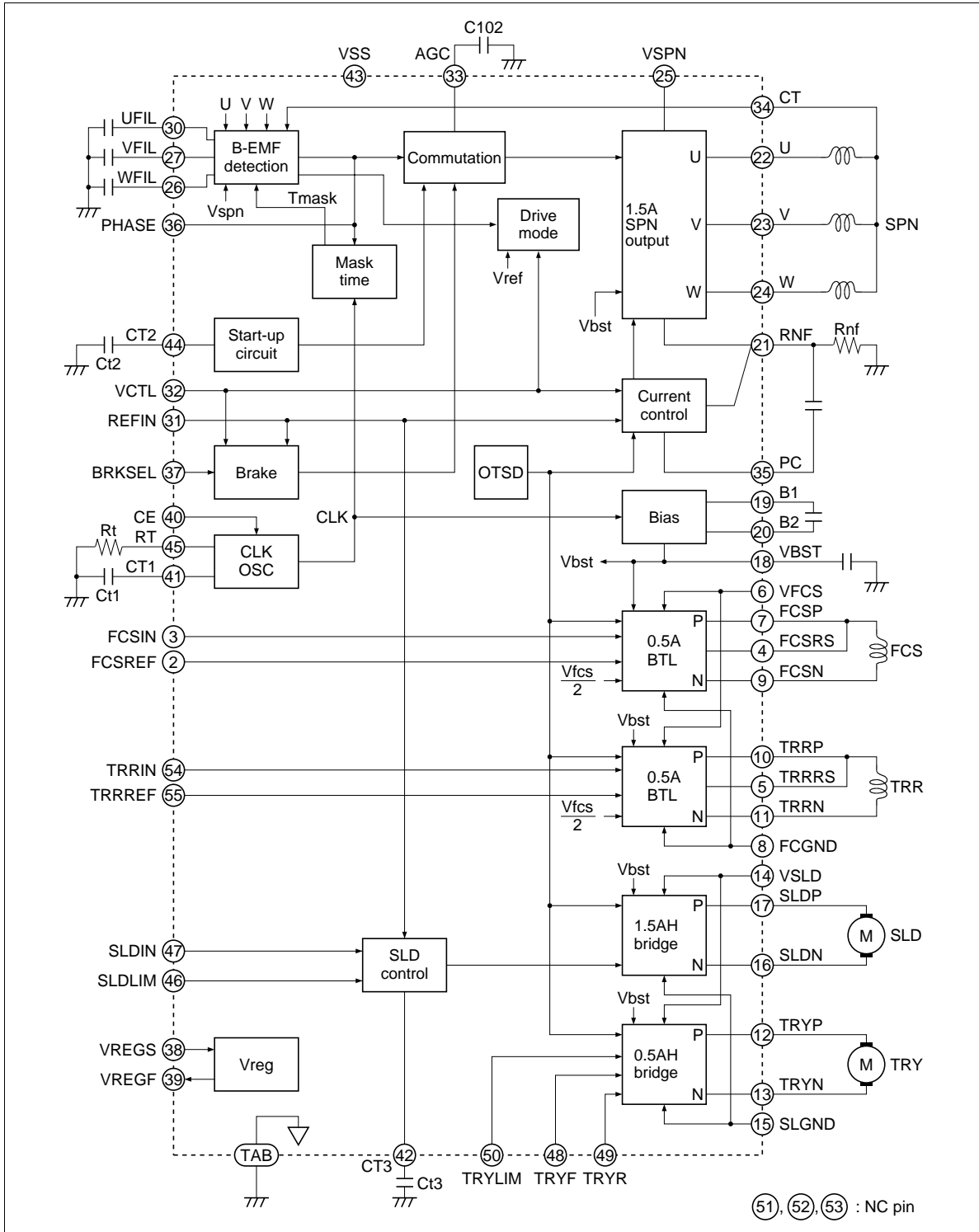
| Pin No. | Pin Name | Function |
|----------------|-----------------|--|
| 2 | FCSREF | FCS driver block reference voltage |
| 3 | FCSIN | FCS control input pin |
| 4 | FCSRS | FCS sense pin |
| 5 | TRRRS | TRR sense pin |
| 6 | VFCS | FCS driver and TRR driver power supply |
| 7 | FCSP | FCS driver P output |
| 8 | FCGND | FCS driver and TRR driver GND |
| 9 | FCSN | FCS driver N output |
| 10 | TRRP | TRR driver P output |
| 11 | TRRN | TRR driver N output |
| 12 | TRYP | TRY driver P output |
| 13 | TRYN | TRY driver N output |
| 14 | VSLD | SLD driver and TRY driver power supply |
| 15 | SLGND | SLD driver and TRY driver GND |
| 16 | SLDN | SLD driver N output |
| 17 | SLDP | SLD driver P output |
| 18 | VBST | Booster output pin. This circuit generates a voltage about 1.5 V above that of the VSPN pin. |
| 19 | B1 | Booster pumping capacitor connection |
| 20 | B2 | |
| 21 | RNF | Spindle driver current detection |
| 22 | U | U phase output |
| 23 | V | V phase output |
| 24 | W | W phase output |
| 25 | VSPN | Spindle and booster power supply |
| 26 | WFIL | W phase low pass filter. Connect a filter C to this pin during GND. |
| 27 | VFIL | V phase low pass filter. Connect a filter C to this pin during GND. |
| 30 | UFIL | U phase low pass filter. Connect a filter C to this pin during GND. |
| 31 | REFIN | Reference voltage of spindle and slide |
| 32 | VCTL | Spindle control input. Generates forward torque when a DC voltage higher than REFIN is applied, and brake when a DC voltage lower than REF is applied. |
| 33 | AGC | For AGC. Holds the level used for IC internal processing fixed even if the B-EMF level fluctuates due to the rotation speed. |
| 34 | CT | Spindle center tap |
| 35 | PC | Spindle driver phase compensation |

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Pin Description (cont)

| Pin No. | Pin Name | Function |
|--------------------|----------|---|
| 36 | PHASE | Outputs the B-EMF zero cross phase. Open corrector. (See the timing chart) |
| 37 | BRKSEL | To select the brake mode. Lo: Short brake, Hi: Reverse full brake (when forward torque input: BRKSEL = H) |
| 38 | VREGS | Voltage regulator sense pin (VREGS \approx 3.3 V output) |
| 39 | VREGF | Voltage regulator force pin |
| 40 | CE | Chip enable. Input Hi: active |
| 41 | CT1 | Time constant for clock oscillator circuit. The clock oscillator frequency is determined by the external capacitor and resistor Ct1 and Rt. |
| 42 | CT3 | Time constant for PWM carrier oscillator. The carrier frequency is determined by the external capacitor and resistor Ct3 and Rt. |
| 43 | VSS | Control block power supply. 5 V |
| 44 | CT2 | Time constant for start-up oscillator. The start-up oscillator frequency is determined by the external capacitor and resistor Ct2 and Rt. |
| 45 | RT | Reference voltage (3.3 V). The IC's internal reference current is determined by this voltage and the external resistor Rt. |
| 46 | SLDLIM | SLD output maximum duty setting |
| 47 | SLDIN | SLD control input pin |
| 48 | TRYF | TRY driver forward input |
| 49 | TRYR | TRY driver reverse input |
| 50 | TRYLIM | TRY output voltage setting pin |
| 51 | NC | No connection |
| 52 | NC | |
| 53 | NC | |
| 54 | TRRIN | TRR control input pin |
| 55 | TRRREF | TRR driver block reference voltage |
| 1, 28, 29, 56, TAB | | GND |

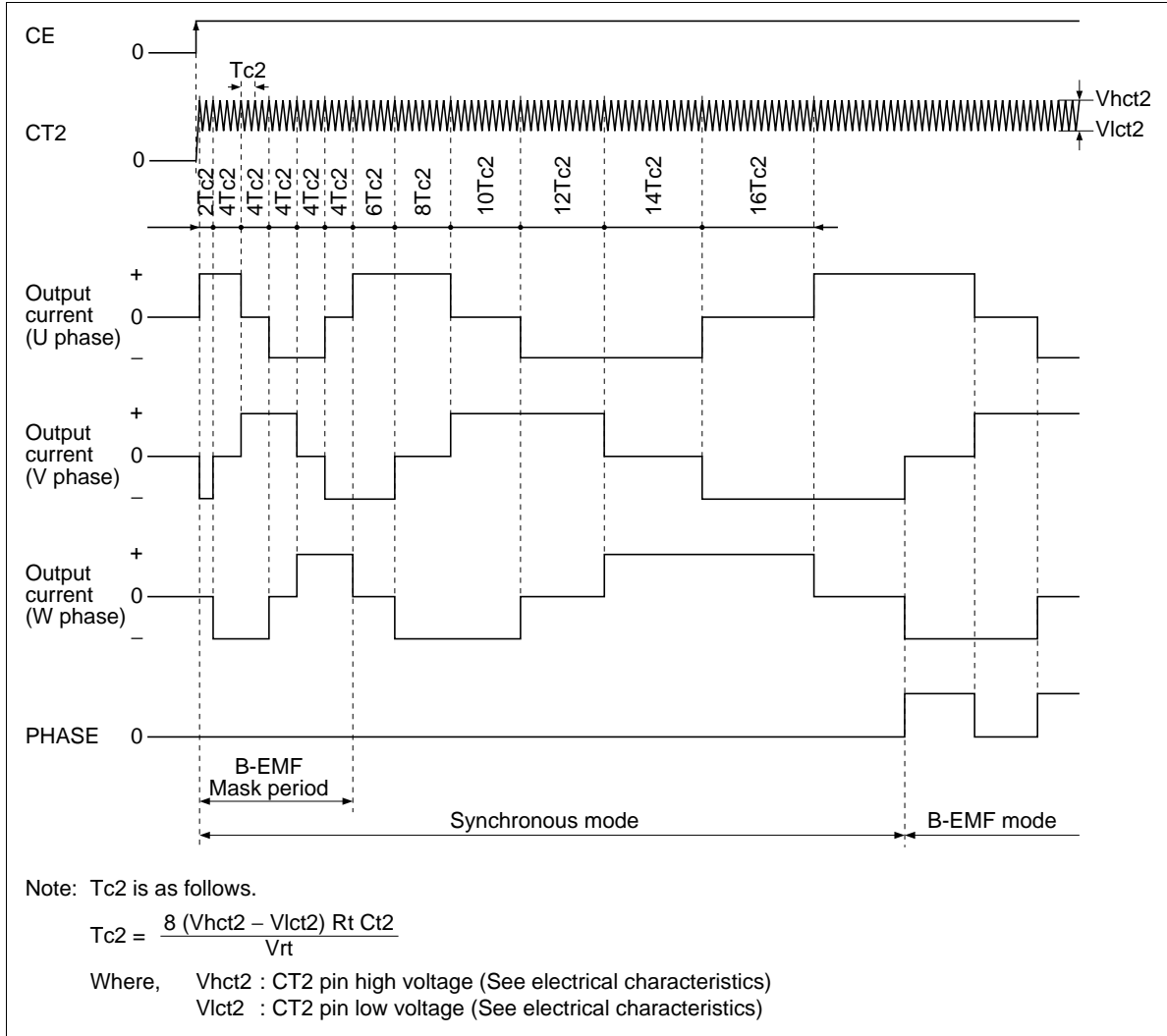
Block Diagram



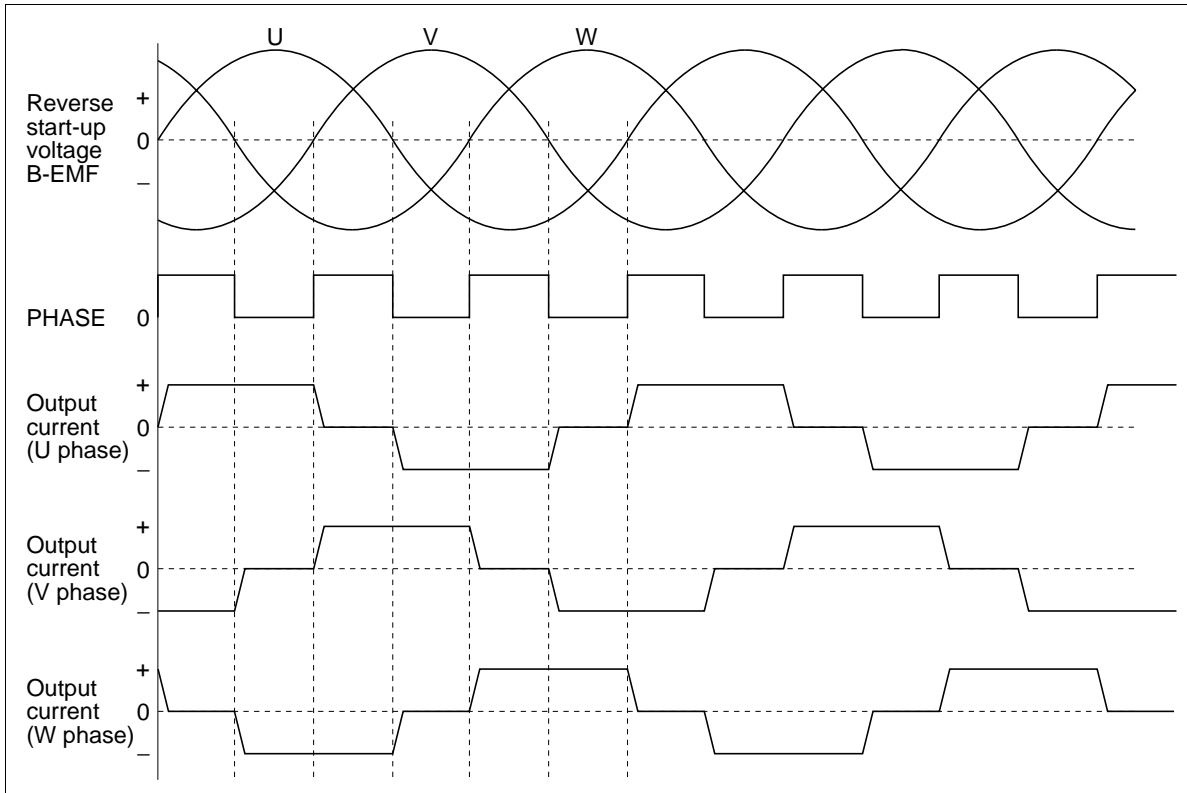
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Timing Chart

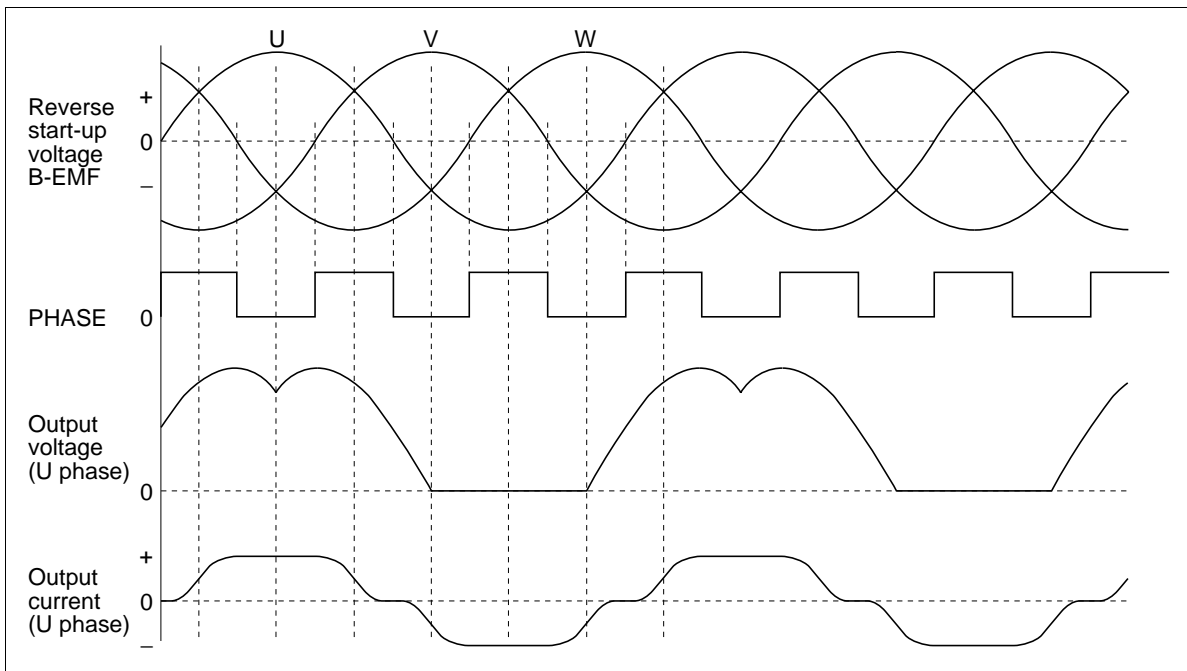
1. Start-up



2. Acceleration (switching mode)



3. Running (soft switching mode)



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Truth Table

Table 1 Overall

| CE | OTSD | SPN Driver | FCS Driver | TRR Driver | SLD Driver | TRY Driver |
|----|------|------------|------------|------------|------------|------------|
| L | X | Z | Z | Z | Z | Z |
| H | ON | Z | Z | Z | Z | Z |
| | OFF | ON | ON | ON | ON | ON |

Note: X: Option, Z: Hi impedance

Table 2 SPN Driver

| BRKSEL | VCTL | SPN Driver |
|--------|---------------|----------------|
| X | > REFIN | Forward torque |
| | REFIN | Z |
| L | < REFIN | Short brake |
| H | REFIN – 0.6 V | Reverse brake |

Note: X: Option, Z: Hi impedance

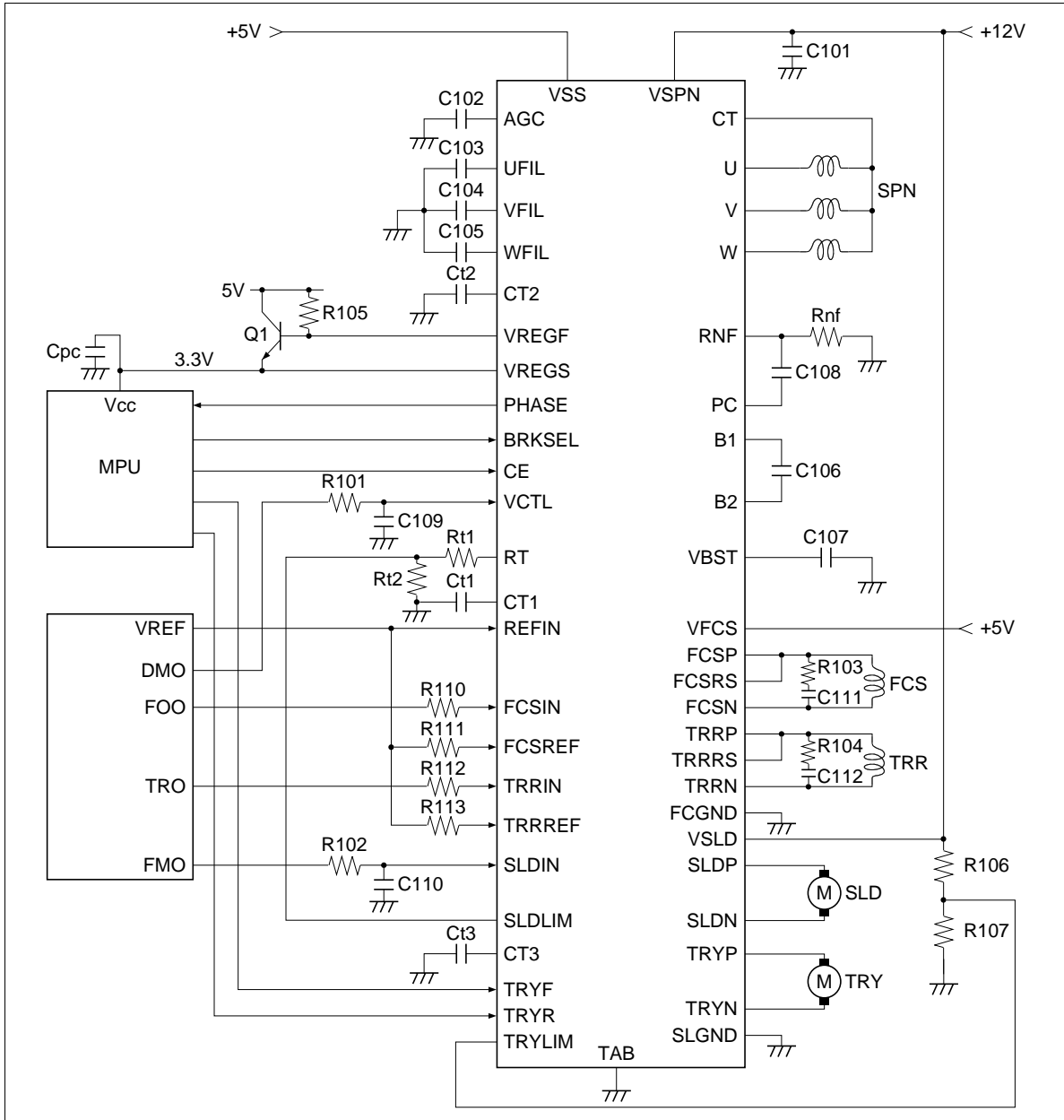
Table 3 TRY Driver

| TRYF | TRYR | P Output | N Output |
|------|------|----------|----------|
| L | L | Z | Z |
| L | H | L | H |
| H | L | H | L |
| H | H | H | H |

Note: Z: Hi impedance

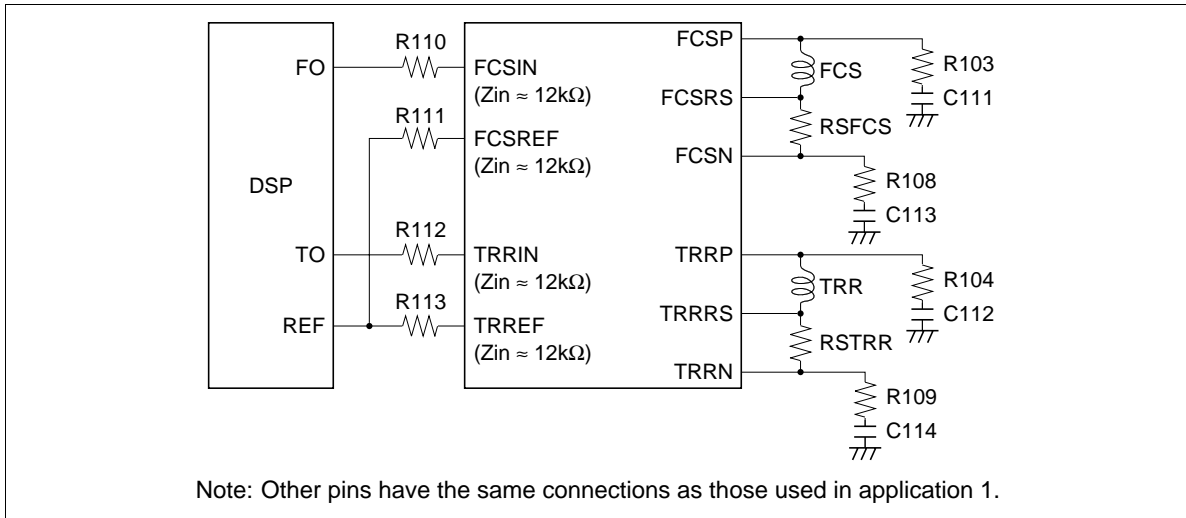
Application

1. FCS, TRR voltage drive

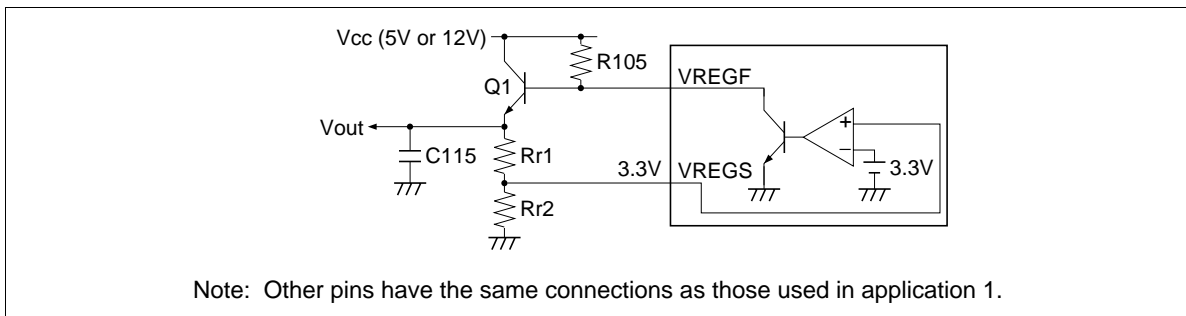


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2. FCS, TRR voltage drive



3. When used at a voltage other than 3.3 V with a voltage regulator ($V_{out} = 3.3$ to $V_{cc} - 1$ V)



External Components

| Parts No. | Reccomended Value | Reccomended Range | Purpose | Note |
|--------------|-------------------|-------------------|---|------|
| R101 | 47 kΩ | ≤ 47 kΩ | Filter for SPN driver control input | |
| R102 | 47 kΩ | ≤ 47 kΩ | Filter for SLD driver control input | |
| R103 | 6.8 Ω | — | To stop FCS block oscillation | |
| R104 | 6.8 Ω | — | To stop TRR block oscillation | |
| R105 | 500 Ω | ≥ 100 Ω | for Q1 bias | |
| R106 | 20 kΩ | — | for TRY driver output voltage setting | |
| R107 | 27 kΩ | — | | |
| R108 | 6.8 Ω | — | To stop FCS block oscillation | |
| R109 | 6.8 Ω | — | To stop TRR block oscillation | |
| R110 to R113 | 20 kΩ | — | for BTL gain setting | 7 |
| Rnf | 0.25 Ω | ≥ 0.25 Ω | SPN driver current detection resistor | 1 |
| Rt1 | 1.8 kΩ | Rt1 + Rt2 = 10 kΩ | Reference current setting and SLD driver maximum duty setting | 2, 5 |
| Rt2 | 8.2 kΩ | | | |
| RSFCS | 1 Ω | ≥ 0.33 Ω | for FCS driver current sense | 7 |
| RSTRR | 1 Ω | ≥ 0.33 Ω | for TRR driver current sense | |
| Rr1 | — | — | Voltage regulator division resistor | 8 |
| Rr2 | — | — | | |
| C101 | 0.1 μF | ≥ 0.1 μF | for Power supply by passing | |
| C102 | 0.047 μF | | for B-EMF Amplitude AGC | |
| C103 | 0.01 μF | | for B-EMF filter | 6 |
| C104 | | | | |
| C105 | | | | |
| C106 | 0.22 μF | ≥ 0.22 μF | for Booster pumping | |
| C107 | 0.47 μF | ≥ 0.47 μF | for Booster output smoothing | |
| C108 | 0.1 μF | | for SPN driver phase compensation | |
| C109 | 0.01 μF | | Filter for SPN control input | |
| C110 | 3300 pF | | Filter for SLD control input | |
| C111 | 0.01 μF | — | To stop FCS block oscillation | |
| C112 | 0.01 μF | — | To stop TRR block oscillation | |
| C113 | 0.01 μF | — | To stop FCS block oscillation | |
| C114 | 0.01 μF | — | To stop TRR block oscillation | |
| C115 | 2.2 μF | | for Voltage regulator smoothing | |

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External Components (cont)

| Parts No. | Reccomended Value | Reccomended Range | Purpose | Note |
|-----------|-------------------|-------------------|--|------|
| Ct1 | 150 pF | ≥ 120 pF | Time constant for CLK oscillation. Use a capacitor with good temperature characteristics. | 3 |
| Ct2 | 0.033 μF | | Time constant for start-up oscillation. Use a capacitor with good temperature characteristics. | 4 |
| Ct3 | 470 pF | ≥ 390 pF | PWM carrier oscillation time constant | 5 |
| Q1 | | | Transistor for voltage regulator | |

Note: 1. The output current maximum value $I_{ospnmax}$ of SPN driver is controlled according to the following equation. However, V_{spncl} is the current limiter reference voltage. (See the electrical characteristics)

$$I_{ospnmax} = \frac{V_{spncl}}{R_{nf}}$$

2. The maximum duty D_{max} of SLD driver output is controlled according to the following equation.

$$D_{max} = \frac{V_{rt}}{V_{hct3} - V_{lct3}} \left(\frac{R_{t2}}{R_t} - \frac{V_{lct3}}{V_{rt}} \right) \times 100 (\%)$$

However,

$$R_t = R_{t1} + R_{t2}, \quad \frac{R_{t2}}{R_t} \geq \frac{V_{lct3}}{V_{rt}}$$

Where, V_{rt} : RT pin voltage (See the electrical characteristics)

V_{lct3} : CT3 pin low voltage (≈ 1.3 V)

V_{hct3} : CT3 pin high voltage (≈ 3.3 V)

Since $V_{rt} \approx V_{hct3}$, D_{max} is not limited at 100% when $R_{t1} = 0 \Omega$.

3. The CLK oscillation frequency is determined by the following equation.

$$f_{clk} = \frac{V_{rt}}{8 C_{t1} R_t \Delta V_{ct1}}$$

Where, V_{rt} : RT pin voltage (See the electrical characteristics)

ΔV_{ct1} : CT1 pin voltage amplitude (≈ 1 V)

4. The C_{t2} for start-up oscillation is determined by the following equation.

$$T_{c2} = \frac{1}{6} \sqrt{\frac{J}{P K_t I_{spnmax}}}$$

$$C_{t2} = \frac{T_{c2} V_{rt}}{8 R_t (V_{hct2} - V_{lct2})}$$

Where, J : Spindle motor inertia ($\text{kg} \cdot \text{cm} \cdot \text{S}^2$)

P : Number of spindle motor poles (Total number of S poles and N poles)

K_t : Spindle motor torque constant ($\text{kg} \cdot \text{cm} / \text{A}$)

V_{hct2} : CT2 pin high voltage (≈ 3.3 V)

V_{lct2} : CT2 pin low voltage (≈ 1.3 V)

5. The PWM oscillation frequency f_{pwm} is determined by the following equation.

$$f_{pwm} = \frac{V_{rt}}{8 C_{t3} R_t (V_{hct3} - V_{lct3})}$$

Where, V_{hct3} : CT3 pin high voltage (≈ 3.3 V)

V_{lct3} : CT3 pin low voltage (≈ 1.3 V)

6. The C103 to C105 for B-EMF filter are determined by the following equation.

$$\frac{21}{\pi \cdot R_{flt} \cdot N_o \cdot P} \leq C_{103} \leq \frac{35}{\pi \cdot R_{flt} \cdot N_o \cdot P}$$

Where, R_{fill} : B-EMF detection output resistor (See the electrical characteristics)

N_o : Maximum rotation speed (rpm)

7. The FCS and TRR is determined by the following equation.

Voltage drive:

$$G_v = \frac{R_1}{R_{in} + R_2}$$

Current drive:

$$G_m = \frac{R_1}{((R_{in} + R_2) \cdot R_s)}$$

Where, R_1 : Resistor of IC inside ($\approx 30k\Omega$)

R_2 : Resistor of IC inside ($\approx 7k\Omega$)

R_{in} : Resistor value inserted in the input (Ω)
(R110 to R113)

R_s : Current sense resistor (Ω)

8. The output voltage V_{out} of voltage regulator is determined by the following equation.

$$V_{out} = 3.3 \left(1 + \frac{R_{r1}}{R_{r2}} \right)$$

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Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Rating | Unit | Note |
|--------------------------------|------------------|-------------|------|------|
| Supplu voltage | Vss | 7 | V | 1 |
| SPN supply voltage | Vspn | 15 | V | 1 |
| FCS & TRR supply voltage | Vfcs | 15 | V | 1 |
| SLD & TRY supply voltage | Vsld | 15 | V | 1 |
| Input voltage | Vin | 0 to Vss | V | 2 |
| | Vintrylim | Vss to Vsld | V | |
| SPN output current | Iospn | 1.5 | A | 3 |
| FCS & TRR & TRY output current | Iofcs | 0.5 | A | 3 |
| SLD output current | Iosld | 1.5 | A | 3 |
| Power dissipation | P _T | 5 | W | 4 |
| Junction temperature | T _j | 160 | °C | 1 |
| Storage temperature range | T _{stg} | -55 to +125 | °C | |

Note: 1. Operating voltage range is shown below.

Vss = 4.25 to 5.75 V

Vspn = 4.25 to 13.8 V

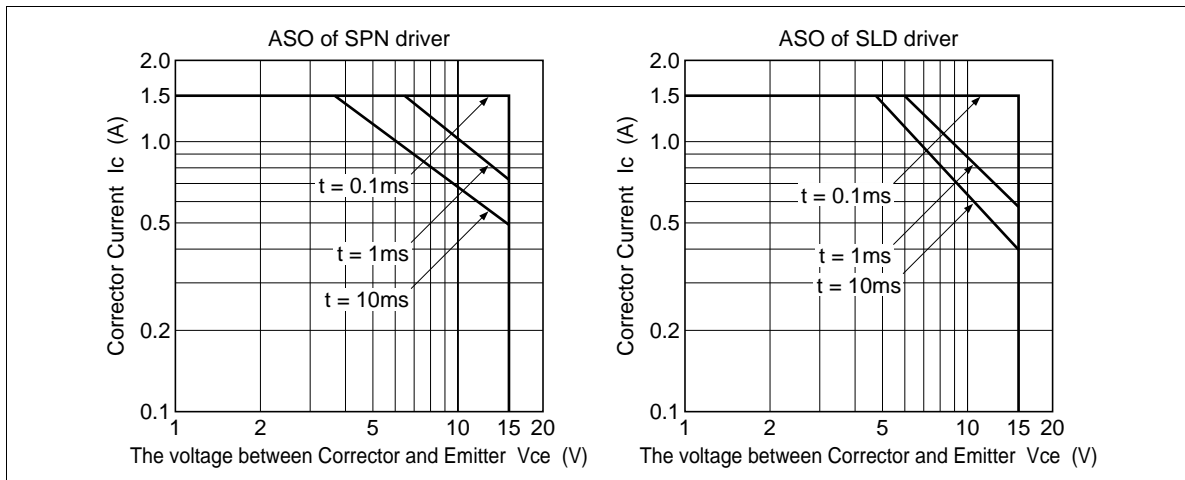
Vfcs = 4.25 to 13.8 V (However, the output high voltage is clamped at 7 V.)

Vsld = 4.25 to 13.8 V

Tjopr = 0 to +135°C

2. Applied to BRKSEL, VCTL, REFIN, CE, FCSIN, FCSREF, TRRIN, TRRREF, SLDIN, SLDLIM, TRYF and TRYR.

3. ASO (Area of Safety Operation) of each output transistor is shown below (TBD).



4. Thermal resistance is shown below.

$\theta_{j-tab} \leq 12^\circ\text{C} / \text{W}$ (back side tab soldering area is 70% or more)

$\theta_{j-a} \leq 25^\circ\text{C} / \text{W}$ (mounted on 4 layer multi glass-epoxy board, back side tab soldering area is 70% or more)

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Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vslid = 12 V)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note | |
|-------------------|---------------------------|-----------------------|------|------|------|-------------------------------------|----------------------------|-----------|---|
| Quiescent current | I _{ss0} | — | 0.7 | 0.9 | mA | CE = L | VSS | | |
| | I _{spn0} | — | — | 0.2 | mA | | VSPN | | |
| | I _{fcs0} | — | — | 0.01 | mA | | VFCS | | |
| | I _{slid0} | — | — | 0.01 | mA | | VSLD | | |
| | I _{ss1} | 14 | 20 | 25 | mA | CE = H, VCTL = | VSS | | |
| | I _{spn1} | 11 | 15 | 20 | mA | FCSIN = TRRIN = | VSPN | | |
| | I _{fcs1} | 6 | 10 | 15 | mA | SLDIN = REFIN, | VFCS | | |
| | I _{slid1} | — | — | 1.0 | mA | TRYF = TRYR = L All load open | VSLD | | |
| | I _{ss2} | 20 | 33 | 60 | mA | CE = H, VCTL = | VSS | | |
| | I _{spn2} | 11 | 30 | 50 | mA | FCSIN = TRRIN = | VSPN | | |
| | I _{fcs2} | 7 | 10 | 15 | mA | SLDIN = 5 V, | VFCS | | |
| | I _{slid2} | -15 | -1.0 | 1.0 | mA | TRYF, TRYR = H, L, All load open | VSLD | | |
| Logic input | Input current | I _{ince} | 0 | 70 | 100 | μA | V _{in} = 0 to 5 V | BRKSEL, | |
| | | I _{in} | — | — | ±10 | μA | | CE, TRYF, | |
| | Low level voltage | V _{il} | — | — | 0.8 | V | | TRYR | |
| | High level voltage | V _{ih} | 2.0 | — | — | V | | | |
| Logic output | Low level voltage | V _{ol} | — | — | 0.4 | V | I _o = 1 mA | PHASE | |
| | Leak current | I _{cer1} | — | — | ±10 | μA | V _{ce} = 15 V | | |
| SPN driver | Output saturation voltage | V _{satspn} | — | 1.25 | 1.75 | V | I _{ospn} = 1.0 A | U, V, W | 1 |
| | Leak current | I _{cer2} | 1.3 | 2.2 | 3 | mA | V _{ce} = 15 V | | |
| | Current limiter voltage | V _{spncl} | 238 | 265 | 292 | mV | R _{nf} = 0.25 Ω | RNF | 2 |
| FCS driver | Input resistance | R _{infcs} | 9.6 | 12 | 14.4 | kΩ | | FCSIN | |
| | | R _{infcsref} | 9.6 | 12 | 14.4 | kΩ | | | |
| | Input voltage range | V _{infcs} | 0 | — | 5 | V | | | |

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Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{SS} = 5\text{ V}$, $V_{SPN} = 12\text{ V}$, $V_{FCS} = 5\text{ V}$, $V_{SLD} = 12\text{ V}$) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|-----------------|---------------------------|-----------|-------|------|---------------|---|-------------------------------|-----------------|------|
| FCS driver | Output quiescent voltage | Vqfcs | 2.375 | 2.5 | 2.625 | V | FCSIN=FCSREF=2.5 V, VFCS=5 V | FCSP, FCSN | 3 |
| | Output offset voltage | Vosfcs | — | — | ±20 | mV | | | |
| | Output saturation voltage | Vsatfcs | — | 1.0 | 1.4 | V | $I_o = 0.33\text{ A}$ | | 1 |
| | Voltage gain | Gvfcs | 11.6 | 12.6 | 13.6 | dB | | | 4 |
| | Gain band width | Bfcs | 100 | — | — | kHz | $\Delta G_v = -3\text{ dB}$ | | |
| TRR driver | Input resistance | Rintrr | 9.6 | 12 | 14.4 | k Ω | | TRRIN | |
| | | Rintrrref | 9.6 | 12 | 14.4 | k Ω | | | |
| | Input voltage range | Vintrr | 0 | — | 5 | V | | | |
| | Output quiescent voltage | Vqtrr | 2.375 | 2.5 | 2.625 | V | FCSIN=TRRREF=2.5 V, VFCS=5 V | TRRP, TRRN | 3 |
| | Output offset voltage | Vostrr | — | — | ±20 | mV | FCSIN = REF | | |
| | Output saturation voltage | Vsatrrr | — | 1.0 | 1.4 | V | $I_o = 0.33\text{ A}$ | | 1 |
| | Voltage gain | Gvtrr | 11.6 | 12.6 | 13.6 | dB | | | 4 |
| Gain band width | Btrr | 100 | — | — | kHz | $\Delta G_v = -3\text{ dB}$ | | | |
| SLD driver | Output saturation voltage | Vsatsld | — | 1.5 | 2.0 | V | $I_{osld} = 0.75\text{ A}$ | SLDP, SLDN | 1 |
| | Leak current | Icer3 | — | — | ±100 | μA | $V_{ce} = 15\text{ V}$ | | |
| | Penetration current | Iovlap | — | — | 100 | mA | | VSLD | 8 |
| | Transient response time | tph1 | — | — | 5 | μs | | SLDP, | |
| tph1 | | — | — | 5 | μs | | SLDN | | |
| TRY driver | Output saturation voltage | Vsattry | — | 1.0 | 1.4 | V | $I_{otry} = 0.33\text{ A}$ | TRYP, TRYN | 1 |
| | Leak current | Icer3 | — | — | ±100 | μA | $V_{ce} = 15\text{ V}$ | | |
| | Penetration current | Iovlap | — | — | 100 | mA | | VSLD | 8 |
| | Transient response time | tph1 | — | — | 5 | μs | | TRYP, | |
| | | tph1 | — | — | 5 | μs | | TRYN | |
| | Input current | Iintrylim | — | — | ±5 | μA | $V_{trylim}=7\text{ to VSLD}$ | | |
| Output voltage | Vlimtry | 0.1 | 0.7 | 1.0 | V | $R_L = 16\Omega$, $V_{trylim} = 7\text{ V}$ | | 9 | |

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Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Applicable Pins | Note |
|---------------------------|---------------------------------------|--------------------|-------|-------------------|-------|------|-------------------------------|---------------------|------|
| SPN current control | Input current | linspn | — | — | ±5.0 | μA | Vctl = 0 to Vss-1V | VCTL, | 2 |
| | REF voltage range | Vref | 1.6 | — | 3.0 | V | | REFIN | |
| | Dead zone voltage | Vdzspn | ±50 | — | ±120 | mV | Vref reference | | |
| | Current control gain | Gctl | — | -12 | ±1.5 | dB | | RNF | |
| Drive mode | Change threshold voltage | Vctl | — | 0.5 | ±0.1 | V | Vref reference | VCTL | 5 |
| | SW ↔ SOFT SW | f _{PHASE} | — | ≥f _{CT2} | ±50% | Hz | SOFT SW mode | U, V, W | 5 |
| | | | — | <f _{CT2} | -20% | Hz | SW mode | | |
| B-EMF detection | Output resistance | Rflt | — | 10 | ±20% | kΩ | | UFIL, VFIL, WFIL | |
| | Threshold voltage of PHASE occurrence | Viemf | — | 40 | ±50% | mVpp | VSPN ≥ Vss + 3V _F | U, V, W | 6 |
| | | | — | 28 | ±50% | mVpp | VSPN ≤ Vss + 3V _F | | |
| CLK | RT voltage | Vrt | 3.135 | 3.30 | 3.465 | V | | RT | |
| OSC | CLK oscillation frequency | fcik | 210 | 240 | 270 | kHz | Rt = 10 kΩ, Ct1 = 82 pF | CT1 | |
| Start-up circuit | Start-up oscillation frequency | fct2 | 437 | 485 | 534 | Hz | Rt = 10 kΩ, Ct2 = 0.033 μF | CT2 | |
| SLD control | Input current | linsld | — | — | ±5.0 | μA | Vsld = 0 to Vss-1V | SLDIN | |
| | Input voltage range | Vinsld | 0 | — | 4.0 | V | | | |
| | Limiter input current | lsldlim | — | — | ±5.0 | μA | | SLDLIM | |
| | PWM oscillation frequency | fpwm | 33 | 38 | 42.35 | kHz | Rt = 10 kΩ, Ct3 = 470 pF | | |
| | Control gain | D/V | 80 | 90 | 100 | %/V | | | 7 |
| | Offset voltage | Vossld | — | — | 20 | mV | SLDIN = REFIN | | |
| Voltage regulator | Output sink current | Isinkreg | 8.5 | 12.2 | — | mA | VREGS = 4 V, VREGF = 4 V | | |
| | Output voltage | Voutreg | 3.135 | 3.30 | 3.465 | V | | | |
| OTSD | Operating temperature | Tsd | 135 | 160 | — | °C | | | 8 |
| | Hysteresis | Thys | — | 50 | — | °C | | | |

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- Note: 1. The output saturation voltage is the sum of the upper and lower saturation voltages.
 2. See figure 1. Where,

$$G_{ctl} = 20 \log \frac{\Delta V_{rnf}}{\Delta V_{ctl}}$$

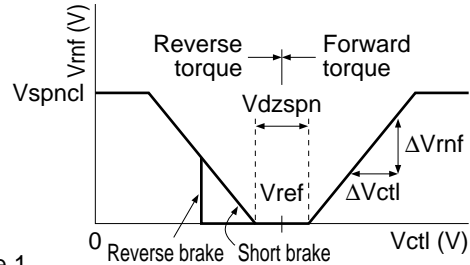


Figure 1

3. Where,

$$V_{qfcs} = \frac{V_{fcsp} + V_{fcsn}}{2}$$

$$V_{qtrr} = \frac{V_{trrp} + V_{trrn}}{2}$$

4. See figure 2. Where,

$$G_{vfc} = 20 \log \left(\frac{\Delta V_{fcsp}}{\Delta V_{fcsin}} \frac{\Delta V_{fcsn}}{\Delta V_{fcsin}} \right)$$

$$G_{vtr} = 20 \log \left(\frac{\Delta V_{trrp}}{\Delta V_{trrn}} \frac{\Delta V_{trrn}}{\Delta V_{trrn}} \right)$$

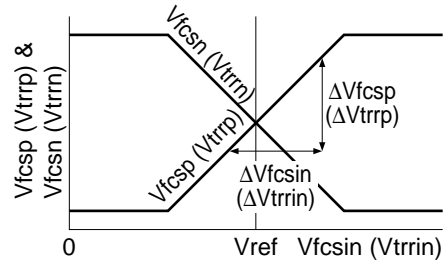


Figure 2

5. The circuit operates in soft switching drive mode only when the control input (V_{ctl}) is lower than f_{CT2} and f_{PHASE} is higher than the threshold voltage. See figure 3.

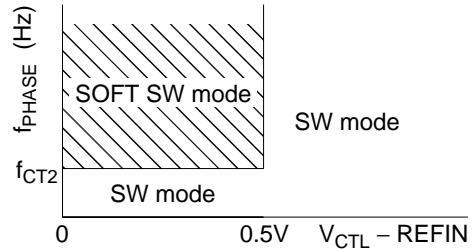


Figure 3

6. PHASE is output only when B-EMF exceeds the threshold voltage.

7. See figure 4. Where,

$$D/V = \frac{\Delta D}{\Delta V_{in}}$$

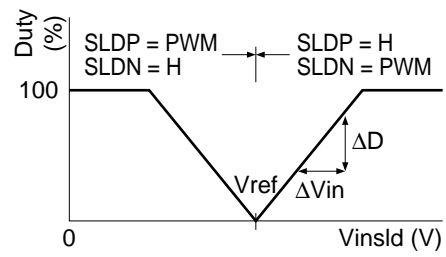


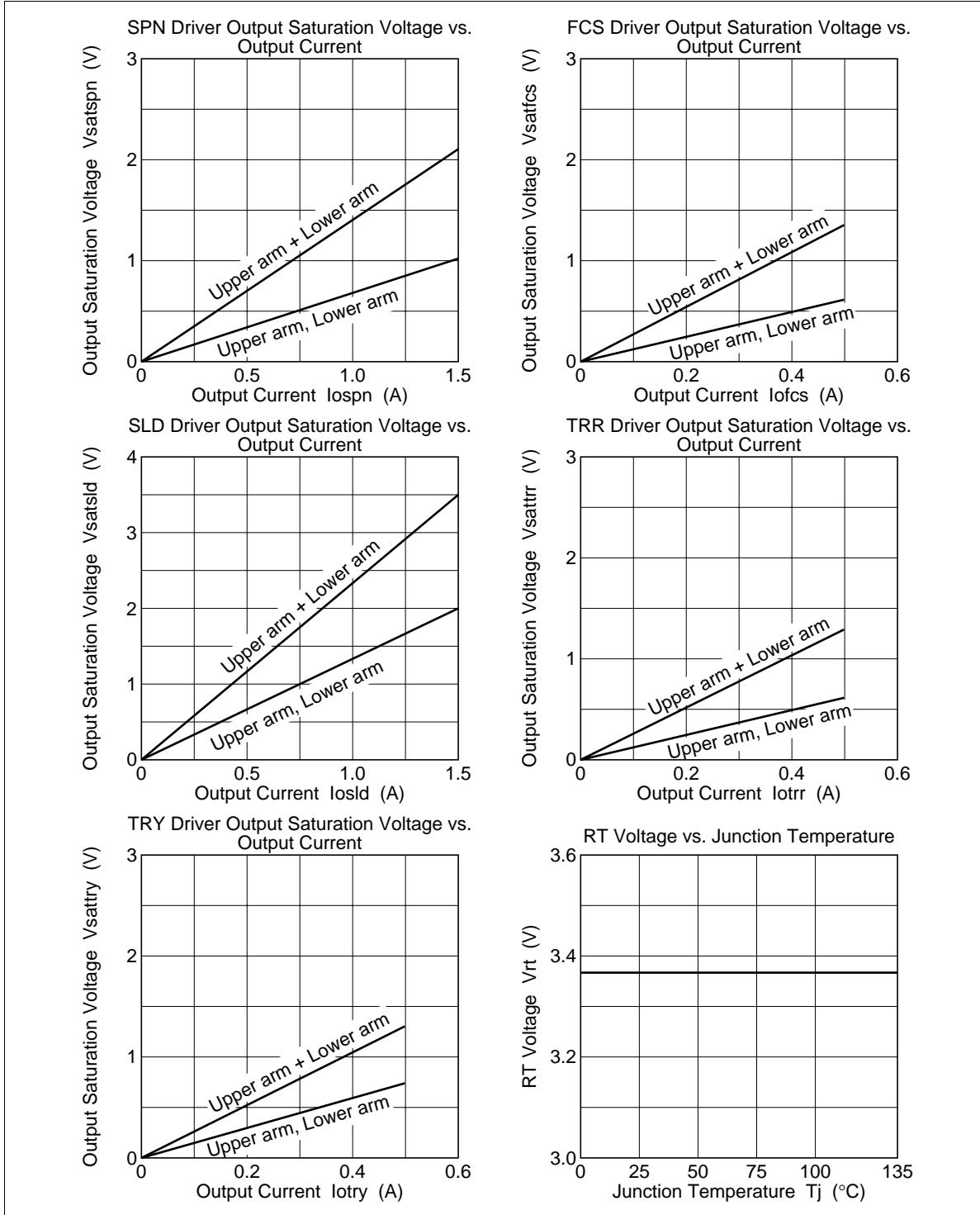
Figure 4

8. Design guide only.

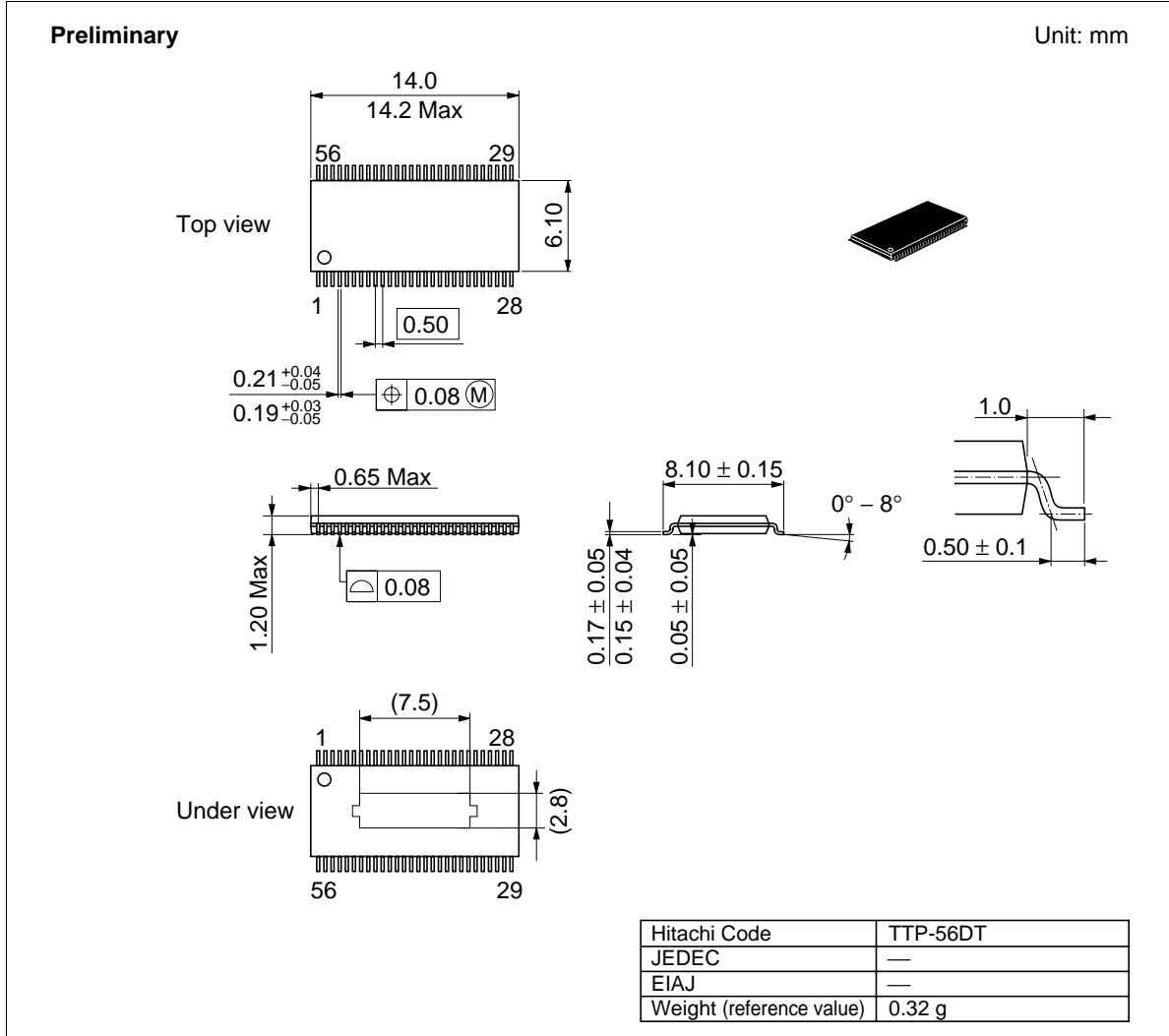
9. $V_{limtry} = V_{TRYP} - V_{TRYLIM}$, or $V_{TRYN} - V_{TRYLIM}$

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Reference Data



Package Dimensions



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