HA13609ANT

Three-Phase Brushless Motor Driver

HITACHI

ADE-207-232 (Z)
1st. Edition
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Description

The HA13609ANT is a 3-phase brushless motor driver IC with digital speed control. It is designed for use as a PPC or LBP scanner motor driver and provides the functions and features listed below.

Function

- Power MOS and power bipolar transistor driver circuits
- 16-bit serial interface
- Variable-speed digital speed control circuit
- Digital PLL
- Digital ready circuit
- PWM oscillator circuit
- Charge pump circuit
- Integrating amplifier circuit
- Current limit circuit
- Overshoot prevention circuit
- Braking function (with braking compete signal)
- Forward/reverse direction circuit
- Hall open circuit protection
- Watchdog timer (LVI, POR, and $\overline{\text{RST}}$ outputs)
- Stuck rotor protection

Features

- High breakdown voltage (50V/30mA) power transistor drive circuit
- PWM drive
- Variable speed control is possible (varying the servo filter constants is not required)
- Selectable rotation control method (discriminator control, PLL plus discriminator control)
- Selectable feedback type (voltage or current)
- Allows both PWM frequency switching and 100% duty operation
- Selectable current limiting level
- Braking mode selection (reverse braking, regeneration braking)

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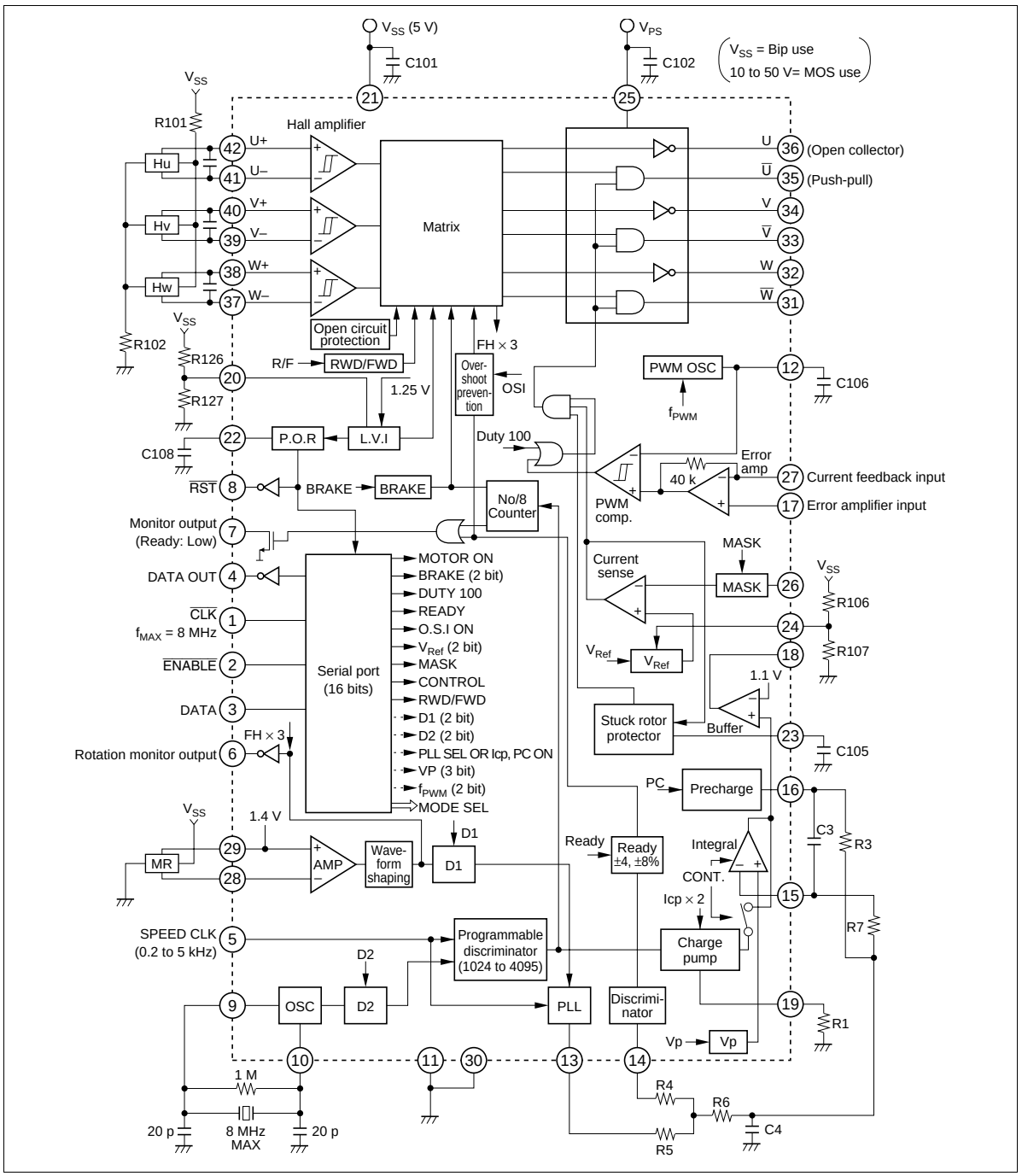
Block Diagram



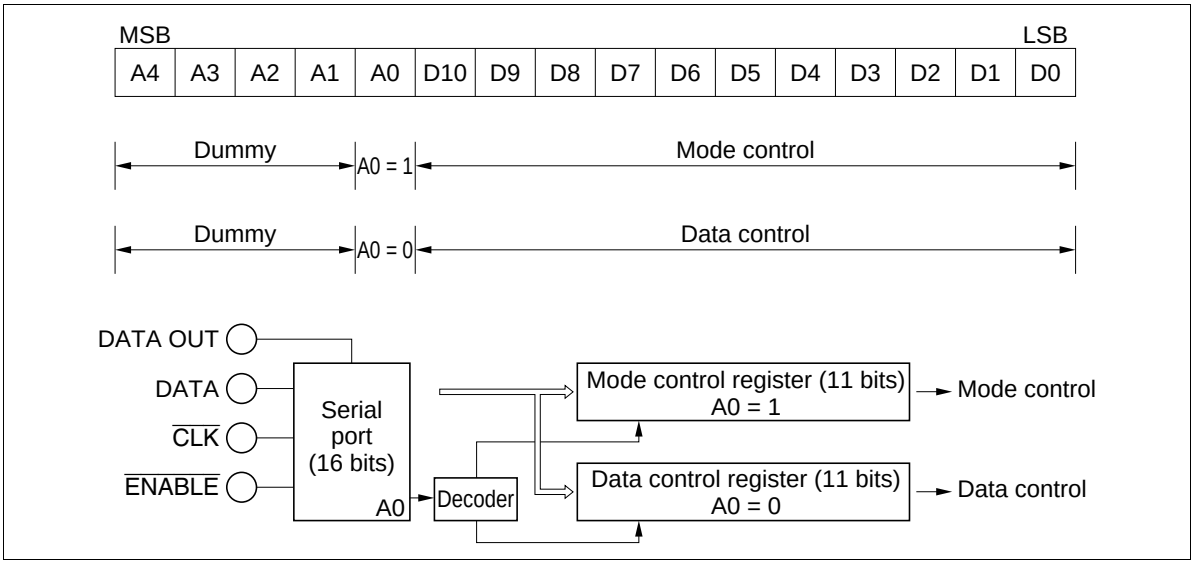
Pin Functions

Pin No.	Pin Name	Function
1	$\overline{\text{CLK}}$	Serial port reference signal input
2	$\overline{\text{ENABLE}}$	Serial port data write/latch signal input
3	DATA	Serial port data input
4	DATA OUT	Serial port data transfer complete signal output
5	SPEED CLK	Speed command signal input
6	TACHO OUT	Rotation monitor (MR, Hall ×3) output
7	READY	Ready and braking done (no/8) output (open collector output)
8	$\overline{\text{RST}}$	Power supply (V_{SS}) monitor output. High when a reduced power-supply voltage is detected.
9	OSC IN	Oscillator circuit input. Reference signal for all circuits other than the serial port.
10	OSC OUT	Oscillator circuit output
11	S-GND	Small-signal ground
12	PWM OSC	Connection for the capacitor that sets the oscillator frequency.
13	PLL OUT	SPEED CLK vs. speed detection signal speed comparison output
14	DIS OUT	SPEED CLK vs. speed detection signal phase comparison output
15	INTEG IN	Integrating amplifier input
16	CP OUT	Charge pump and integrating amplifier output
17	ERROR AMP IN	Error amplifier input
18	BUFFER OUT	Buffer amplifier output. Connect to pin 17 when current feedback is selected.
19	R1	Charge pump output current and PWM oscillator frequency setting
20	LVI	Reduced voltage detection level setting
21	V_{SS}	Small-signal circuit power supply. 5.5V maximum
22	POR	Power-on reset delay time setting
23	LOCK PRO	Motor rotation constraint mode coil current on/off time setting
24	V_{Ref}	Current limit setting
25	V_{PS}	Output driver power supply. 50V maximum
26	C Sense	Motor coil current detection
27	C F B	Current feedback input
28	MR IN –	Speed detection input
29	MR IN +	Speed detection input
30	P-GND	Output driver ground

Pin Functions (cont)

Pin No.	Pin Name	Function
31, 33, 35	$\overline{U}$, $\overline{V}$, $\overline{W}$	Lower arm driver push-pull output. Driven by a PWM signal. (Connect power NMOS or NPN transistors.)
32, 34, 36	U, V, W	Upper arm driver open drain output. (Connect a power PMOS or PNP transistor.)
37 to 42	U+, U– V+, V– W+, W–	Hall signal inputs

Serial Port Input Data Structure



Mode Control Register (A0 = 1)

Bit	Symbol	1	0	
MD0	MOTOR ON	MOTOR ON	MOTOR OFF	
MD1	BRAKE 1	MD1 0 1 0 1 MD2 0 0 1 1		*1
MD2	BRAKE 2	BRAKE OFF Brake 1 Brake 2 Brake 3		
MD3	DUTY 100	DUTY 100%	DUTY	
MD4	READY	4%	8%	*2
MD5	O.S.I ON	Active	Non Active	
MD6	$V_{Ref\ 1}$	MD6 0 1 0 1 MD7 0 0 1 1		
MD7	$V_{Ref\ 2}$	V_{Ref} V_{Ref} ×2 ← ×1 ← ×0.75 ← ×0.5		
MD8	MASK	×2	×1	*3
MD9	CONTROL	Discriminator	Discriminator + PLL	
MD10	R/F	Reverse	Forward	

Data Select Register (A0 = 0)

Bit	Symbol	1				0				
DD0	D1 A	DD0	0	1	0	1				
		DD1	0	0	1	1				
DD1	D1 B	D1	1/1	1/2	1/4	1/8				
DD2	D2 A	DD2	0	1	0	1				
		DD3	0	0	1	1				
DD3	D2 B	D2	1/1	1/2	1/4	1/8				
DD4	PLLSEL1 OR Icp	DD4	0	1	0	1				*4
		DD5	0	0	1	1				
DD5	PLLSEL2 OR PC ON	PLL OUT(Vp-p)	×100%	← ×75%	← ×50%	← ×25%				
DD6	VP1	DD6	0	1	0	0	1	1	0	1	*5
		DD7	0	0	1	0	1	0	1	1	
DD7	VP2	DD8	0	0	0	1	0	1	1	1	
DD8	VP3	VP (V)	2.2	+0.15	+0.3	+0.45	+0.6	–0.15	–0.3	–0.45	
DD9	f_{PWM1}	DD9	0	1	0	1					*6
		DD10	0	0	1	1					
DD10	f_{PWM2}	f_{PWM}	f_{PWM} ×1	← ×1.4	← ×1.9	← ×2.8					

Notes: 1. Off: The brake function does not operate.

Brake 1: Braking up to No/8.

Brake 2: Braking up to No/8, and then regenerative braking.

Brake 3: Regenerative braking. The No/8 signal is output.

During a braking operation, when the MR frequency when braking completes cannot be detected in the circuit (During braking, the speed detection signal for under setting is not output over the 2/D1 occurrence. Thus this occurs more easily for lower settings.), reverse rotation may continue in some cases. Note that this bit is also used to set the rotation monitor output (FH × 3 or the MR frequency). FH × 3 is only output from the rotation monitor when motor on (MD0 = 1) and brake 3 are selected.

2. The ready setting range has the following manufacturing variation:

4.3% ±25% (@MD4 = 1)

8.6% ±25% (@MD4 = 0)

3. This function masks the current limiter input (pin 27) (incorrect operation due to the recovery current). See page 20 for details.

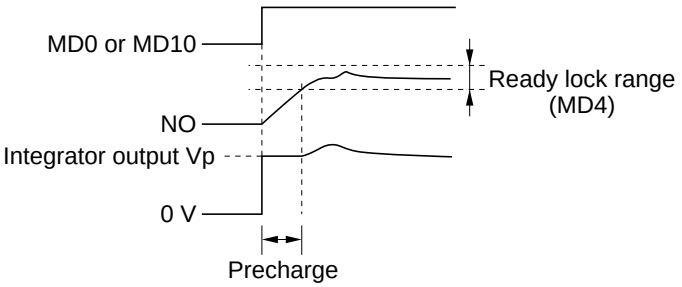
4. The PLL output setting indicates a change relative to 3.5 Vp-p. See the electrical characteristics.

This is valid when MD9 = 0 (PLL control). Note that DD4 also functions as the Icp selection in discriminator control mode.

$$Icp = \frac{V_{R1}}{4 \cdot R1}$$

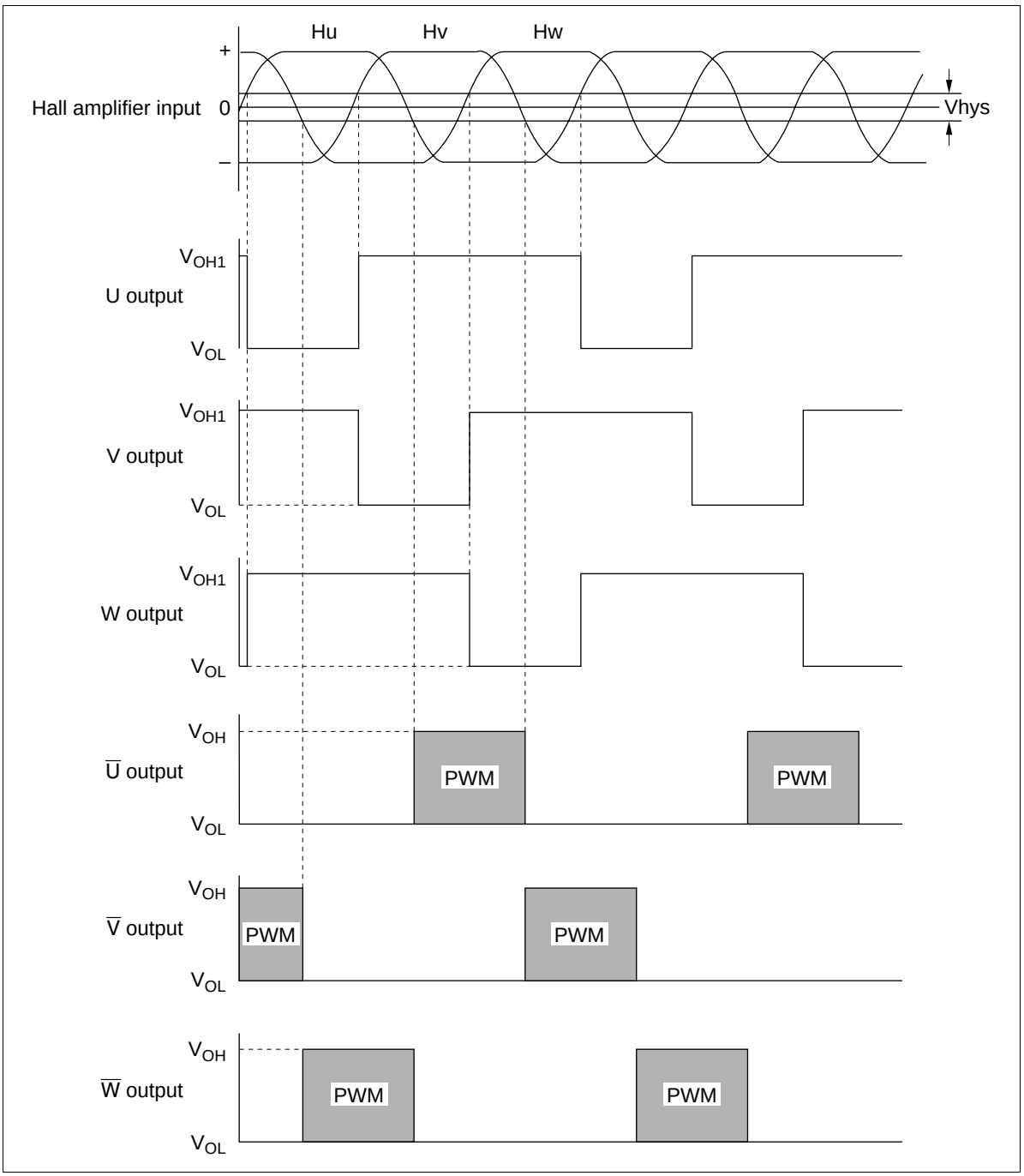
DD4 = 1 . . . . . Icp × 2
DD4 = 0 . . . . . Icp × 1 } @MD9 = 1

DD5 also controls the PC on function to reduce motor rotation overshoot when MD9 is 1 (discriminator control). This function does not operate when D9 is 0. The precharge voltage (i.e., the integrator output voltage initial clamp voltage) can be set by Vp1 to Vp3 (DD6 to DD8). The figure shows the precharge operation.

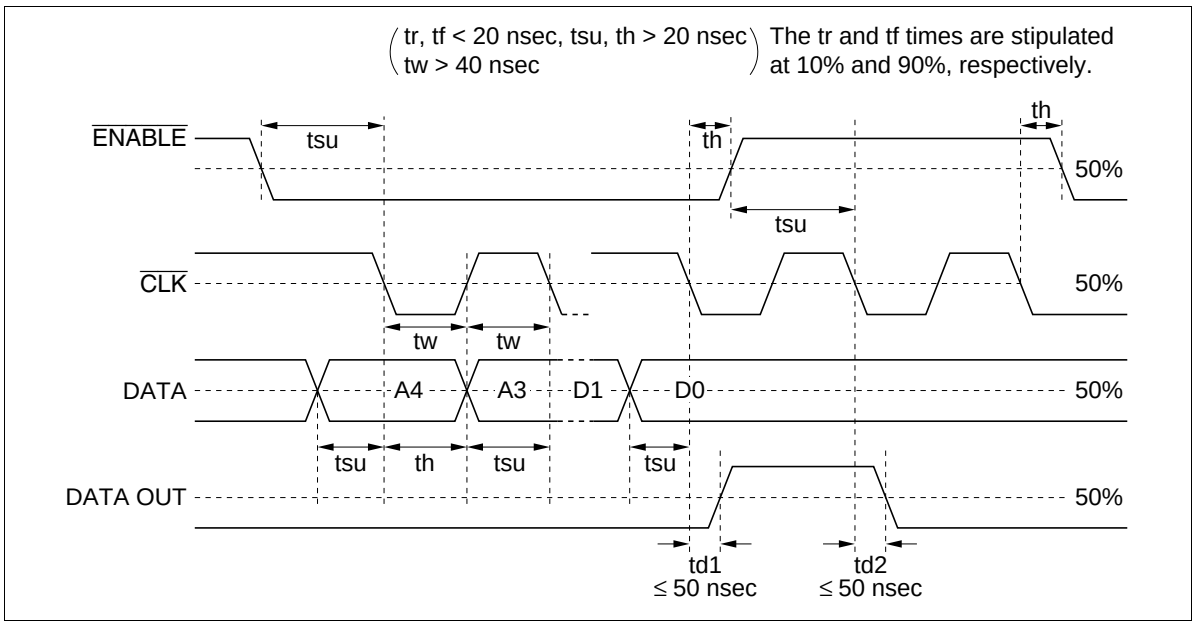


5. The Vp setting indicates the change relative to 2.2V. See the electrical characteristics.
6. Indicates the change relative to f_{PWM}. See the setting formula.

Timing Chart (Forward Mode)



Serial Port Timing Chart

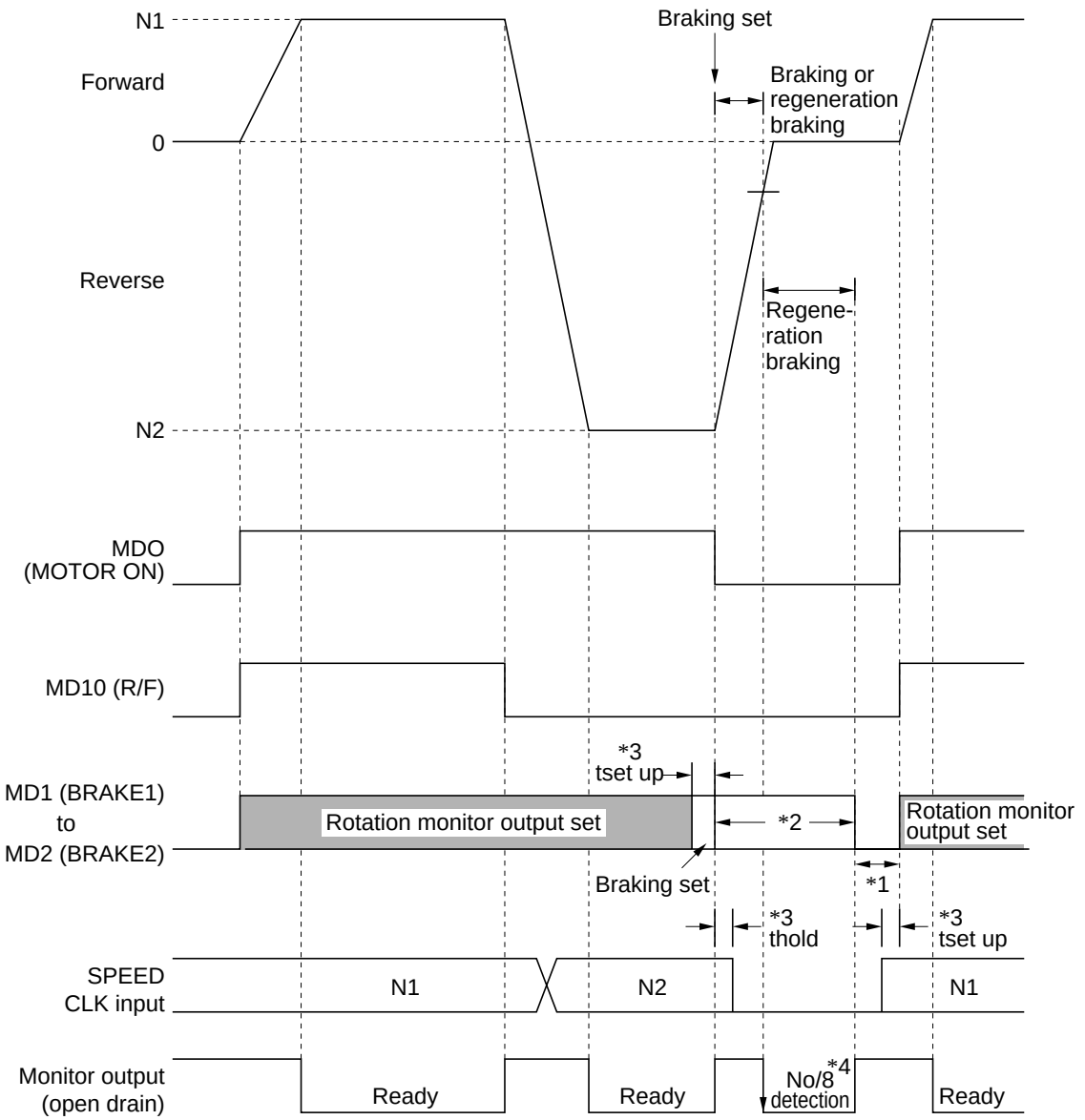


Braking Function

Input and Output Logic

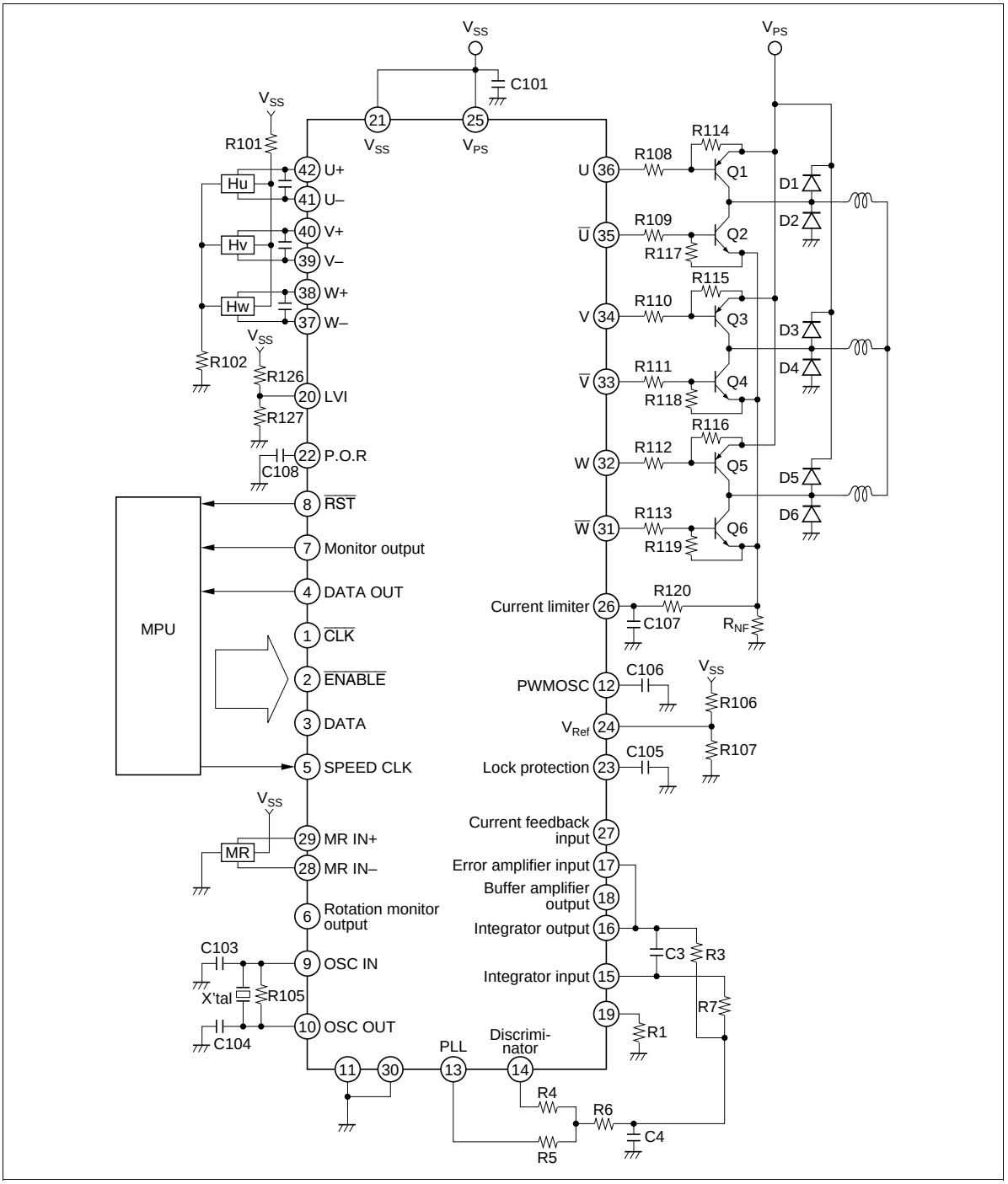
Serial Port Input				Output		
MOTOR ON (MD0)	**BRAKE 1 (MD1)**	**BRAKE 2 (MD2)**	**R/F (DD10)**	**Rotation Direction**	**Braking**	
1	*	*	0	Forward	OFF	*1
	*	*	1	Reverse	OFF	
0	0	0	*	—	OFF	*2
	*	*	0	Reverse	Brake	*3
	*	*	1	Forward		

Notes: 1. OFF: The braking function does not operate.
2. The IC goes to standby mode.
3. See the description of mode control for details on the braking operation.



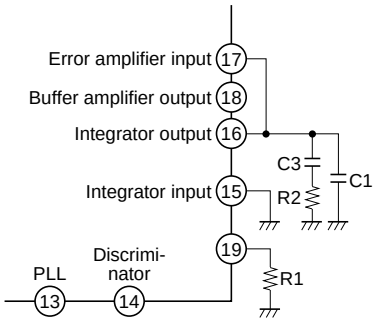
Notes:
1. The IC goes to standby mode when MOTOR ON, BRAKE1, and BRAKE2 are all 0.
2. Hold the data values here.
3. thold, tset up > $\frac{1}{f_{SPEED\ CLK}} \times 4$
4. The No/8 (braking completion) function does not operate when BRAKE1 and BRAKE2 are 0. Note that the No/8 detection signal is initialized to the high level in the mode in note 1 (standby mode).

Basic Application Circuit (Bipolar Transistor Circuit, Discriminator + PLL, Voltage Feedback, and Hall Elements)

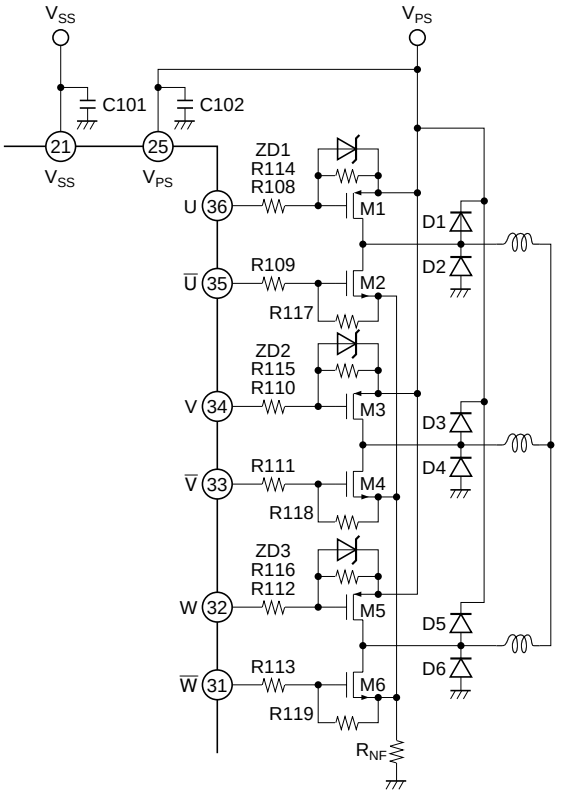


Application Circuits

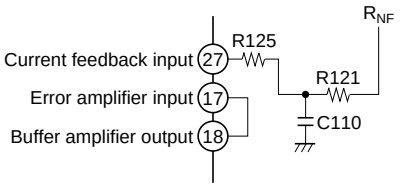
Application Circuit 1 (Discriminator)



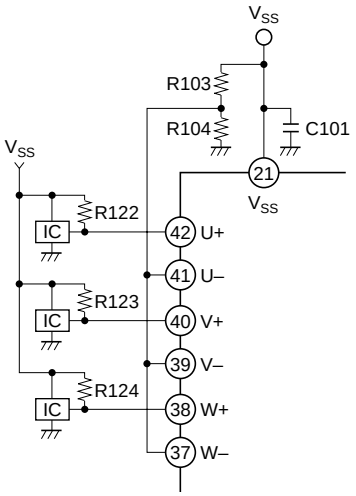
Application Circuit 2 (MOS Transistor Circuit)



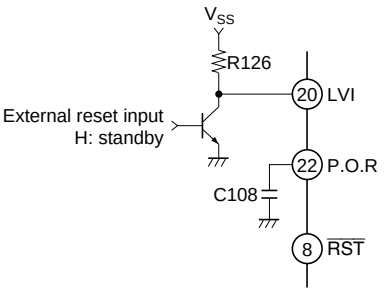
Application Circuit 3 (Current Feedback)



Application Circuit 4 (Hall IC input)



Application Circuit 5 (External Reset Input)



External Components

Part No.	Recommended Value	Purpose	Note
R101, R102	—	Hall element bias current	12
R103, R104	—	Hall IC applications, Hall input voltage	14
R105	1MΩ	Oscillator stabilization	
R106, R107	—	Current limiter reference voltage	15
R108 to R113	—	Power transistor base current limiter	16
R114 to R119	—	Power transistor base-emitter resistors (gate-source resistors)	16
R120	≥ 4.7kΩ	Current limiter filter	13
R121	—	Current feedback input filter	9
R122 to R124	—	Hall IC output current	14
R125	—	Current feedback input gain adjustment	10
R126, R127	—	LVI operating voltage, external reset input pull up	11
R_{NF}	—	Current detection	1
R1	≥ 1.5kΩ	Integration constant, PWM carrier frequency	2, 3, 5
R2	—	Integration constant	2
R3 to R7	—	Integration constant	3
C101, C102	≥ 0.1μF	Power supply stabilization	
C103, C104	10p to 50pF	Oscillator stabilization	7
C105	—	Lock protection operation time	4
C106	—	PWM carrier frequency	5
C107	—	Current limiter filter	13
C108	—	Power-on reset delay time	11
C110	—	Current feedback input filter	9
C111 to C113	—	Hall output stabilization	8
C1	—	Integration constant	2
C2	—	Integration constant	2
C3, C4	—	Integrator filter	3
ZD1 to ZD3	≈ 20V	MOS power transistor gate destruction protection	8
D1 to D6	—	Fly wheel diodes	8
X'tal	4 to 8MHz	Oscillator	6, 7

Notes: 1. Current limiter operates according to the following formula:

$$Iop = \frac{V_{Ref}}{R_{NF}} \quad [A]$$

Here, V_{Ref} is the value according to the V_{Ref} select function.

2. Use the following formulas as a guideline for setting the integration constant (@MD9 = 1). To minimize rotation deviation, set R1 to a relatively small value.

$$\omega o \leq \frac{2\pi}{20} \cdot f_{MR} \cdot D1 \quad [rad/s]$$

$$R1 = \frac{9.55 \cdot V_{R1} \cdot K_T \cdot R2}{4 \cdot J \cdot \omega o \cdot No} \cdot A \quad [\Omega]$$

However, R1 must be in the range $1.5k\Omega \leq R1 \leq 15k\Omega$.

$$C1 = 1 / (\sqrt{10} \cdot \omega o \cdot R2) \quad [F]$$

$$C2 = 10 \cdot C1 \quad [F]$$

Here, No : Rotation speed [min^{-1}]
f_{MR} : MR frequency [Hz]
D1 : Divider determined by D1 select
V_{R1} : Charge pump bias voltage 1.16 [V]
K_T : Motor torque constant [N·m/A]
J : Motor moment of inertia [$kg \cdot m^2$]
A : PWM comparator current gain [A/V]

Voltage feedback method: $A = \frac{2Vps - 0.83V_E - Vsat}{Rm \cdot Vosc}$

Current feedback method: $A = \frac{G_B}{R_{NF}}$

V_{PS} : Power system power-supply voltage [V]
V_E : Motor back EMF [V_{P-P}/T·T]
Vsat : External transistor saturation voltage [V] (See the electrical characteristics)
Rm : Motor coil resistance [Ω/T·T]
Vosc : PWM amplitude voltage [V_{P-P}] (See the electrical characteristics)
G_B : Buffer amplifier gain [V/V] (See the electrical characteristics)

3. Use the following formulas as guidelines for setting the integrator filter:

First determine the angular frequency of ω_P for DIS OUT and PLL OUT.

$$\omega_P = 2\pi \cdot f_{MR} \cdot D1 \quad [rad/s]$$

Determine the angular frequency of ω_M for Motor.

$$\omega_M \approx \frac{9.55}{No} \cdot \frac{1}{J} \left(K_T \cdot \frac{Vref}{R_{NF}} - T_L \right) \quad [rad/s]$$

Determine the ωo.

$$\omega o = \sqrt{\omega_P \cdot \omega_M} \quad [rad/s]$$

Determine the integrator's DC gain $G_{(E)}$.

$$G_{(E)} = \frac{J \cdot \omega o}{9.55 \cdot K_T \cdot A} \cdot \frac{1}{\frac{Z}{60} \cdot D1 \cdot 2\pi \cdot \frac{K\phi}{\omega o} \cdot PLL\ SEL}$$

Here, Kø : PLL gain = 0.28 [V/rad/s]
T_L : Rated load torque [N·m]
PLL SEL : PLL output ratio
Vref : Current limiter reference voltage [V]
Z : MR pulse per round [P/R]

Set C3 and derive the integration constants from following formulas.

$R6 = 0\ \Omega$

$$R3 = \frac{1}{\omega_P \cdot C3}$$

$$R5 = \frac{R3}{G_{(E)}}$$

$$C4 = \frac{1}{2 \cdot R5 \cdot \omega o}$$

$R7 = R5$

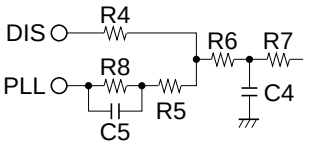
Next, determine R4 to match the phase of PLL OUT.

$$R4 = \frac{(3.46 - V_P)\ R3}{(V_P - 1.2) - (1.9 - V_P) \cdot R3 / R5}$$

Here, V_P : See the electrical characteristics.

When log ω_P/ω_M is greater than 2, a phase advance to compensate for this phenomenon is required. Use the following formula to set the phase advance;

$$C5 \cdot R8 > \frac{20 \cdot 2}{\omega_P}$$



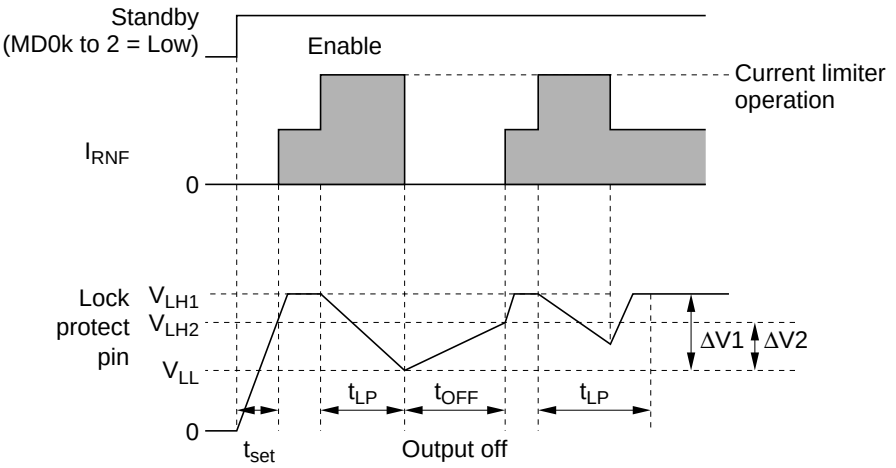
4. The following formulas determine the stuck rotor protect detection time t_{LP} (detects the current limiter operating time), the output off time t_{OFF}, and the setup time t_{set}. The figures show the operating waveforms.

$$t_{LP} = \frac{\Delta V1}{Isink} \cdot C105 \approx 0.09 \times 10^6 \cdot C105 \quad [sec]$$

$$t_{OFF} = \frac{\Delta V2}{Isource} \cdot C105 \approx 0.32 \times 10^6 \cdot C105 \quad [sec]$$

$$t_{set} = \frac{V_{LH2}}{Is} \cdot C105 \approx 0.0005 \times 10^6 \cdot C105 \quad [sec]$$

See the electrical characteristics for the definitions of ΔV1, ΔV2, Isink, Isource, and Is.



Note that a capacitor with a leakage current sufficiently smaller that Isource must be used for C105.

5. The PWM carrier frequency f_{PWM} is determined by the following formula:

$$f_{PWM} = 0.0489 \frac{1}{C106 \cdot R1} \quad [Hz]$$

6. The relationships between the crystal oscillator frequency f_{OSC} and the speed command clock f_{CLK}, the speed detection signal f_{MR}, and the discriminator resolution (number of counts) C are shown below.

$f_{CLK} = f_{MR} \cdot D1$

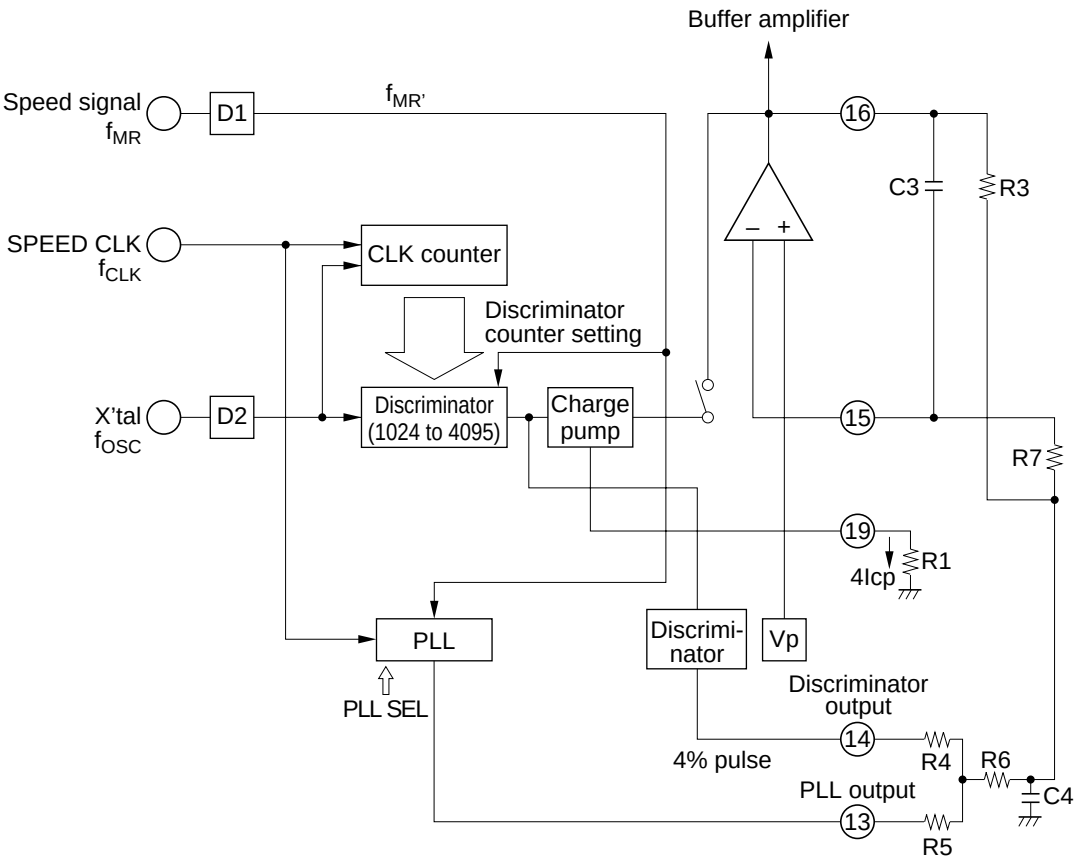
$f_{OSC} = f_{CLK} \cdot 1 / D2 \cdot C$ [Hz]

However, C must be in the range $1024 \leq C \leq 4095$

Here, D1 : The MR signal divisor determined by D1 select

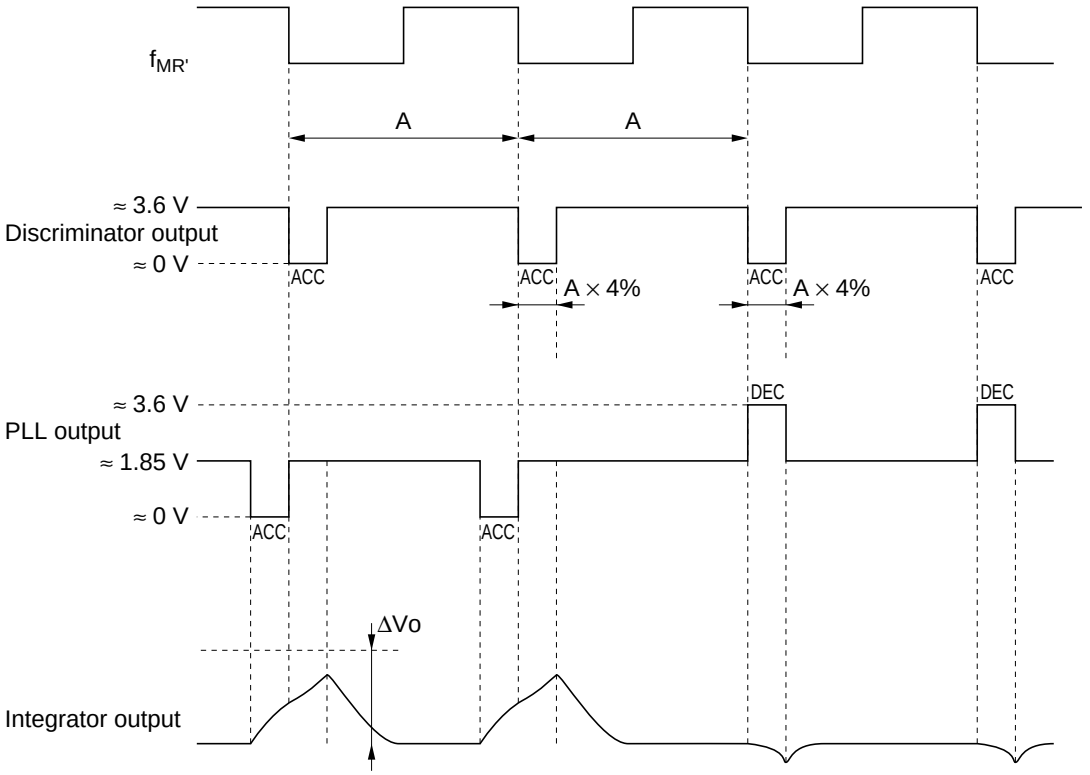
D2 : The crystal oscillator frequency divisor determined by D2 select.

Configuration of the speed control and phase control blocks when @MD9 = 0

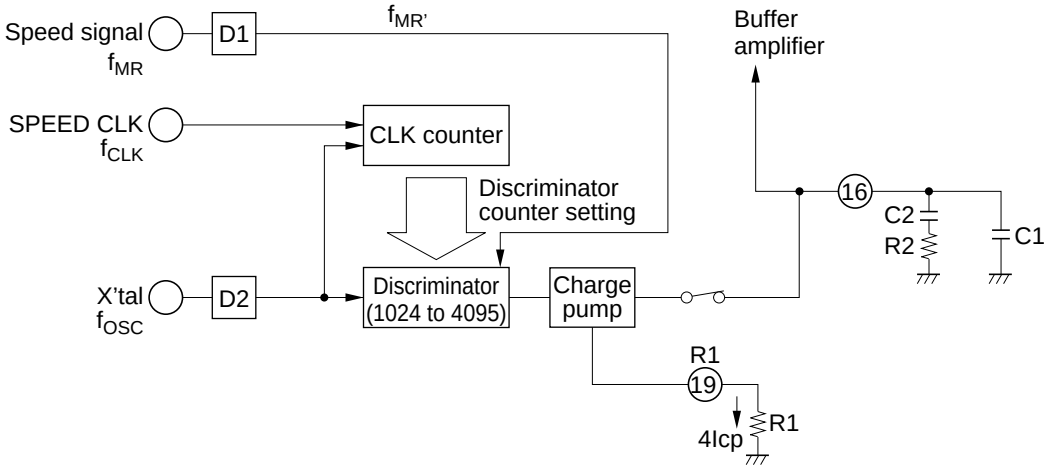


Note: If possible, Tr and Tf for the SPEED CLK signal should be under 20 ns when using this circuit.

Timing in phase control mode



Configuration of the speed control block when @MD9 = 1



Note: If possible, Tr and Tf for the SPEED CLK signal should be under 20 ns when using this circuit.

7. The table below lists reference values for the stabilization capacitors C103 and C104 for the crystal oscillator element according to the frequency used.

X'tal (MHz)	C103, C104 (pF)
4 to 6	≈ 20 to 40
6 to 8	≈ 10 to 20

   Use a resonance resistance of under 50Ω as a criterion for selecting the crystal element used.

8. Include these components if required.
9. The cutoff frequency of the filter formed by C110 and R121 should be between 3 and 10 times the PWM oscillator frequency.
10. The gain, G_{CTL}, from the error amplifier input to R_{NF} is given be the following formula:

$$G_{CTL} = 1 + \frac{Rif}{R125}$$

11. The formulas below determine the relationship between capacitor C108, which sets the power on reset (POR) delay time, and the resistors R126 and R127, which set LVI.

$$V_{LVI} = V_{SD}\left(1 + \frac{R126}{R127}\right) \quad [V]$$

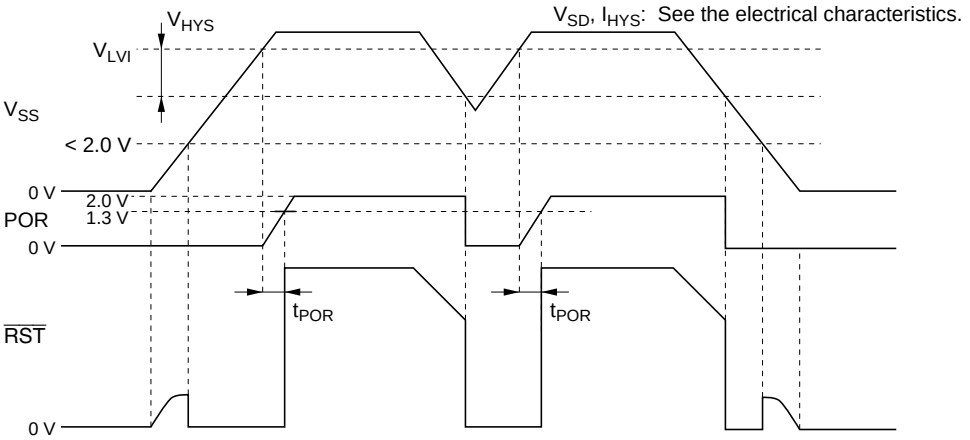
   However, $V_{LVI} > 3V$

$$V_{HYS} = R126 \cdot I_{HYS} \quad [V]$$

   However, $V_{LVI} - V_{HYS} > 2.5V$

$$t_{POR} = 0.052 \times 10^6 \cdot C108 \quad [sec]$$

   The time t_{POR} is the time required for the oscillator to reach stability. This time should be 20ms or longer.

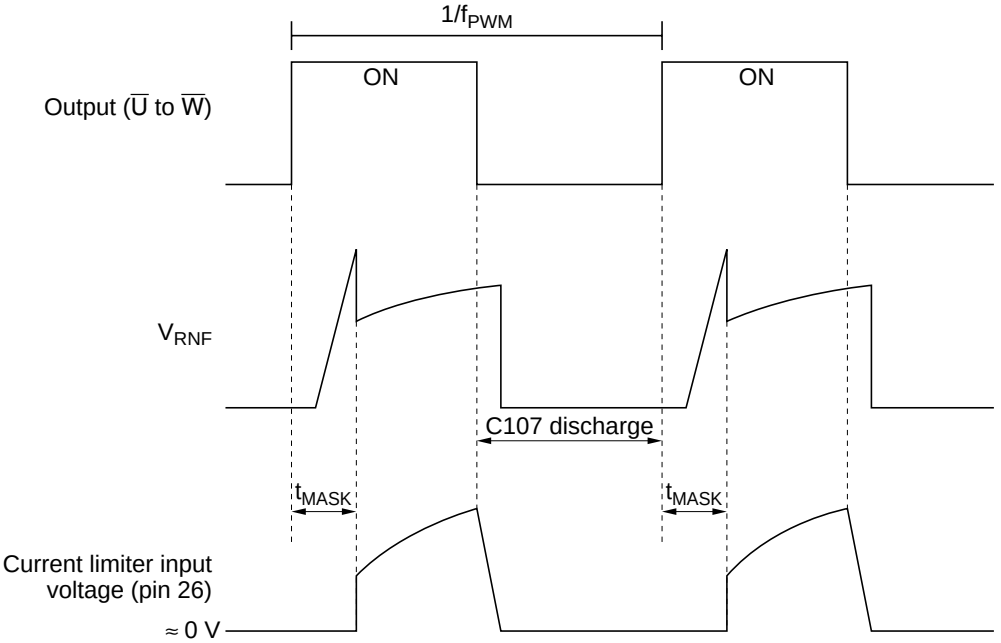


   When using an external reset input to set the IC to the standby state, pin 20 must be set to a low level that is under 0.4V.

12. When the Hall inputs are common mode input, the open circuit protection circuit makes the output transistors non-operational. When all the Hall input phases are open, the lower side output transistors become non-operational.

    The output transistors will be disabled if one or two phases are disconnected (become open) only when the Hall inputs are common mode.

13. When setting up the current limiter filter consisting of R120 and C107, R120 should be 4.7kΩ or larger, and C107 and R120 should function as a filter for the recovery current. This filter masks the recovery current due to internal circuits for the current limiter input (pin 26) and the C107 discharge operation determines the PWM off time (by making the current limiter input a low impedance). See the figures.



For recovery current masking:

$$t_{MASK} = \frac{48}{fosc} \text{ to } \frac{64}{fosc} \text{ [SEC]}$$

@MD8 = 1

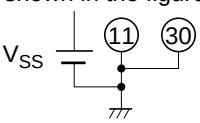
$$t_{MASK} = \frac{24}{fosc} \text{ to } \frac{32}{fosc} \text{ [SEC]}$$

@MD8 = 0

14. Use the formula below as a guideline for determining the values of R103, R104, and R122 to R124 when a Hall IC is used.

    R103 // R104 = R122 to R124 < 20kΩ

15. Take the current limiter input current (see the electrical characteristics) into consideration when determining the values for R106 and R107.
16. Determine the values of R108 to R119 based on the characteristics of the output power transistors used and the output driver characteristics (see the electrical characteristics).
17. Design the wiring in applications so that the potential of the pin 11 ground (the small-signal ground) does not become higher than that of the pin 30 ground (the output stage ground) as shown in the figure.



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit	Note
Power-supply voltage	V_{SS}	5.5	V	1
	V_{PS}	V_{SS} to 50	V	2
Input voltage	V_{IN}	V_{SS}	V	3
Output voltage	Vout	50	V	4
Output current	Iout	30	mA	5
Allowable power dissipation	P_T	0.8	W	
Operating temperature	Topr	–20 to 70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. A surge voltage of 6.0V is allowed for up to 10ms. Note that the operating range is as follows:
V_{SS} = 4.25 to 5.5V
2. The maximum is VSS if bipolar transistors are used as the output transistors.
The maximum is 50 V if bipolar transistors are used as the output transistors.
3. Applies to the logic input pins 1, 2, 3, 5, and 9, and to the analog input pins 17, 20, 24, 26 to 29, and 37 to 42.
4. Applies to the output pins 32, 34, and 36, and to pin 7, the monitor output pin.
5. Applies to the output pins 31 to 36. The maximum value for the monitor output pin is 10mA.

Electrical Characteristics

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Notes
Current drain		I_{SSO}	—	3.0	6.5	mA	MD0 to 2 = 0, V_{SS} = 5.5V	21	6
		I_{SS}	—	15	25	mA	MD0 to 2 = 1, V_{SS} = 5.5V		
		I_{PSO}	—	0.13	0.5	mA	MD0 to 2 = 0, V_{PS} = 50V	25	6
		I_{PS}	—	2.5	3.5	mA	MD0 to 2 = 1, no load, V_{PS} = 50V		
Logic inputs	Input low-level current	I_{IL}	—	–50	–100	µA		1 to 3, 5, 9	
	Input high-level current	I_{IH}	—	0	±10	µA			
	Input low-level voltage	V_{IL}	—	—	1.5	V			
	Input high-level voltage	V_{IH}	3.5	—	—	V			
	Clock frequency	f_{CLK}	4	—	20	MHz		9	
Logic outputs	Output high-level voltage	V_{OH1}	3.5	4.6	—	V	I_{OH} = 0.5mA	4, 6, 8, 10	
	Output low-level voltage	V_{OL1}	—	0.25	0.4	V	I_{OL}= 0.5mA		
Hall amplifier	Input resistance	Rh	—	10	±25%	kΩ		37 to 42	
	Common-mode input voltage range	Vh	1.5	—	V_{SS}–1.5	V			
	Differential-mode input voltage range	Vd	70	—	V_{SS}/2	mV			
	Hysteresis	V_{HYS}	—	40	—	mV	Rh = 400Ω		1, 2
Output drivers	Output high-level voltage	V_{OH2}	V_{PS}–1.8	V_{PS}–1.6	—	V	I_{OH} = 20mA, V_{PS} = V_{SS}	31, 33, 35	
		V_{OH2}	10	12.5	15	V	I_{OH} = 1mA, V_{PS} = 24V		
		V_{OH2}	5.5	9.0	—	V	I_{OH} = 1mA, V_{PS} = 12V		

Electrical Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Notes
Output drivers	Output leakage current	I_{LEAK}	—	—	±100	µA	V_{OH1} = 50V	32, 34, 36	
	Output low-level voltage	V_{OL2}	—	0.15	0.3	V	I_{OL} = 20mA	31 to 36	
	Output response time	T_{PHI}	—	—	1.0	µs	I_O = 10mA		3
		T_{PLH}	—	—	1.0	µs			
PWM oscillator and	Oscillator low-level voltage	V_L	—	1.1	±10%	V		12	
PWM comparator	Oscillator high-level voltage	V_H	—	2.8	±10%	V			
	Oscillator frequency range	f_{PWM}	2	—	30	kHz			2
	Oscillator frequency precision	ferr1	—	7.7	±10%	kHz	$f_{PWM} \times 1$, R1 = 6.2kΩ, C106 = 1000pF		
	Comparator hysteresis	V_{PHYS}	—	50	—	mV			2
Current limiter	Input current	I_{IN1}	—	—	±10	µA	Vi = 0 to 2V	24, 26	
	Offset voltage	V_{OFF}	–15	–25	–40	mV	Vi = 0.5 to 2V	26	
Speed detection amplifier	Common-mode input voltage range	V_{CM}	1.5	—	V_{SS} –1.5	V		28, 29	
	Differential-mode input voltage range	V_{DIFF}	60	—	V_{SS}	mV_{P-P}			
	Gain	Gain	—	32	—	dB	f = 1kHz		2
	Input current	I_{IN2}	—	—	±20	µA	Vi = 1.4V		
		I_{28}	–146	–95	–62	µA	Vi = 0V		
		I_{29}	–67	–53	–39	µA	Vi = 0V		
	Input current ratio	Iratio	1.45	—	2.25	—	I_{28} / I_{29}		
	Input sensitivity	V_S	15	—	—	mV		6	2

Electrical Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Notes
Clock oscillator	Oscillator frequency range	fosc	4	—	—	MHz	X'tal	9, 10	
	Oscillator frequency precision	ferr2	—	—	±0.01	%	X'tal = 8MHz		2
Program-mable discrimi-nator	Count range	N	1024	—	4095	Count		14, 16	
	Operating frequency	fdis	—	—	20	MHz			4
	Count error	DC	0	—	1LSB	—			
Charge pump	R1 voltage	V_{R1}	—	1.16	±10%	V	R1 = 1.5kΩ	19	
	Charge current	I_{CP+}	—	190	±10%	µA	R1 = 1.5kΩ,	16	
	Discharge current	I_{CP-}	—	190	±10%	µA	Vo = 2.0V		
	Current ratio	I_{CP+}/I_{CP-}	0.8	1.0	1.2	—			
	Leakage current	Ioff1	—	—	±100	nA	Vi = 1.5V		
	Clamp voltage	Vclamp	2.8	3.0	—	V			
Digital ready	Lock range manufacturing variation	ΔN	—	—	±25	%		7	
Pre-charge	Clamp voltage (1)	Vcp(1)	—	Vp	±10%	V		16	
Buffer amplifier	Internal reference voltage	Vref	—	1.15	±10%	V		16	
	Output resistance	Ro	9.8	14	18.2	kΩ		18	
	Maximum output voltage	$V_{B(MAX)}$	—	0.7	±10%	V			
	Voltage gain	G_B	–8	–6	–4	dB			
Error amplifier	Input current	I_{IN3}	—	—	±150	nA	Vi = 1.5V	17, 27	
	Offset voltage	Voff	—	–25	–50	mV			
	Voltage gain	Ge	—	60	—	dB	Vi = 2.5V		2
	Gain-bandwidth product	Be	—	0.1	—	MHz			2
	Feedback resistance	Rif	—	40	±25%	kΩ	V_{SS} = 5V		

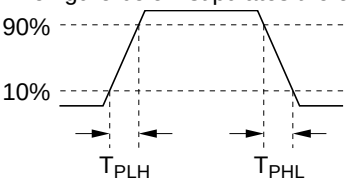
Electrical Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Notes
Integrating amplifier	Internal reference voltage	Vp	—	2.2	±10%	V	DD6 to 8 = 0	15, 16	
	Internal reference voltage difference	ΔVp	—	2.2+ΔVp	±10%	V			
	Input current	I_{IN4}	—	—	±250	nA	Vi = 1.5V		
	Output voltage	V_{OH3}	2.75	3.0	—	V	Io = 0.5mA		
		V_{OL3}	—	—	0.9	V	Io = 0.5mA		
	Voltage gain	G_I	—	60	—	dB	Vi = 2.5V		2
	Gain-bandwidth product	B_I	—	0.3	—	MHz			2
PLL and offset discriminator output	Output high-level voltage	V_{OH4}	—	3.6	±10%	V	Io = 0.1mA	13, 14	
	Output low-level voltage	V_{OL4}	—	0.1	0.2	V			
Monitor output	Output leakage current	I_{LEAK2}	—	—	50	µA	V_{OH} = 50V	7	
	Output low-level voltage	V_{OL5}	—	0.2	0.4	V	I_{OL} = 10mA		
Stuck rotor protector	Minimum detection time	t_{LP}	—	40	±25%	ms	C105 = 0.47µF	23	2
	Output off time	t_{OFF}	—	165	±25%	ms			
	High-level	V_{LH1}	3.0	3.2	—	V			
	voltage	V_{LH2}	2.5	2.7	—	V			
	Low-level voltage	V_{LL}	—	1.4	1.6	V			
	Potential	ΔV1	—	1.9	±10%	V	V_{LH1}–V_{LL}		
	difference	ΔV2	—	1.35	±10%	V	V_{LH2}–V_{LL}		
	Detection-time sink current	I_{SINK}	—	25	±30%	µA	Pin 23 voltage = 2.5V		
	Output off source current	I_{Source}	—	5.0	±30%	µA	Pin 23 voltage = 2.5V		
	Standby-mode source current	I_S	—	4.7	±35%	mA	Pin 23 voltage = V_{LH}		2

Electrical Characteristics (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pins	Notes
LVI	Internal reference voltage	Vsd	1.13	1.21	1.29	V	Turn on	20	
	Hysteresis current	I_{HYS}	—	50	±25%	µA			
	Output voltage maintained range	V_{LV}	2.0	—	—	V		21	
P.O.R	Delay time	t_{POR}	—	24.5	±25%	ms	C108 = 0.47µF	8, 22	

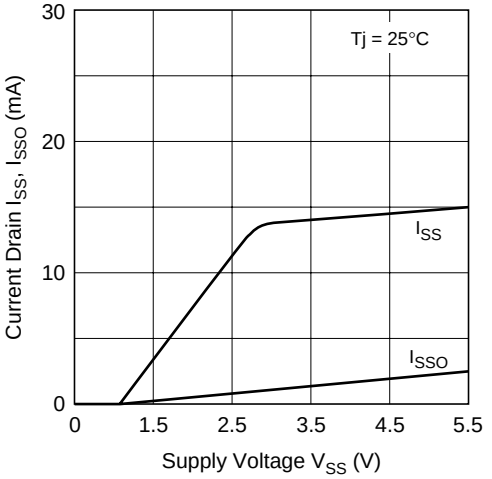
Notes:
1. Timing chart
2. Design target values. These are not tested at delivery time.
3. The figure below stipulates the output response time. This is not tested at delivery time.



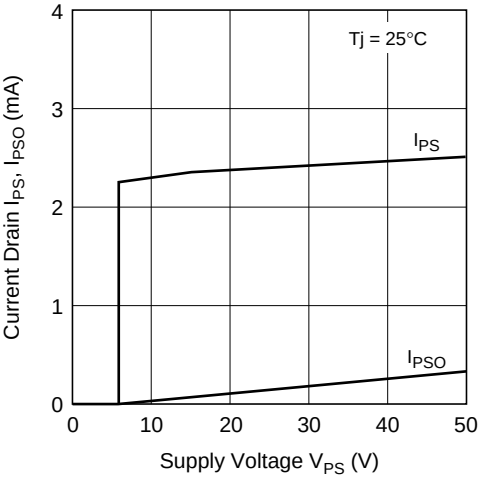
4. Stipulated at the discriminator input frequency.
5. See the timing charts.
6. Stipulated at conditions in which the OSC input is fixed.

Reference Data

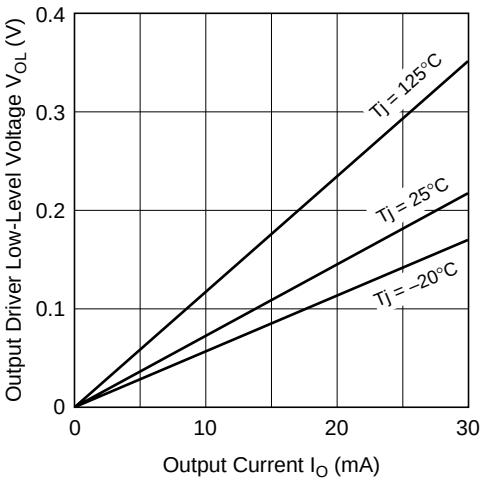
Current Drain vs. Supply Voltage



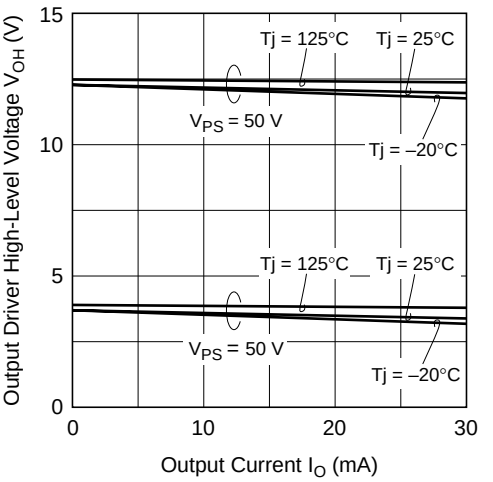
Current Drain vs. Supply Voltage



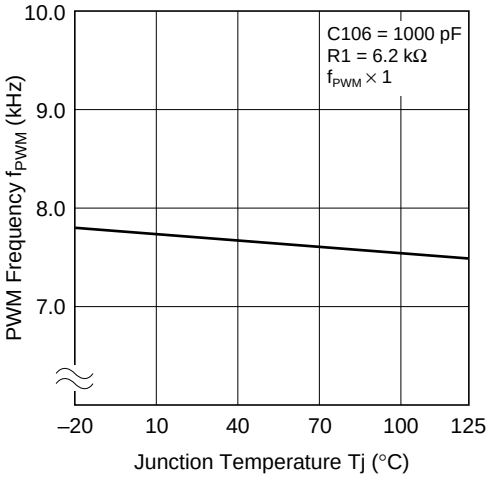
Output Driver Low-Level Voltage vs. Output Current



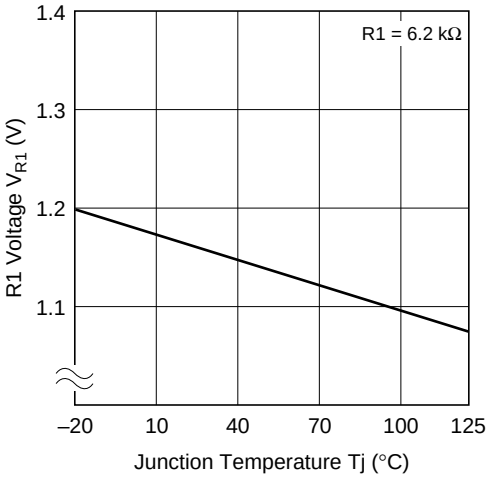
Output Driver High-Level Voltage vs. Output Current



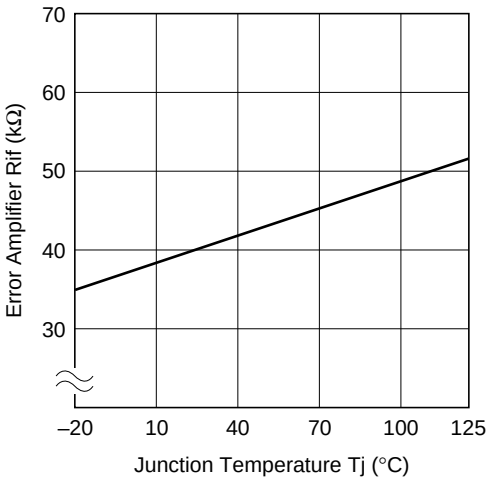
PWM Frequency vs. Junction Temperature



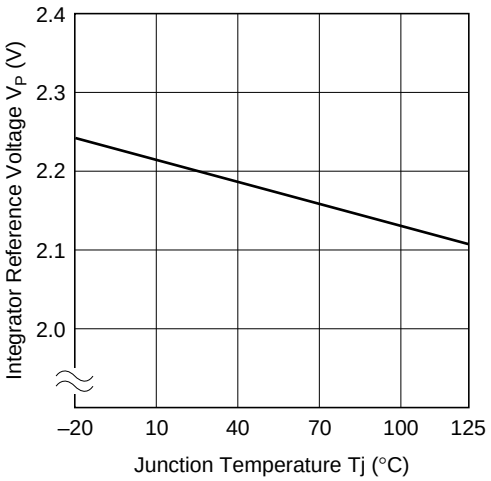
R1 Voltage vs. Junction Temperature



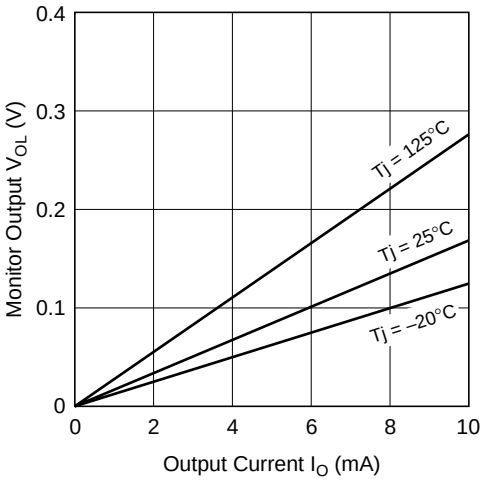
Error Amplifier Rif vs. Junction Temperature



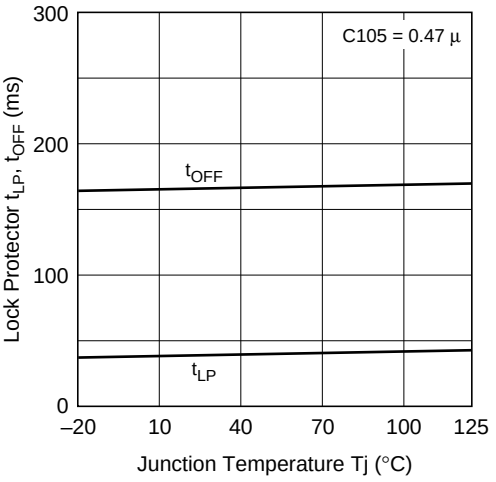
Integrator vs. Junction Temperature



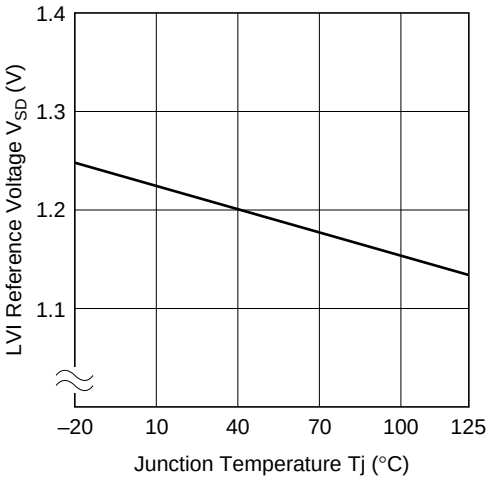
Monitor Output vs. Output Current



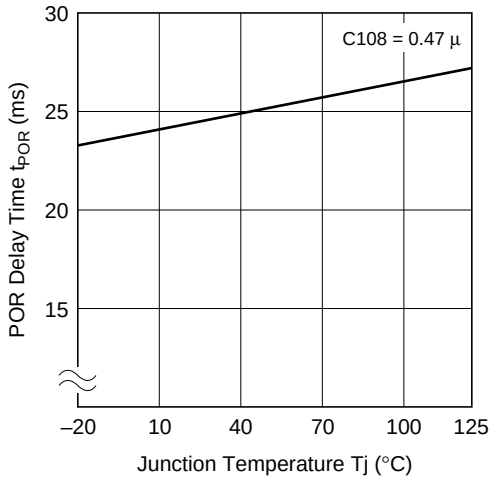
Lock Protector vs. Junction Temperature



LVI Reference Voltage vs. Junction Temperature

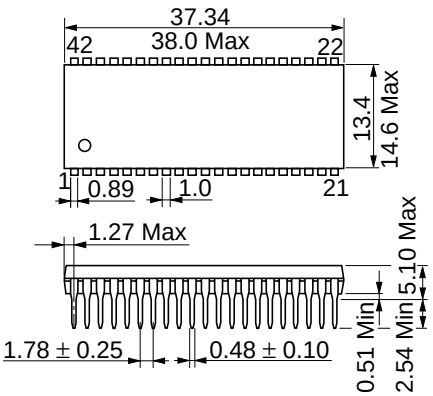


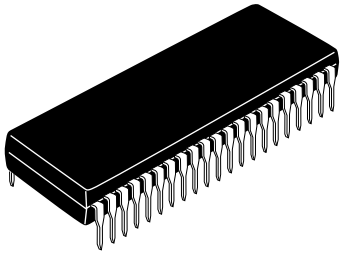
POR Delay Time vs. Junction Temperature

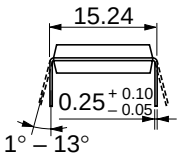


Package Dimensions

Unit: mm







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