HCPL-7723/0723

50 MBd 2 ns PWD High Speed CMOS Optocoupler

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

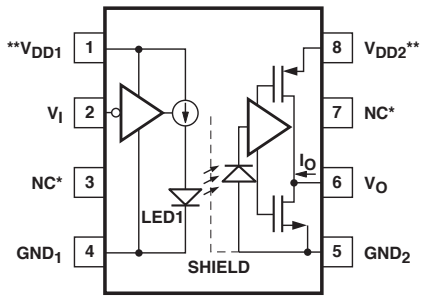
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Available in either 8-pin DIP or SO-8 package style respectively, the HCPL-7723 or HCPL-0723 optocoupler utilize the latest CMOS IC technology to achieve outstanding speed performance of minimum 50 MBd data rate and 2 ns maximum pulse width distortion.

Basic building blocks of HCPL-7723/0723 are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



* PIN 3 IS THE ANODE OF THE INTERNAL LED AND MUST BE LEFT UNCONNECTED FOR GUARANTEED DATASHEET PERFORMANCE. PIN 7 IS NOT CONNECTED INTERNALLY.

** A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 1 AND 4, AND 5 AND 8.

TRUTH TABLE
(POSITIVE LOGIC)

V_I, INPUT	LED1	V_O, OUTPUT
H	OFF	H
L	ON	L

Features

- +5 V CMOS compatibility
- High speed: 50 MBd min.
- 2 ns max. pulse width distortion
- 22 ns max. prop. delay
- 16 ns max. prop. delay skew
- 10 kV/μs min. common mode rejection
- –40 to 85°C temperature range
- Safety and regulatory approvals:

  UL recognized
  – 5000 V_{rms} for 1 min. per UL1577 for HCPL-7723 for option 020
  – 3750 V_{rms} for 1 min. per UL1577 for HCPL-0723

  CSA component acceptance notice #5

  IEC/EN/DIN EN 60747-5-5
  – V_{iorm} = 630 V_{peak} for HCPL-7723 option 060
  – V_{iorm} = 567 V_{peak} for HCPL-0723 option 060

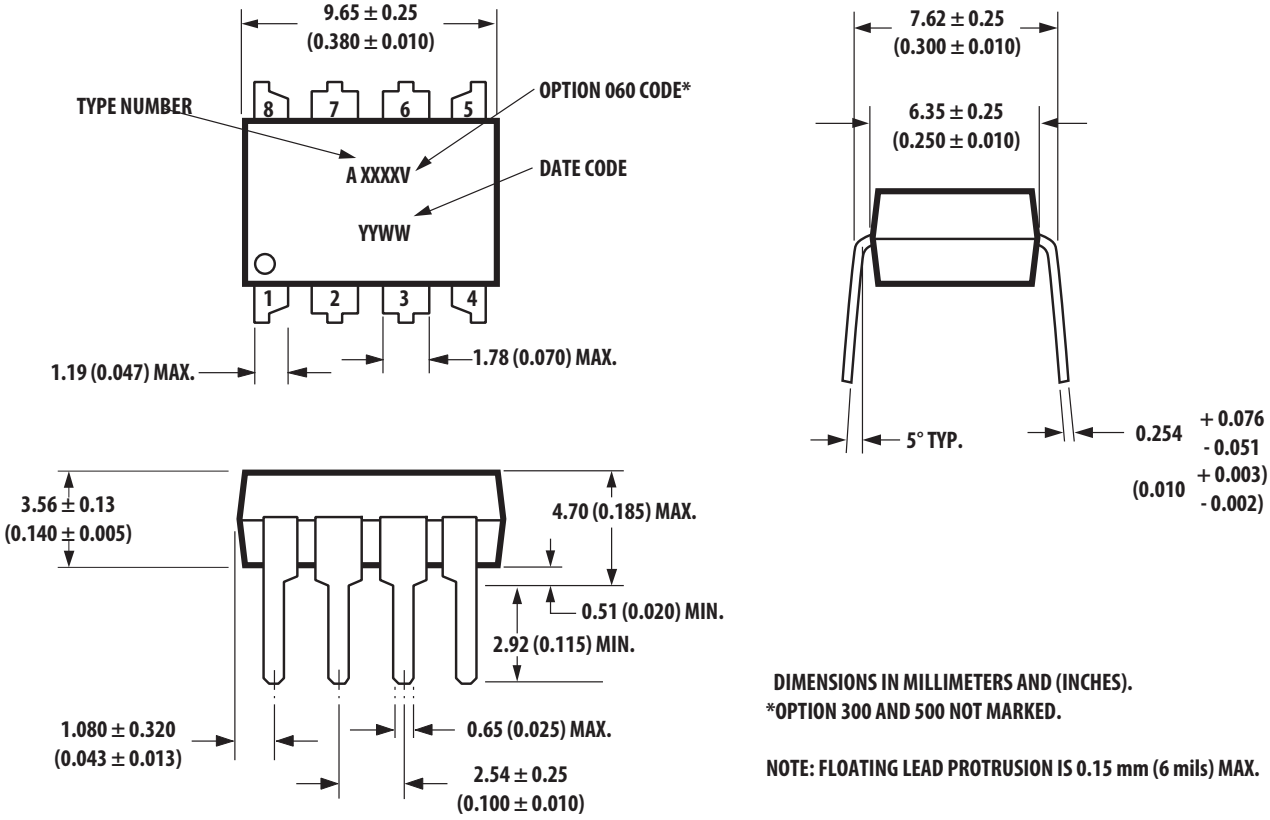
Applications

- Digital fieldbus isolation: CC-Link, DeviceNet, Profibus, SDS, Isolated A/D or D/A conversion
- Multiplexed data transmission
- High speed digital input/output
- Computer peripheral interface
- Microprocessor system interface

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

Package Outline Drawings

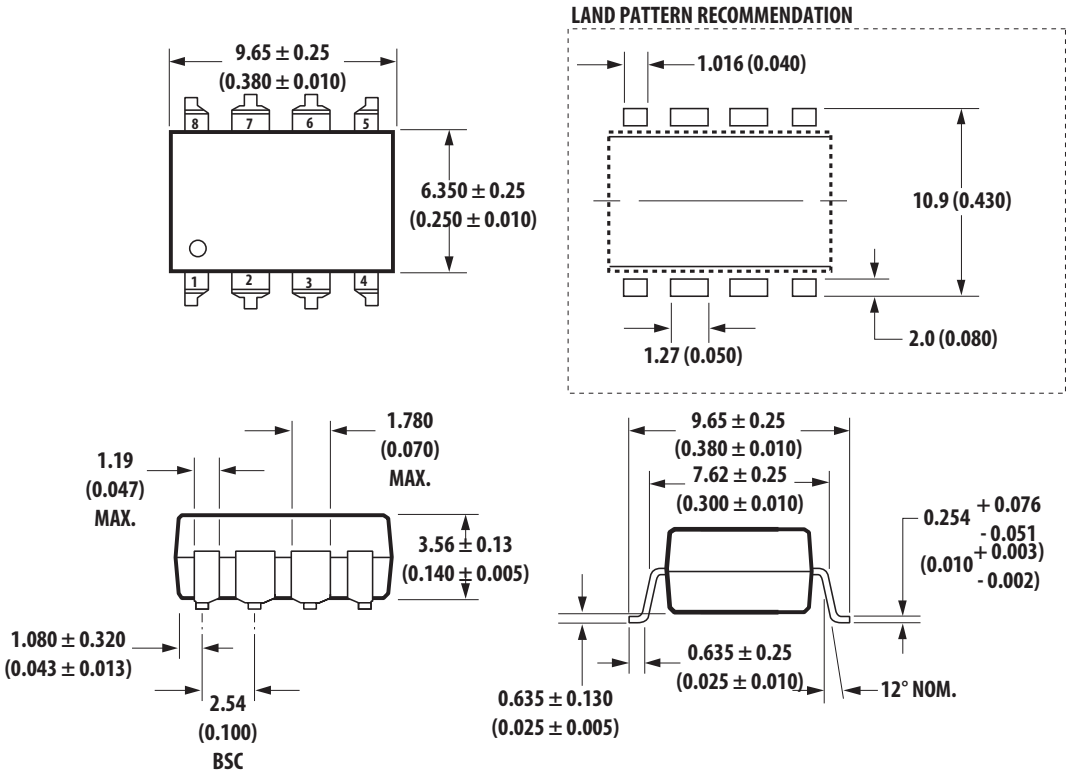
HCPL-7723 8-Pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).
*OPTION 300 AND 500 NOT MARKED.

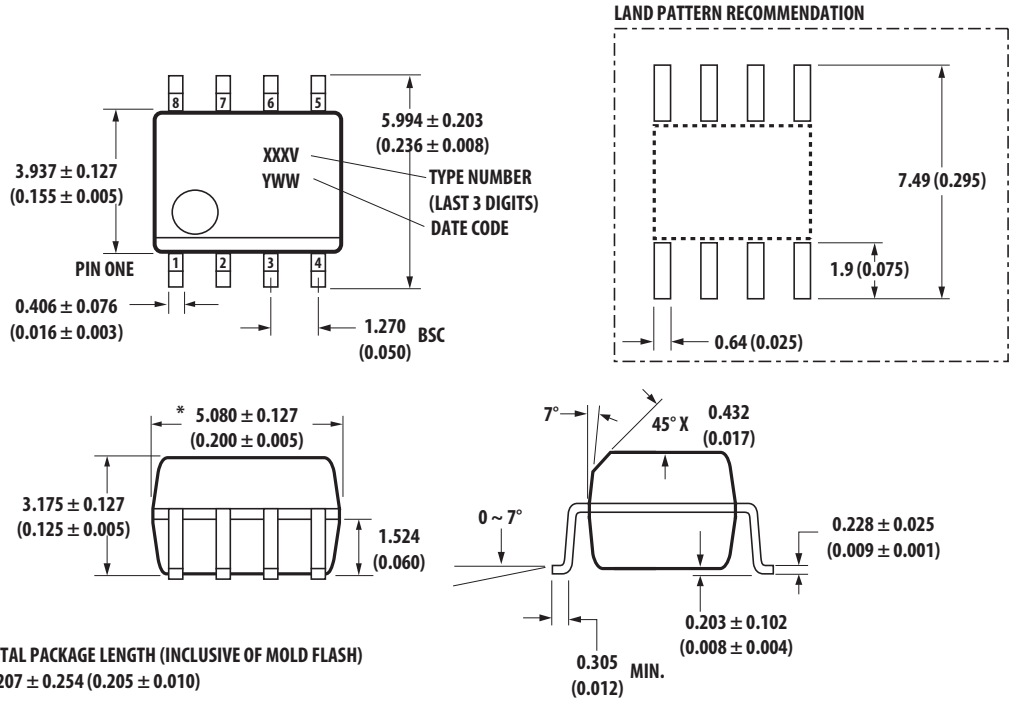
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

HCPL-7723 Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

HCPL-0723 Small Outline SO-8 Package



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES). LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

OPTION NUMBER 500 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Device Selection Guide

8-Pin DIP (300 mil)	Small Outline SO-8
HCPL-7723	HCPL-0723

Ordering Information

HCPL-0723 and HCPL-7723 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	non RoHS Compliant							
HCPL-7723	-000E	no option	300 mil DIP-8						50 per tube
	-300E	-300		X	X				50 per tube
	-500E	-500		X	X	X			1000 per reel
	-020E	-020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	-060						X	50 per tube
	-360E	-360		X	X			X	50 per tube
	-560E	-560		X	X	X		X	1000 per reel
HCPL-0723	-000E	no option	SO-8	X					100 per tube
	-500E	-500		X		X			1500 per reel
	-060E	-060		X				X	100 per tube
	-560E	-560		X		X		X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:
HCPL-7723-560E to order product of Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliant.

Example 2:
HCPL-0723 to order product of Small Outline SO-8 package in Tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

Regulatory Information

The HCPL-7723/0723 have been approved by the following organizations:

UL
Recognized under UL1577, component recognition program, File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA88324.

IEC/EN/DIN EN 60747-5-5

Approved with Maximum Working Insulation Voltage:
V_{iorm} = 567 V_{peak} for HCPL-0723,
V_{iorm} = 630 V_{peak} for HCPL-7723

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Insulation and Safety Related Specifications

		Value			
Parameter	**Symbol**	**7723**	**0723**	**Units**	**Conditions**
Minimum External Air Gap (Clearance)	L(I01)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	≥ 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs, which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

		Characteristic		
Description	**Symbol**	**HCPL-7723**	**HCPL-0723**	**Unit**
Installation classification per DIN VDE 0110, Table 1				
for rated mains voltage ≤ 150 V_{rms}		I – IV	I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	I – III	
for rated mains voltage ≤ 600 V_{rms}		I – IV	I – III	
Climatic Classification		55/85/21	55/85/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	630	567	V_{peak}
Input to Output Test Voltage, Method b*				
V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	1063	V_{peak}
Input to Output Test Voltage, Method a*				
V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1008	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175	150	°C
Input Current	$I_{S, INPUT}$	230	150	mA
Output Power	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	$\geq 10^9$	Ω

*Refer to the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	125	°C
Ambient Operating Temperature[1]	T_A	–40	85	°C
Supply Voltages	V_{DD1}, V_{DD2}	0	6.0	Volts
Input Voltage	V_I	–0.5	V_{DD1} +0.5	Volts
Output Voltage	V_O	–0.5	V_{DD2} +0.5	Volts
Average Output Current	I_O		10	mA
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	85	°C
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V
Logic Low Input Voltage	V_{IL}	0.0	0.8	V
Input Signal Rise and Fall Times	t_r, t_f		1.0	ms

Electrical Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at $T_A = +25°C$, $V_{DD1} = V_{DD2} = +5$ V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Logic Low Input Supply Current[2]	I_{DD1L}		8.4	10	mA	$V_I = 0$ V; Figure 1
Logic High Input Supply Current[2]	I_{DD1H}		0.6	3	mA	$V_I = V_{DD1}$; Figure 2
Output Supply Current	I_{DD2L}		2.1	5	mA	Figure 3
	I_{DD2H}		2.0	5	mA	Figure 4
Input Current	I_I	–10		10	µA	
Logic High Output Voltage	V_{OH}	4.4	5.0		V	$I_O = -20$ µA, $V_I = V_{IH}$
		4.0	4.8		V	$I_O = -4$ mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I = V_{IL}$
			0.5	1.0	V	$I_O = 4$ mA, $V_I = V_{IL}$

Switching Specifications

Test conditions that are not specified can be anywhere within the recommended operating range.

All typical specifications are at $T_A = +25°C$, $V_{DD1} = V_{DD2} = +5$ V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output[3]	t_{PHL}		16	22	ns	$C_L = 15$ pF CMOS Signal Levels; Figure 5
Propagation Delay Time to Logic High Output[3]	t_{PLH}		16	22	ns	$C_L = 15$ pF CMOS Signal Levels; Figure 5
Pulse Width	PW	20			ns	$C_L = 15$ pF CMOS Signal Levels
Maximum Data Rate		50			MBd	$C_L = 15$ pF CMOS Signal Levels
Pulse Width Distortion[4] $\lvert t_{PHL} - t_{PLH} \rvert$	$\lvert PWD \rvert$		1	2	ns	$C_L = 15$ pF CMOS Signal Levels; Figure 6
Propagation Delay Skew[5]	t_{PSK}			16	ns	$C_L = 15$ pF CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R		8		ns	$C_L = 15$ pF CMOS Signal Levels
Output Fall Time (90% - 10%)	t_F		6		ns	$C_L = 15$ pF CMOS Signal Levels
Common Mode Transient Immunity at Logic High Output[6]	$\lvert CM_H \rvert$	10	15		kV/µs	$V_{CM} = 1000$ V, $T_A = 25°C$, $V_I = V_{DD1}$, $V_O > 0.8\,V_{DD2}$
Common Mode Transient Immunity at Logic Low Output[6]	$\lvert CM_L \rvert$	10	15		kV/µs	$V_{CM} = 1000$ V, $T_A = 25°C$, $V_I = 0$ V, $V_O < 0.8$ V

Package Characteristics

All Typical Specifications are at $T_A = 25°C$.

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[7,8,9]	–7723 Option 020 –0723	V_{ISO}	3750 5000 3750			V rms	RH ≤ 50%, t = 1 min, $T_A = 25°C$
Input-Output Resistance[7]		R_{I-O}		10^{12}		Ω	$V_{I-O} = 500$ V dc
Input-Output Capacitance		C_{I-O}		0.6		pF	f = 1 MHz
Input Capacitance[10]		C_I		3.0		pF	
Input IC Junction-to-Case Thermal Resistance	–7723 –0723	θ_{jci}		145 160		°C/W	Thermocouple located at center underside of package
Output IC Junction-to-Case Thermal Resistance	–7723 –0723	θ_{jco}		145 135		°C/W	
Package Power Dissipation		P_{PD}			150	mW	

Notes:

1. Absolute Maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee functionality.
2. The LED is ON when V_I is low and OFF when V_I is high.
3. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the VI signal to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the VI signal to the 50% level of the rising edge of the V_O signal.
4. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
5. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
6. CMH is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CML is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
7. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
8. In accordance with UL1577, each HCPL-0723 is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). Each HCPL-7723 is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second (leakage detection current limit. $I_{I-O} \leq 5$ μA.)
9. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
10. C_I is the capacitance measured at pin 2 (V_I).

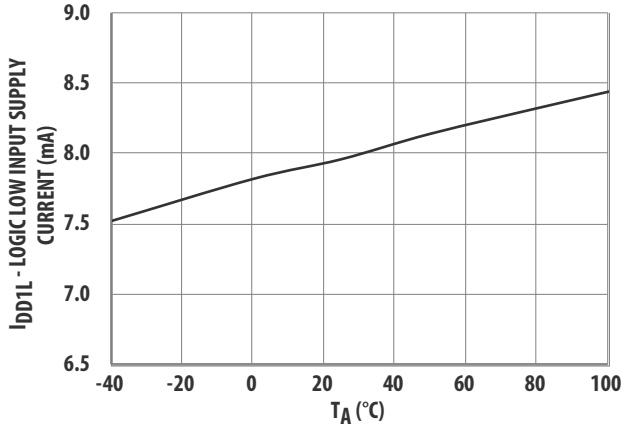


Figure 1: Typical Logic Low Input Supply Current vs. temperature

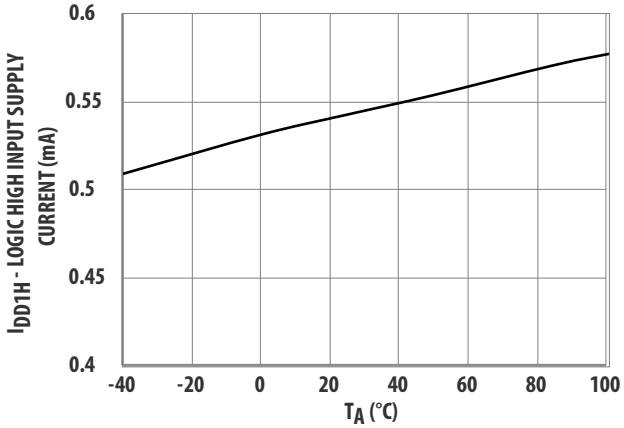


Figure 2. Typical Logic High Input Supply Current vs. temperature

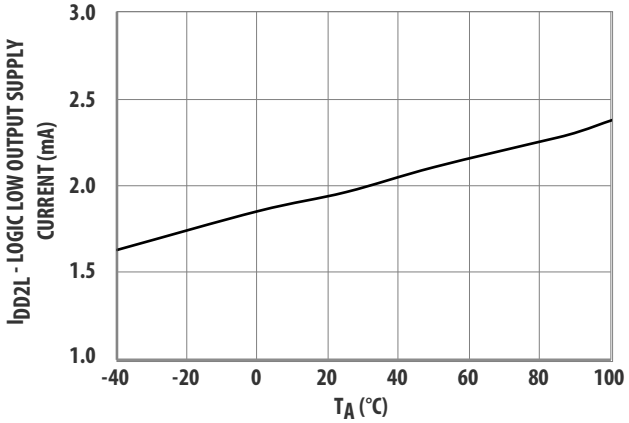


Figure 3. Typical Logic Low Output Supply Current vs. temperature

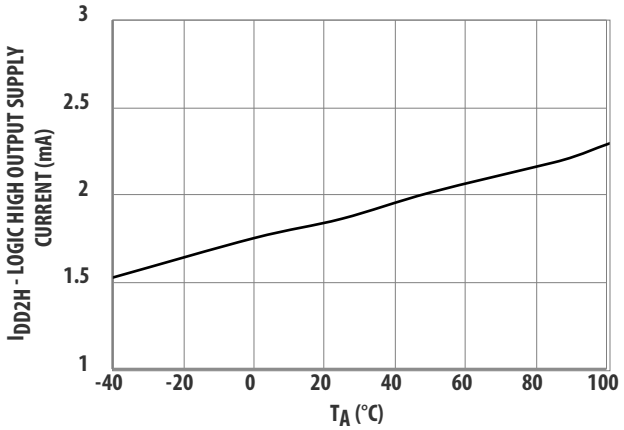


Figure 4. Typical Logic High Output Supply Current vs. temperature

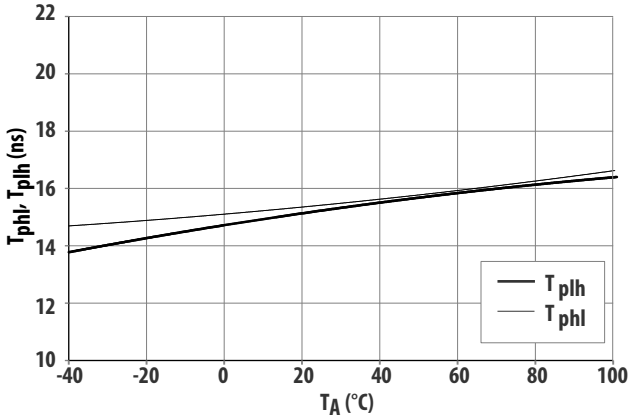


Figure 5. Typical propagation delay vs. temperature

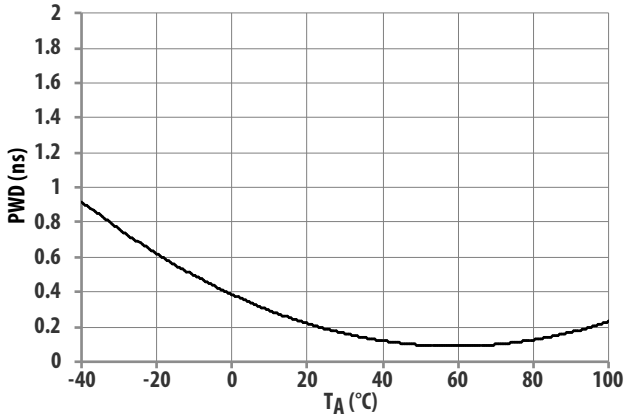


Figure 6. Typical pulse width distortion vs. temperature

Application Information

Bypassing and PC Board Layout

The HCPL-7723/0723 optocouplers are extremely easy to use. No external interface circuitry is required because the HCPL-7723/0723 use high-speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 7, the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 8 illustrates the recommended printed circuit board layout for the HCPL-7723/0723.

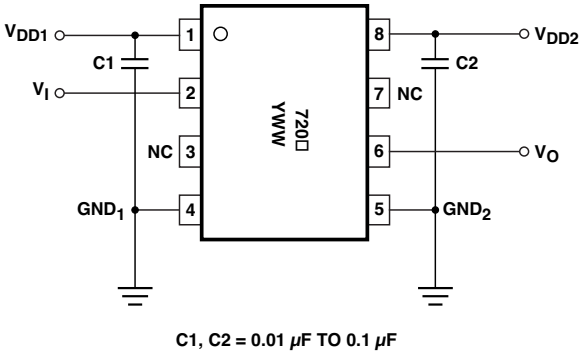


Figure 7. Functional diagram.

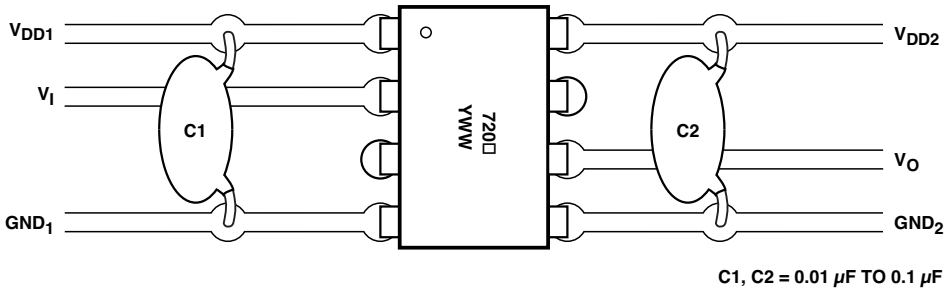


Figure 8. Recommended printed circuit board layout.

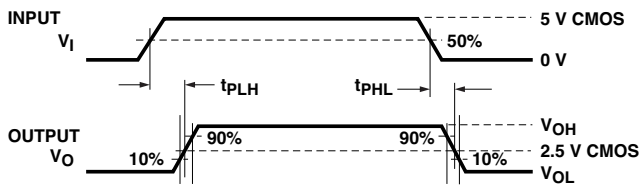


Figure 9. Timing diagram to illustrate propagation delay, tplh and tphl.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation Delay is a figure of merit which describes how quickly a logic signal propagates through a system as illustrated in Figure 9. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low.

Pulse-width distortion (PWD) is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable.

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

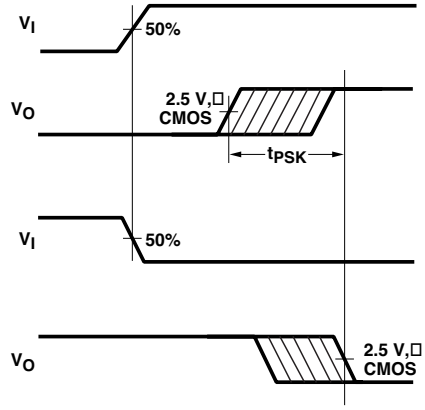


Figure 10. Timing diagram to illustrate propagation delay skew, tpsk.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and data lines being sent through the optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. In this case the data is assumed to be clocked off of the rising edge of the clock.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-7723/0723 optocouplers offer the advantage of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature and power supply ranges.

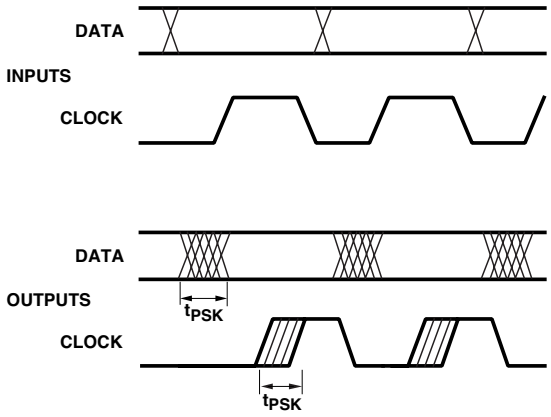


Figure 11. Parallel data transmission example.