

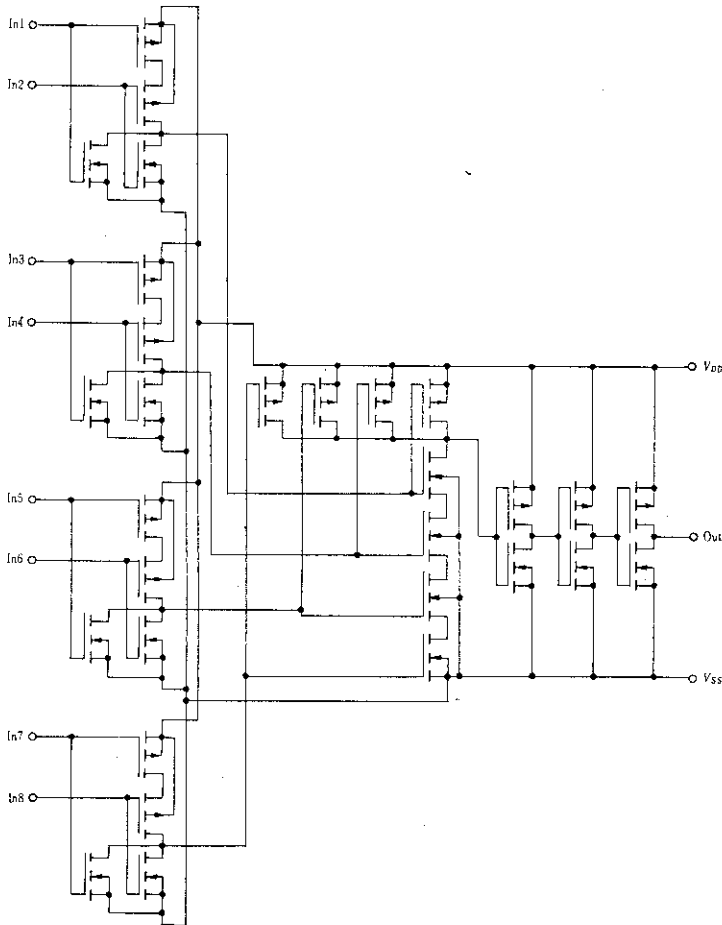
HD14078B

8-input NOR Gate

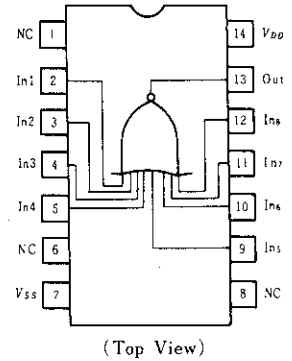
■ FEATURES

- Quiescent Current = 0.5nA typ/pkg @5V
- Noise Immunity = 45% of V_{DD} typ
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacements for CD4078B and MC14078B Series

■ CIRCUIT SCHEMATIC



■ PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

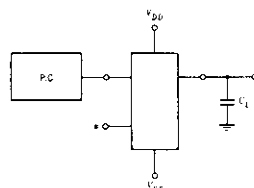
Characteristic	Symbol	$V_{DD}(V)$	Test Conditions	-40°C		25°C			85°C		Unit	
				min	max	min	typ	max	min	max		
Output Voltage	V_{OL}	5.0	$V_{in}=V_{DD}$	—	0.05	—	0	0.05	—	0.05	V	
		10		—	0.05	—	0	0.05	—	0.05		
		15		—	0.05	—	0	0.05	—	0.05		
	V_{OH}	5.0		$V_{in}=0$	4.95	—	4.95	5.0	—	4.95	—	V
		10			9.95	—	9.95	10	—	9.95	—	
		15			14.95	—	14.95	15	—	14.95	—	
Input Voltage	V_{IL}	5.0	$V_{out}=4.5V$		—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0V$		—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5V$		—	4.0	—	6.75	4.0	—	4.0	
	V_{IH}	5.0	$V_{out}=0.5V$	3.5	—	3.5	2.75	—	3.5	—	V	
		10	$V_{out}=1.0V$	7.0	—	7.0	5.50	—	7.0	—		
		15	$V_{out}=1.5V$	11.0	—	11.0	8.25	—	11.0	—		
Output Drive Current	I_{OH}	5.0	$V_{OH}=2.5V$	-2.5	—	-2.1	-4.2	—	-1.7	—	mA	
		5.0	$V_{OH}=4.6V$	-0.52	—	-0.44	-0.88	—	-0.36	—		
		10	$V_{OH}=9.5V$	-1.3	—	-1.1	-2.25	—	-0.9	—		
	I_{OL}	15	$V_{OH}=13.5V$	-3.6	—	-3.0	-8.8	—	-2.4	—		
		5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—		
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—		
Input Current	I_{in}	15		—	±0.3	—	±0.0001	±0.3	—	±1.0	μA	
				—	—	—	5.0	7.5	—	—	pF	
Quiescent Current	I_{DD}	5.0	Zero Signal, per Package	—	1.0	—	0.0005	1.0	—	7.5	μA	
		10		—	2.0	—	0.0010	2.0	—	15.0		
		15		—	4.0	—	0.0015	4.0	—	30.0		
Total Supply Current*	I_T	5.0	Dynamic $+I_{DD}$, $C_L=50pF$ per Gate, $f=1kHz$	—	—	—	0.3	—	—	—	μA	
		10		—	—	—	0.6	—	—	—		
		15		—	—	—	0.9	—	—	—		

* To calculate total supply current at frequency other than 1kHz.
 @ $V_{DD}=5.0V$ $I_T=10.3\mu A/kHz/f+I_{DD}$. @ $V_{DD}=10V$ $I_T=10.6\mu A/kHz/f+I_{DD}$. @ $V_{DD}=15V$ $I_T=10.9\mu A/kHz/f+I_{DD}$.

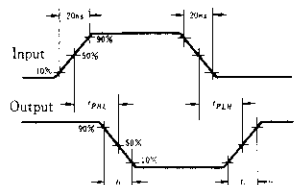
■ SWITCHING CHARACTERISTICS ($C_L=50pF$, $T_a=25^\circ C$)

Characteristic	Symbol	$V_{DD}(V)$	min	typ	max	Unit
Output Rise Time	t_r	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_f	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH}	5.0	—	200	400	ns
		10	—	80	160	
		15	—	60	120	
	t_{PHL}	5.0	—	200	400	ns
		10	—	80	160	
		15	—	60	120	

■ SWITCHING TIME TEST CIRCUIT



* All Unused inputs of OR, NOR gates must be connected to V_{SS}





Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

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