HD151011

Dual BCD Programmable Counter with Synchronous Preset Enable

HITACHI

ADE-205-100(Z)
Rev 0
April 1995

The HD151011 has BCD decimal two digits down counter and D-type Flip Flop. The counter can set up to max 99 counts and synchronous preset ($\overline{SPE}$) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
  tpd (CLK or $\overline{CLK}$ to Q) = 35 ns (typ)
- High output current
  Fanout of 10 LS TTL Loads
- Wide operating voltage
  Vcc = 2 to 6 V
- Low supply current (Ta = 25°C)
  Icc (Static) = 4 μA (max)

Hitachi semiconductor

Function Table

Control Inputs

CLR	PR	$\overline{SPE}$	C/$\overline{T}$	Mode	Operation Description
H	H	H	X	Generally count	Down count at the rise edge of clock (CLK), Down count at the fall edge of clock ($\overline{CLK}$)
X	X	L	X	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock ($\overline{CLK}$)
—	—	—	H	—	Clock inputs (CLK, $\overline{CLK}$) is CMOS level
—	—	—	L	—	Clock inputs (CLK, $\overline{CLK}$) is TTL level
L	H	—	—	Initialize of Q output	Initialize of Q = "L"
H	L	—	—	Initialize of Q output	Initialize of Q = "H"

H: High level

L: Low level

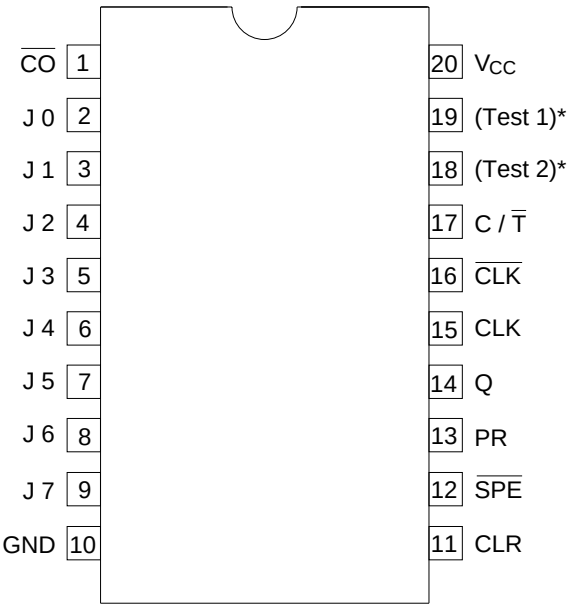
Z: Immaterial

—: Irrespective of condition

1. Synchronous preset ($\overline{SPE}$) input can set max 99 down counts.
2. When the count value is 0, the next clock pulse presets the data to invert the output.
3. CLR and PR inputs initialize output state.
4. Clock inputs (CLK, $\overline{CLK}$) is selectable CMOS level (V_{CC} = 2.0 to 6.0 V) and TTL level (V_{CC} = 4.5 to 5.5V) (Jn, C/$\overline{T}$, PR, CLR and $\overline{SPE}$ inputs are CMOS level)

Note: Don't set data exceeding 99 to Jn. (J0: LSB, J7: MSB)

Pin Arrangement



(Top view)

* Pins 18 and 19 are for function test only and should be open.

Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	C/T	Level change input for CLK, CLK (CMOS level or TTL level)	
	CLK, CLK	Clock inputs	CLK : Rise edge trigger
			CLK : Fall edge trigger
	SPE	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize "L" at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize "H" at Q output)	
Output pins	CO	Output for BCD decimal counter	
	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to 7.0	V
Input / output voltage	V_{IN} / V_{OUT}	–0.5 to V_{CC} +0.5	V
VCC, GND current	I_{CC}, I_{GND}	±50	mA
Output current / pin	I_{OUT}	±25	mA
Power dissipation	P_T	757	mW
Storage temperature	Tstg	–65 to 150	°C
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA

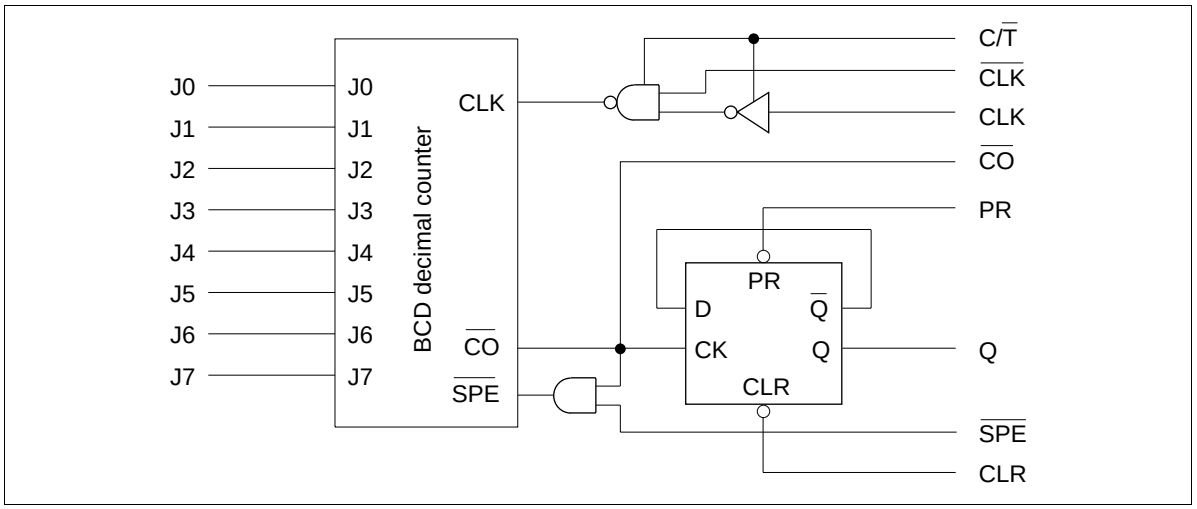
Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	2	—	6	V
Input / output voltage		V_{IN} / $_{OUT}$	0	—	V_{CC}	V
Operating temperature		Topr	–40	—	+85	°C
Input rise / fall time [*1]	V_{CC} = 2.5 V	tr, tf	0	—	1000	ns
	V_{CC} = 4.5 V		0	—	500	
	V_{CC} = 5.5 V		0	—	400	

Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

			Ta = 25°C			Ta = –40 to 85°C			
Item	**Symbol**	**V_{CC}**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
High level input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7
		4.5	3.15	—	—	3.15	—		C/$\overline{T}$, $\overline{SPE}$
		6.0	4.2	—	—	4.2	—		PR, CLR
		2.0	1.5	—	—	1.5	—		$\overline{CLK}$, CLK C/$\overline{T}$ = V_{IH}
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
		4.5 to 5.5	2.0	—	—	2.0	—		C/$\overline{T}$ = V_{IL}
Low level input voltage	V_{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7
		4.5	—	—	1.35	—	1.35		C/$\overline{T}$, SPE
		6.0	—	—	1.8	—	1.8		PR, CLR
		2.0	—	—	0.5	—	0.5		$\overline{CLK}$, CLK C/$\overline{T}$ = V_{IH}
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
		4.5 to 5.5	—	—	0.8	—	0.8		C/$\overline{T}$ = V_{IL}
High level output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	V_{IN} = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	4.31	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	5.80	—	5.63	—		I_{OH} = –5.2 mA
Low level output voltage	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	V_{IN} = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	0.17	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	0.18	0.26	—	0.33		I_{OL} = 5.2 mA
Input capacitance	IIN	6.0	—	—	±0.1	—	±1.0	mA	V_{IN} = V_{CC} or GND
Supply current	I_{CC}	6.0	—	—	4.0	—	40.0	mA	V_{IN} = V_{CC} or GND

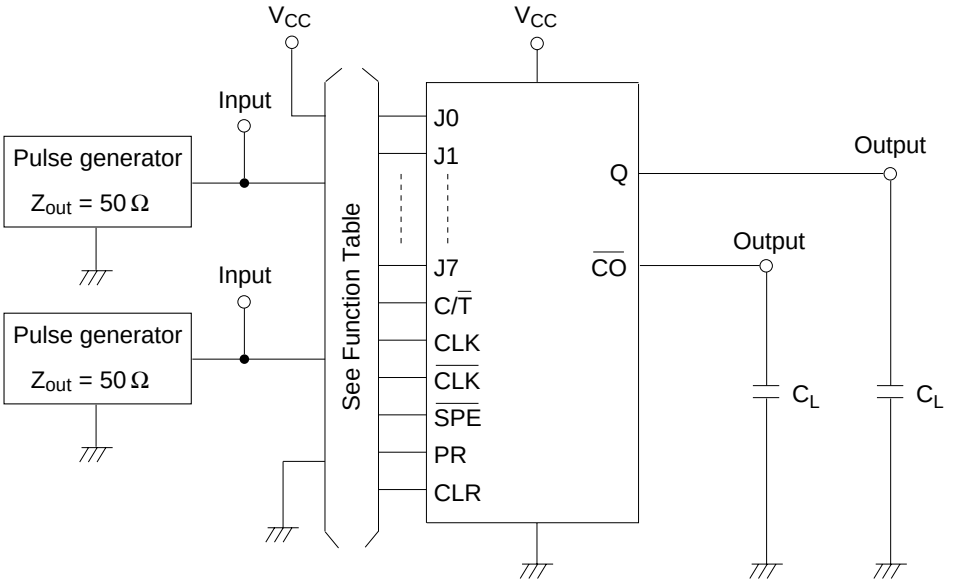
Switching Characteristics (C_L = 50 pF, tr = tf = 6 ns)

			Ta = 25°C			Ta = –40 to 85°C			
Item	**Symbol**	**V_{CC}**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	fmax	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise / fall time	t_{TLH}	2.0	—	30	75	—	95	ns	
	t_{THL}	4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH}	2.0	—	—	250	—	318	ns	CLK or $\overline{CLK}$ to $\overline{CO}$
	t_{PHL}	4.5	—	30	50	—	63		
		6.0	—	—	45	—	53		
	t_{PLH}	2.0	—	—	300	—	380		CLK or $\overline{CLK}$ to Q
	t_{PHL}	4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH}	2.0	—	—	150	—	185		PR or CLR to Q
	t_{PHL}	4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width	tw	2.0	80	—	—	100	—	ns	
(CLK, CLK, PR, CLR)		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	ts	2.0	100	—	—	125	—	ns	
(Jn - CLK, CLK)		4.5	20	—	—	25	—		
(SPE, CLK, CLK)		6.0	17	—	—	21	—		
Hold time	th	2.0	15	—	—	15	—	ns	
(Jn - CLK, CLK)		4.5	10	—	—	10	—		
(SPE, CLK, CLK)		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance	C_{PD}	—	—	48	—	—	—	pF	

Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

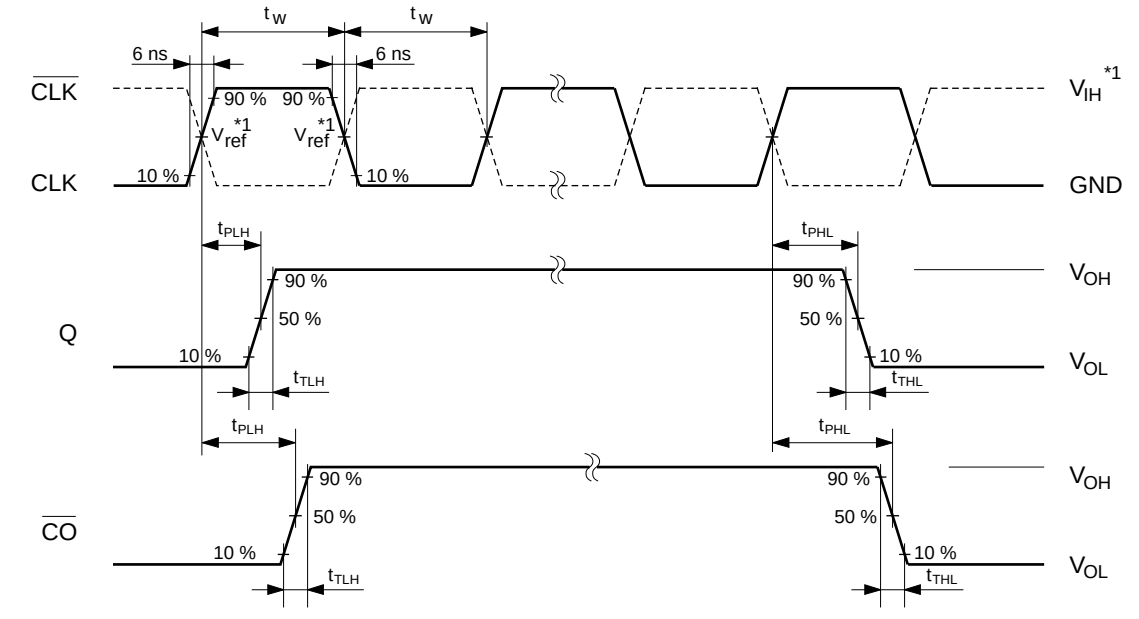
$$I_{CC}\ (opr) = C_{PD}\ V_{CC} \bullet f_{IN} + I_{CC}$$

- **Test Circuit**



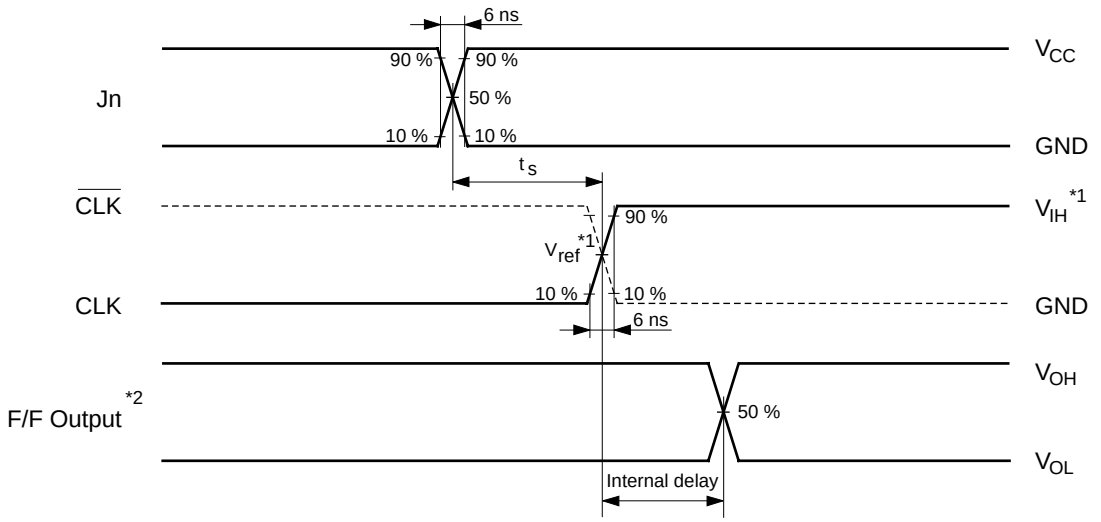
Note: 1. C_L includes probe and jig capacitance.

- **Waveforms – 1**



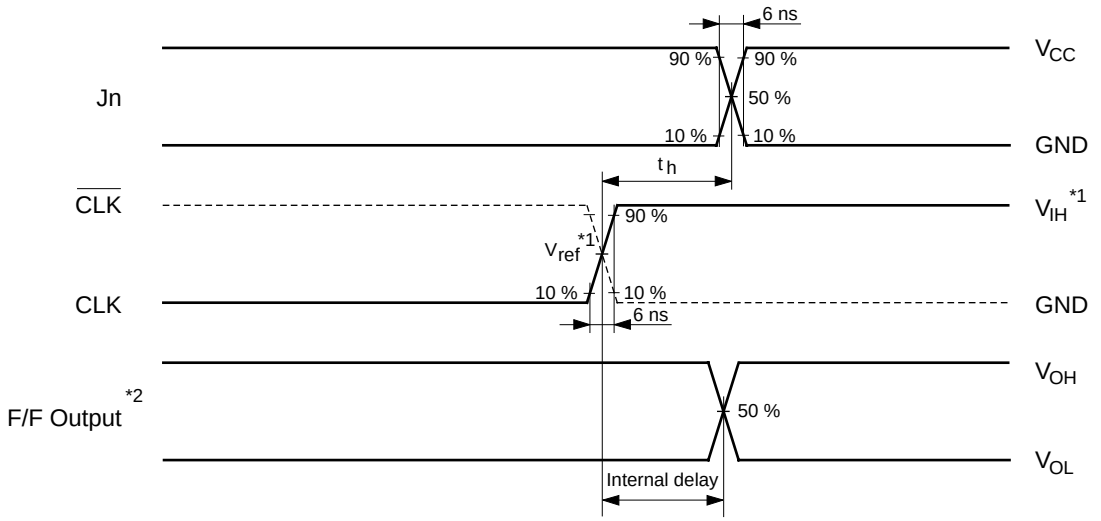
Note: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%

- **Waveforms – 2**



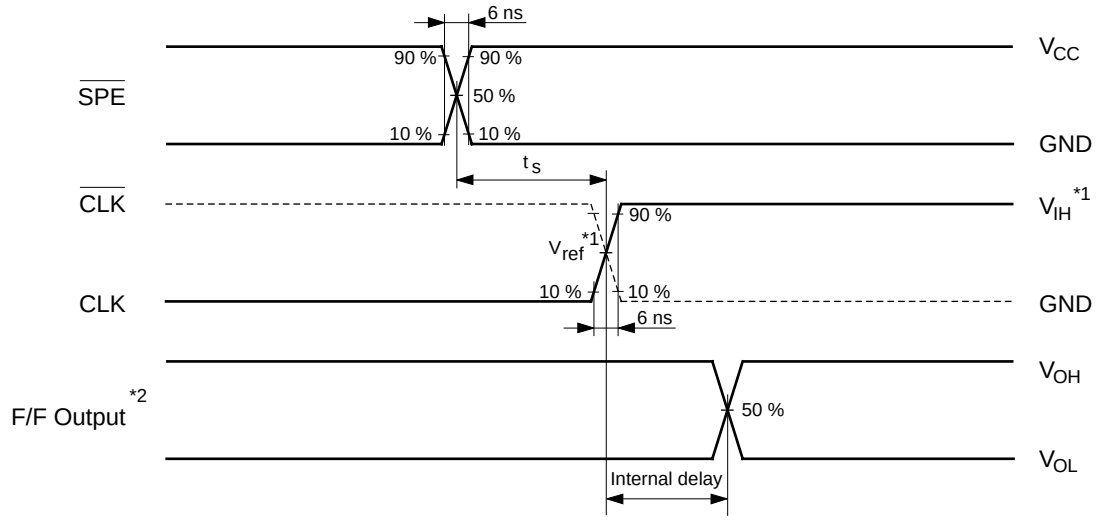
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 3**



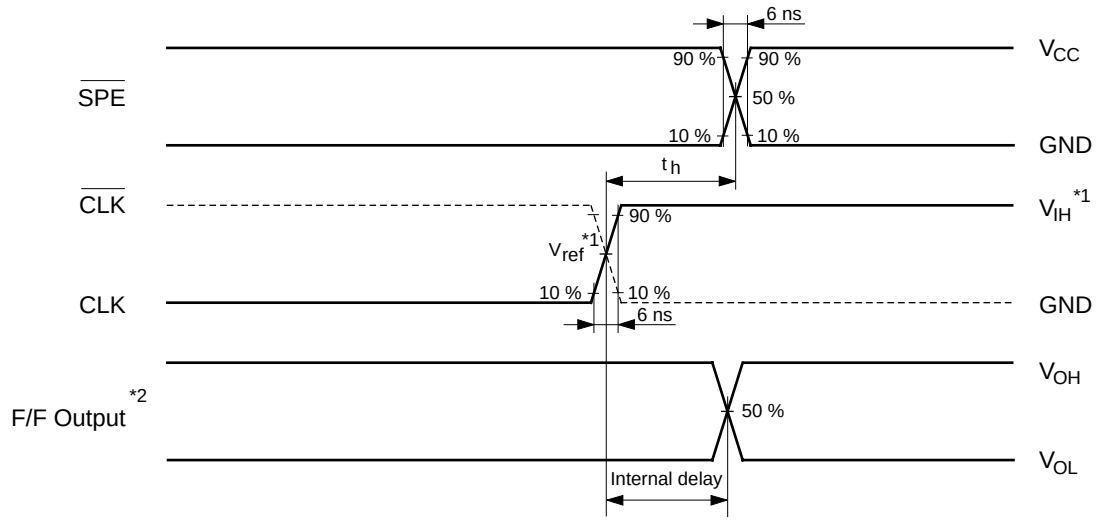
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 4**



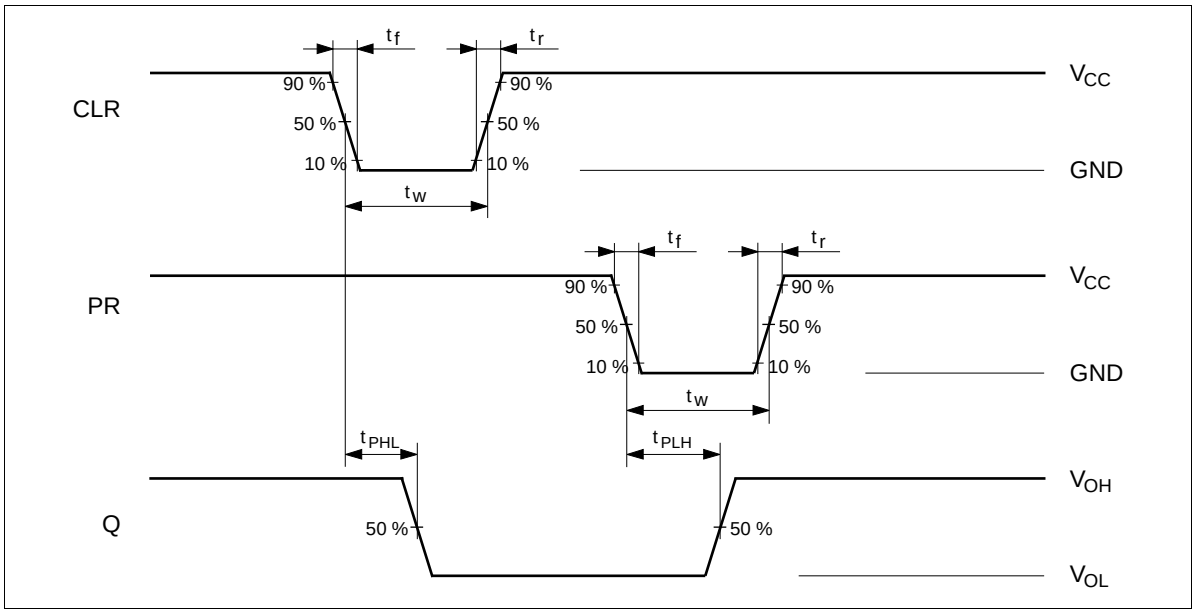
Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 5**

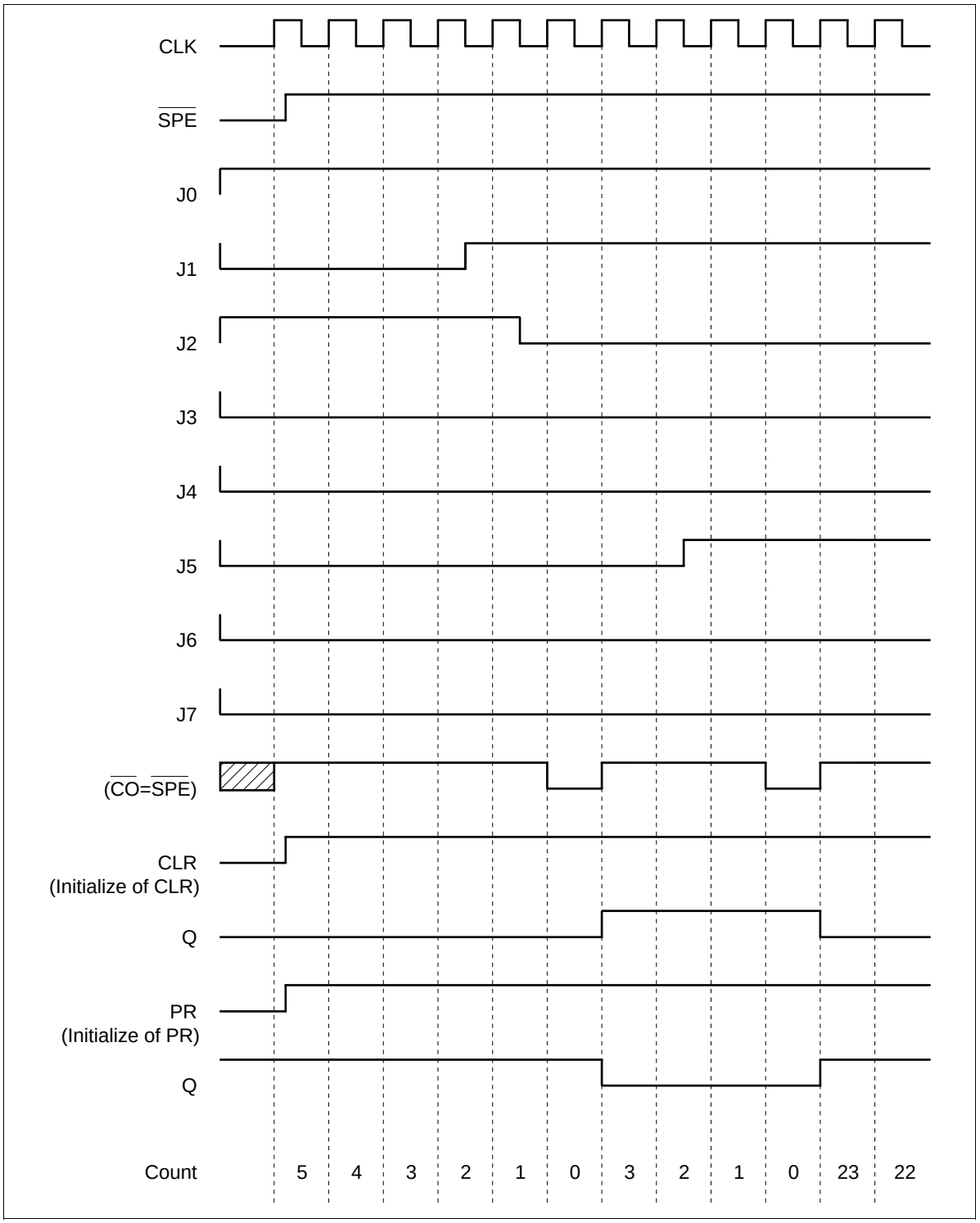


Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/T = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%
2. F/F output is internal signal of IC.

- **Waveforms – 6**



Timing Chart

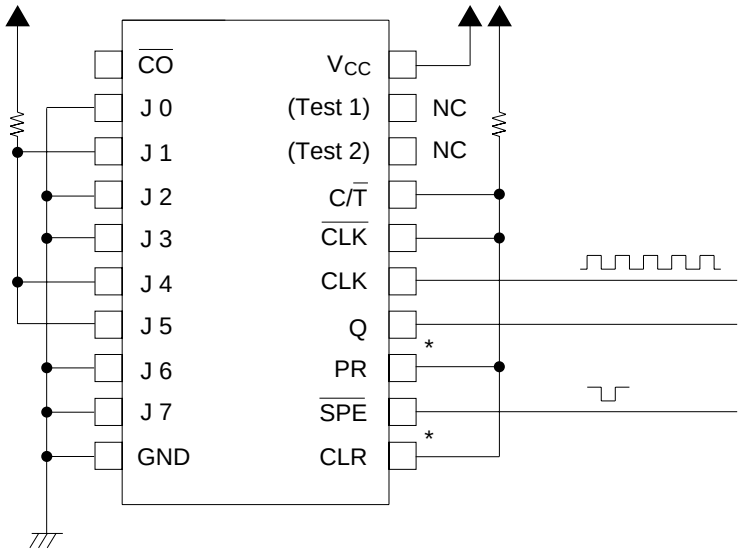


Example of Application Circuit

• AC Signal Generator for STN Type Liquid Crystal Panel

CLK ($\overline{CLK}$) : CMOS level input

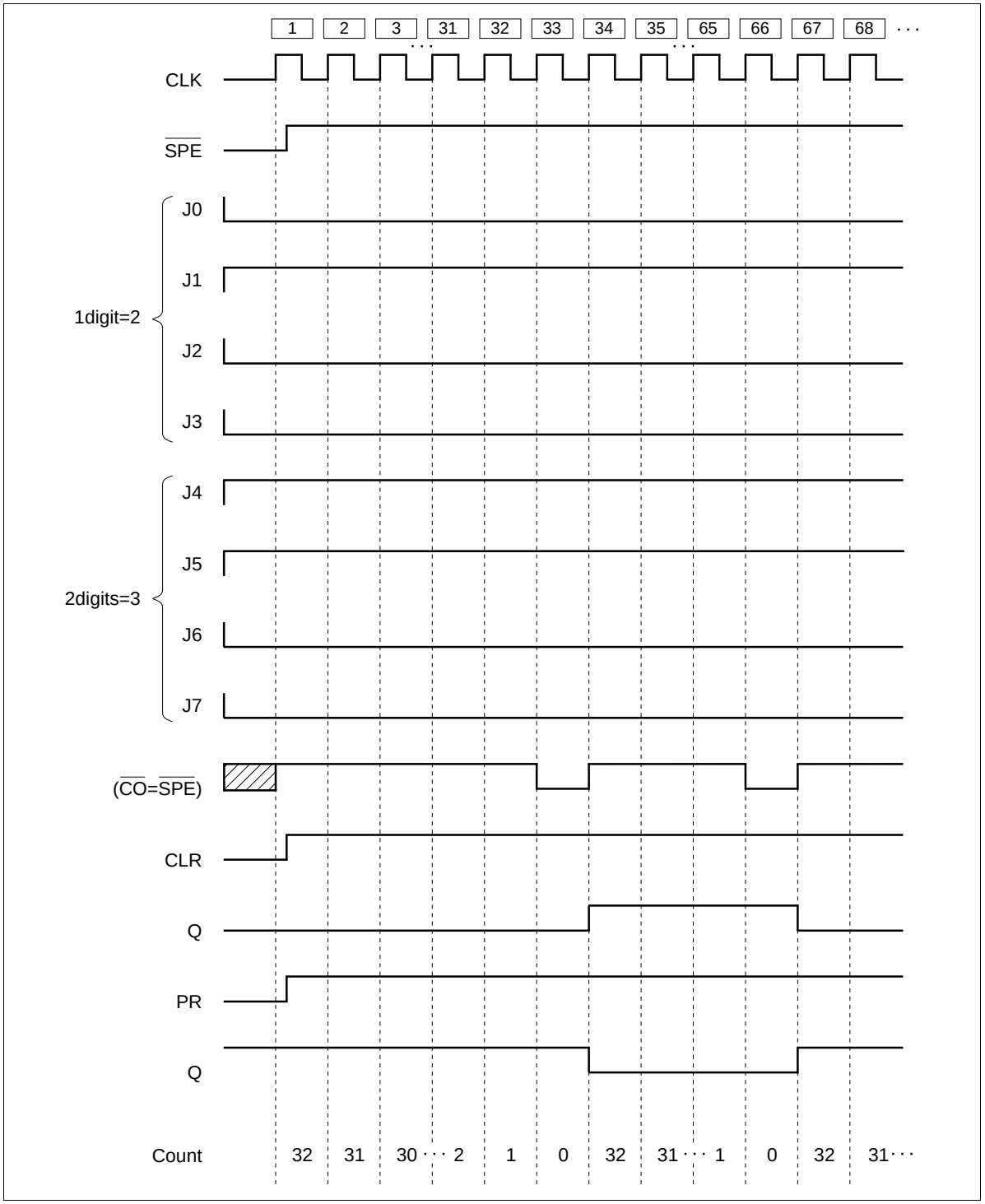
Initialize counter : 32



*When initializing output D-F/F apply "L"

Timing Chart

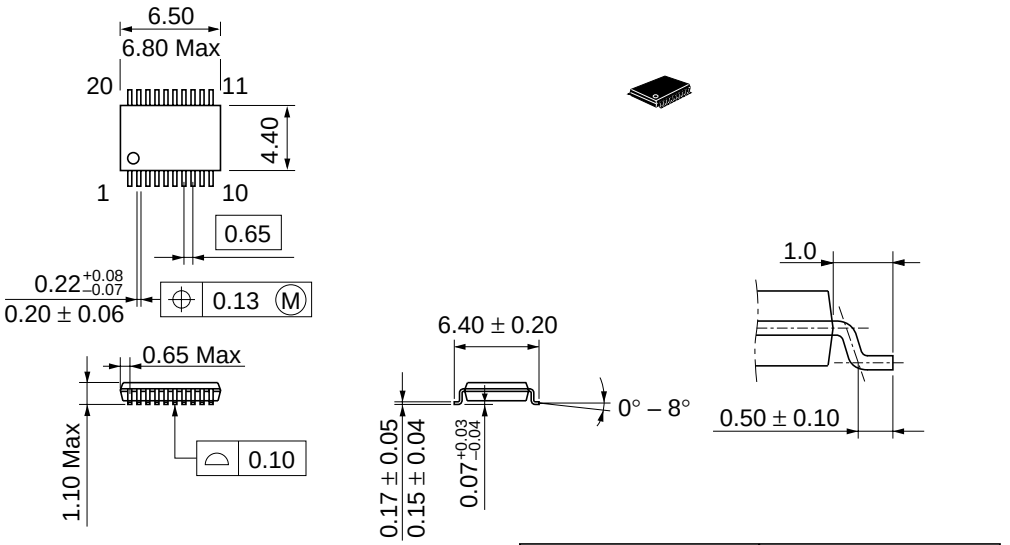
• Example of AC Signal Generator



Package Dimensions

Unit : mm

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX