HD153021F — Preliminary

25-Mbps VFO with Built-in 1-7 Encoder/Decoder

Description

The HD153021F is a 25-Mbps VFO with built-in 1-7 run-length-limit encoder/decoder developed for use in magnetic disk drives. In read mode it decodes 1-7 RLL encoded data from the magnetic disk to an NRZ signal, which it outputs in synchronization with a read clock. In write mode it encodes an NRZ signal to 1-7 RLL data. The HD153021F supports zone bit recording and has circuits for generating the necessary write clock.

HD153021F

(FP-80A)

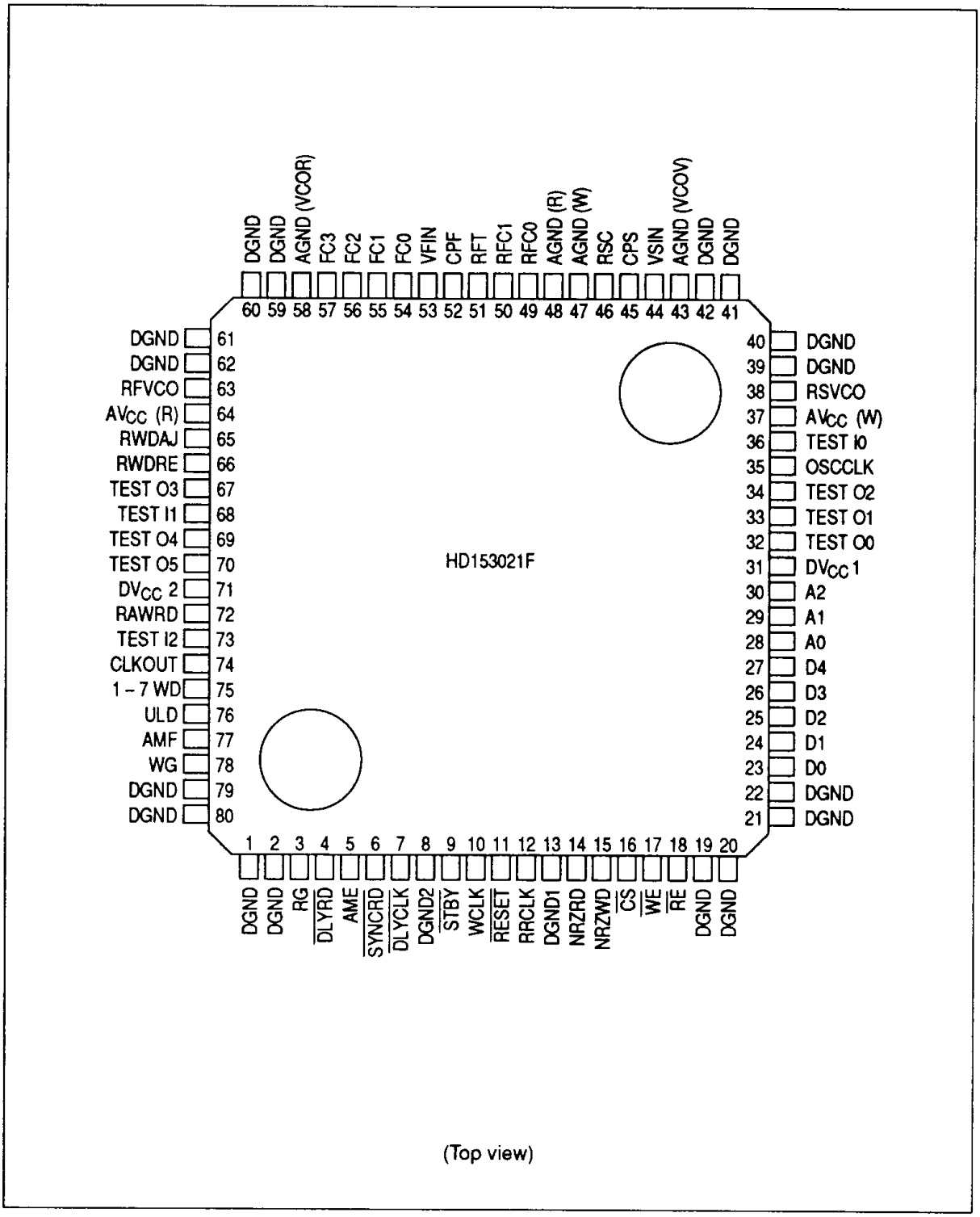
Features

- Maximum data transfer rate: 25 Mbps
- Data transfer clock frequency: 1.5 × data transfer rate
- Encoding and decoding: IBM 1-7 RLL code
- Settings are microcontroller-programmable
- Supports zone bit recording
- On-chip frequency synthesizer generates encode clock (32 frequencies, 3.125% steps)
- Window centering adjustment (rough and fine) and window monitoring functions
- Programmable write precompensation table and delay
- The following are programmable for zone bit recording: VCO center frequency (32 settings), loop filter constant (2 settings), charge pump current (2 settings), and T/I converter output current (8 settings).
- Supports both hard sectoring and soft sectoring (DC erase)
- Detects sync field (3T)
- Hi-BiCMOS process achieves high speed with lower power dissipation
- Standby function
- QFP80 package suitable for compact surface mounting (resin size: 14 mm^2)
- Convenient single 5-V power supply

Ordering Information

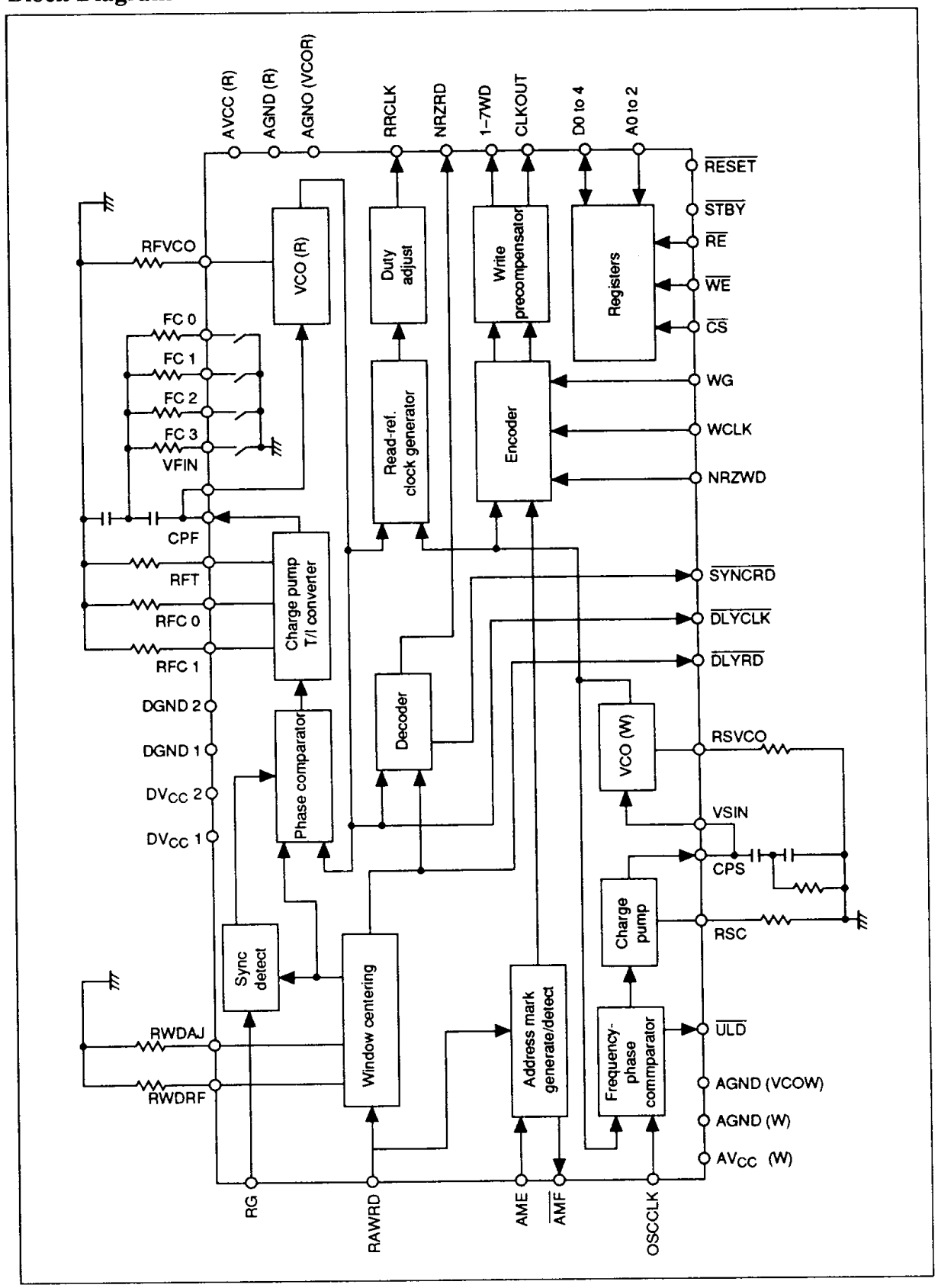
Type No.	Package
HD153021F	FP-80A

Pin Arrangement



(Top view)

Block Diagram



Pin Functions

Pin Name	Pin No.	Type	Function
RG (Read gate)	3	In	High input selects read mode, in which 1-7 encoded data read from disk are converted to an NRZ signal and output. This signal switches the clock for counters and internal circuits, starts NRZ signal output, and begins phase synchronization of the decode clock generator's VFO with the 1-7 coded data. When bit 4 in register MDC is set to 1, the sync field detect circuit is activated and the internal RG signal is delayed until after sync detection.
AME (Address mark enable)	5	In	Used for soft sector formats. Drive this line high to generate or detect address marks. For address mark generation, drive this line high for 1 to 3 bytes when WG is high to write a fixed-length address-mark pattern (8T, 8T, 11T, 11T). For address mark detection, drive this line high when WG is low. An $\overline{\text{AMF}}$ signal will be output when an address mark is detected. When the $\overline{\text{AMF}}$ signal is output, the disk controller should drive AME low.
$\overline{\text{STBY}}$ (Standby)	9	In	Low input selects standby mode, reducing power dissipation. Internal circuits are initialized. Keep this line high during normal operation.
WCLK (Write clock)	10	In	Apply a clock signal synchronized with the NRZ write data signal input to NRZWD. If the connected disk controller provides write clock output, connect the write clock directly to this input line. If the disk controller does not provide write clock output, connect this input line to the RRCLK output line from this IC. The signal input to NRZWD must then be synchronized with the RRCLK output.
$\overline{\text{RESET}}$	11	In	Low input initializes internal circuits. Drive this line low at power-up. Low input also locks the two built-in VCOs to their center frequencies. Keep this line high during normal operation.
NRZWD (NRZ write data)	15	In	NRZ signal to be written to disk. Must be synchronized with the clock signal input to WCLK. Input on this line is inverted on-chip, then converted to 1-7 code.
$\overline{\text{CS}}$ (Chip select)	16	In	Register control input. On-chip registers connected to the microcontroller's bus are selected when this line is driven low.
$\overline{\text{WE}}$ (Write enable)	17	In	Register control input. Data on the microcontroller's bus are written on the rising edge of $\overline{\text{WE}}$ to the on-chip register selected by address input. $\overline{\text{CS}}$ must be low.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{RE}$ (Read enable)	18	In	Register control input. While this line is low, contents of the on-chip register selected by address input are output on the microcontroller's bus, permitting register contents to be verified. $\overline{CS}$ must be low.
D0 to D4 (Data 0 to data 4)	23 – 27	In/Out	Register data lines, normally connected to the microcontroller's data bus. Input lines when $\overline{RE}$ is high. Output lines when $\overline{RE}$ is low.
A0 to A2 (Address 0 to address 2)	28 – 30	In	Register address input lines, normally connected to the microcontroller's address bus.
OSCCLK (Oscillator clock)	35	In	Reference clock input. The encode clock generator's on-chip frequency synthesizer generates encode clock frequencies from the clock input on this line. Data writing is synchronized with the encode clock. When not reading data, the decode clock generator's VFO is also synchronized with the encode clock. Apply a clock signal with frequency frequency 1.5/8 times the minimum data transfer rate. If not using the encode clock generator's on-chip frequency synthesizer, apply an encode clock at 1.5 times the transfer rate directly to OSCCLK. Bit 4 of register WPC1 must then be set to 1.
RAWRD (Raw read data)	72	In	Input line for 1-7 encoded data read from disk. The leading edge of the input signal is timed with magnetic reversal. Leading edge polarity can be selected by bit 3 in register WPC0. The decode clock generator's VFO is phase-synchronized with this leading edge.
WG (Write gate)	78	In	High input selects write mode, in which the NRZ write data signal is converted to 1-7 code and output. Drive this line high to generate a soft sector address mark, and low to detect address marks.
$\overline{DLYRD}$ (Delay read data)	4	Out	Window adjustment monitor output. Low output on this line corresponds to 1s in 1-7 code read from disk. In window adjustment, center the falling edge of the output on this line halfway between the falling and rising edges of the output at $\overline{DLYCLK}$. Bit 0 of register MDC must be set to 1. If MDC bit 0 is cleared to 0, $\overline{DLYRD}$ is always high.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{\text{SYNCRD}}$ (Sync. read data)	6	Out	Window adjustment monitor output. 1-7 codes read from the disk are latched on the decode clock and output on this line. $\overline{\text{SYNCRD}}$ output is equivalent to capturing the 1-7 codes output from $\overline{\text{DLYRD}}$ on the $\overline{\text{DLYCLK}}$ output. Use this line to monitor window margin tests. Bit 0 of the MDC register must be set to 1. If MDC bit 0 is cleared to 0, $\overline{\text{SYNCRD}}$ is always high.
$\overline{\text{DLYCLK}}$ (Delay clock)	7	Out	Window adjustment monitor output. Provides decode clock output synchronized with the 1-7 codes read from disk. The 1-7 codes can be latched on this clock. In window adjustment, center the falling edge of the $\overline{\text{DLYRD}}$ output halfway between the falling and rising edges of the $\overline{\text{DLYCLK}}$ output. Bit 0 of register MDC must be set to 1. If MDC bit 0 is cleared to 0, $\overline{\text{DLYCLK}}$ is always high.
RRCLK (Read reference clock)	12	Out	In read mode, a clock signal synchronized with the converted NRZ read data is output on this line. At other times, a reference clock is output for input by the disk controller. In read mode, the disk controller should latch the NRZ read data on the RRCLK output. If the connected disk controller does not provide write clock output, connect RRCLK to WCLK on this IC. The signal input at NRZWD must then be synchronized with the RRCLK output. The RRCLK clock output is free of glitches at clock switchover. The duty cycle of the clock output on this line can be selected by bits 0 to 3 in register DTC.
NRZRD (NRZ read data)	14	Out	1-7 codes read from the disk are converted to an NRZ signal and output on this line. The NRZRD signal is synchronized with the RRCLK signal.
CLKOUT (Clock out)	74	Out	Clock output used for external write phase compensation (write precompensation). The clock signal output on this line is synchronized with the 1-7WD output. Bit 3 of register WPC3 must be set to 1. If WPC3 bit 3 is cleared to 0, CLKOUT is always high.
1-7WD (1-7 write data)	75	Out	Output signal to be written to disk, consisting of 1-7 codes obtained by encoding the NRZ signal. The polarity of the output on this line can be switched by bit 4 of register WPC1. For external write precompensation, use the CLKOUT clock output, which is synchronized with the 1-7WD output.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$\overline{ULD}$ (Unlock detect)	76	Out	Error output from the encode clock generator's frequency synthesizer. $\overline{ULD}$ goes low to indicate that the PLL in the encode clock generator's frequency synthesizer has lost lock. The disk controller should immediately halt write operations. Data must be written again from the beginning.
$\overline{AMF}$ (Address mark found)	77	Out	Soft sector address mark detect output. If AME input is high and WG input is low, $\overline{AMF}$ goes low whenever an address mark pattern is detected. The disk controller should then drive AME low, to clear the $\overline{AMF}$ output to high.
RSVCO	38	External component connection	Connect a resistor to set the center frequency of the VCO in the encode clock generator's frequency synthesizer.
VSIN	44	External component connection	Voltage input controlling the VCO in the encode clock generator's frequency synthesizer. Reset causes a VCO bias voltage generated on-chip to be applied to VSIN through an analog switch, making the VCO oscillate at its center frequency. Normally this line should be connected to CPS.
CPS	45	External component connection	Current output to an external loop filter. Normally this line should be connected to VSIN as well as to the loop filter.
RSC	46	External component connection	Connect a resistor to set the charge pump output current for the encode clock generator's frequency synthesizer.
RFC0	49	External component connection	Connect a resistor to set the charge pump output current for the decode clock generator's VFO. This line is selected when bit 3 in the GAC register is cleared to 0, and is deselected if bit 3 is set to 1.
RFC1	50	External component connection	Connect a resistor to set the output current of the charge pump used in the decode clock generator's VFO. This line is selected when bit 3 in the GAC register is set to 1, and is deselected if bit 3 is cleared to 0.
RFT	51	External component connection	Connect a resistor to set the T/I converter's sampling feedback gain to 1 (nominal). The T/I converter's output current is determined by this resistor, bits 0 to 4 of register VFC, and bits 0 to 2 of register GAC.
CPF	52	External component connection	Current output to external loop filter. Normally this line should be connected to VFIN as well as to the loop filter.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
VFIN	53	External component connection	Voltage input controlling the VCO in the decode clock generator's VFO. Reset causes a VCO bias voltage generated on-chip to be applied to VFIN through an analog switch, making the VCO oscillate at its center frequency. Normally this line should be connected to CPF.
FC0	54	External component connection	Connect a loop filter resistor to set the attenuation ζ of the PLL. This line is grounded through an MOS switch when bit 3 of register GAC is set to 1, and is internally disconnected when bit 3 is cleared to 0.
FC1	55	External component connection	Connect a loop filter resistor to set the attenuation ζ of the PLL. This line is grounded through an MOS switch in high gain mode when bit 3 of register GAC is set to 1, and is internally disconnected at other times.
FC2	56	External component connection	Connect a loop filter resistor to set the attenuation ζ of the PLL. This line is grounded through an MOS switch when bit 3 of register GAC is cleared to 0, and is internally disconnected when bit 3 is set to 1.
FC3	57	External component connection	Connect a loop filter resistor to set the attenuation ζ of the PLL. This line is grounded through an MOS switch in high gain mode when bit 3 of register GAC is cleared to 0, and is internally disconnected at other times.
RFVCO	63	External component connection	Connect a resistor to set the center frequency of the VCO in the decode clock generator's VFO.
RWDAJ	65	External component connection	Connect a resistor for fine adjustment of window centering. Fine adjustment is determined by the relative values of this resistor and the reference resistor connected to RWDRF
RWDRF	66	External component connection	Connect a reference resistor for fine adjustment of window centering.
DV_{CC1}	31	Power	Digital V_{CC} power supply.
DV_{CC2}	71	Power	Digital V_{CC} power supply.
DGND1	13	Power	Digital ground.
DGND2	8	Power	Digital ground.
$AV_{CC(R)}$	64	Power	Analog V_{CC} power supply. Powers analog circuits in the decode clock generator.

Pin Functions (cont)

Pin Name	Pin No.	Type	Function
$AV_{CC(W)}$	37	Power	Analog V_{CC} power supply. Powers analog circuits in the encode clock generator.
AGND(R)	48	Power	Analog ground. Powers analog circuits in the decode clock generator.
AGND(W)	47	Power	Analog ground. Powers analog circuits in the encode clock generator.
AGND(VCOR)	58	Power	Grounds the decode clock generator's VCO.
AGND(VCOW)	43	Power	Grounds the encode clock generator's VCO.
DGND	1, 2 19 – 22 39 – 42 59 – 62 79, 80	Power	Ground lines for cooling.
TESTI0	36	In	Test input line. Drive this line high at all times.
TESTI1	68	In	Test input line. Drive this line low in test mode to monitor clock output from the encode clock generator's frequency synthesizer and decode clock generator's VFO. If $\overline{\text{RESET}}$ is also driven low, the output clocks are locked at center frequency. Normally, keep this line high.
TESTI2	73	In	Test input line. Drive this line high at all times.
TESTO0	32	Out	Test output line. In test mode, this line outputs the clock signal created by the encode clock generator's frequency synthesizer. Normally, leave this line unconnected.
TESTO1	33	Out	Test output line. Leave unconnected.
TESTO2	34	Out	Test output line. Leave unconnected.
TESTO3	67	Out	Test output line. In test mode, this line outputs the clock signal created by the decode clock generator's VFO. Normally, leave this line unconnected.
TESTO4	69	Out	Test output line. Leave unconnected.
TESTO5	70	Out	Test output line. Leave unconnected.

Registers

The HD153021F has eight 5-bit registers that control the center frequency of the decode clock generator's VFO and the frequency of the encode clock generator's frequency synthesizer, adjust the decode window, adjust the write precompensation, control the duty cycles of the read clock and reference clock signals output to the disk controller, and select various modes.

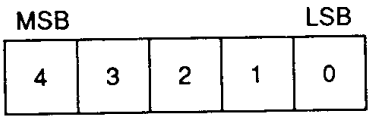
Registers

Address	Name	Abbreviation
0	VCO center frequency control register	VFC register
1	Gain control register	GAC register
2	Window adjust register	WAJ register
3	Duty control register	DTC register
4	Write precompensation control register 0	WPC0 register
5	Write precompensation control register 1	WPC1 register
6	Write precompensation control register 2	WPC2 register
7	Mode control register	MDC register

Note: The registers are initialized to 0 by a low input on the $\overline{\text{RESET}}$ line or $\overline{\text{STBY}}$ line.

Register Descriptions

Register 0: VCO Center Frequency Control Register (VFC)



This register is used in zone bit recording to set the center frequency of the decode clock generator's VCO, the T/I converter's reference current, and the oscillation frequency of the encode clock generator's frequency synthesizer.

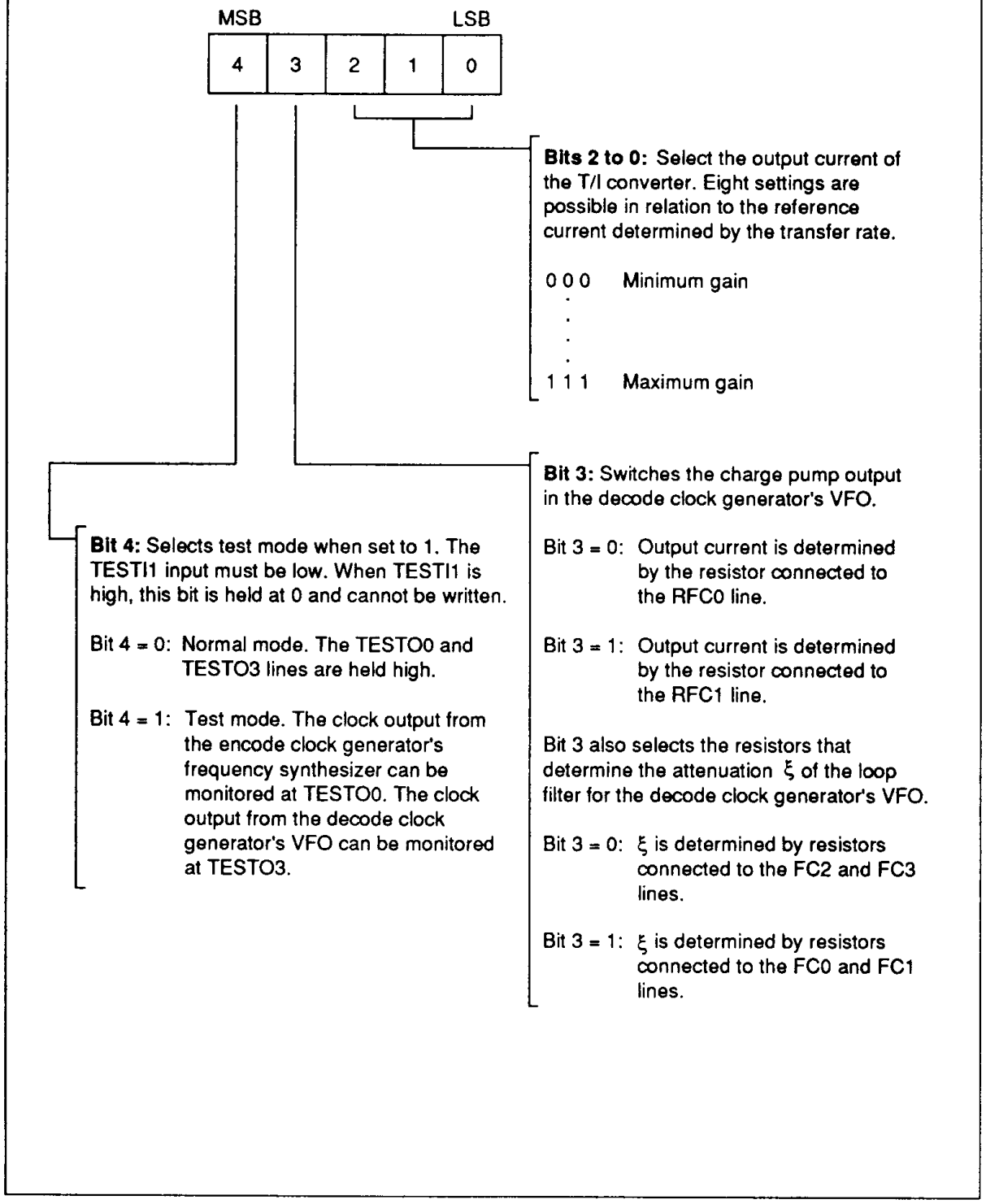
Resistors connected to the RFVCO, RFT, and RSVCO lines set these values for the minimum data transfer rate. The VFC register raises these values in steps of 3.125%, permitting 32 settings up to a maximum transfer rate double the minimum rate.

0 0 0 0 0 Minimum transfer rate (reference rate)

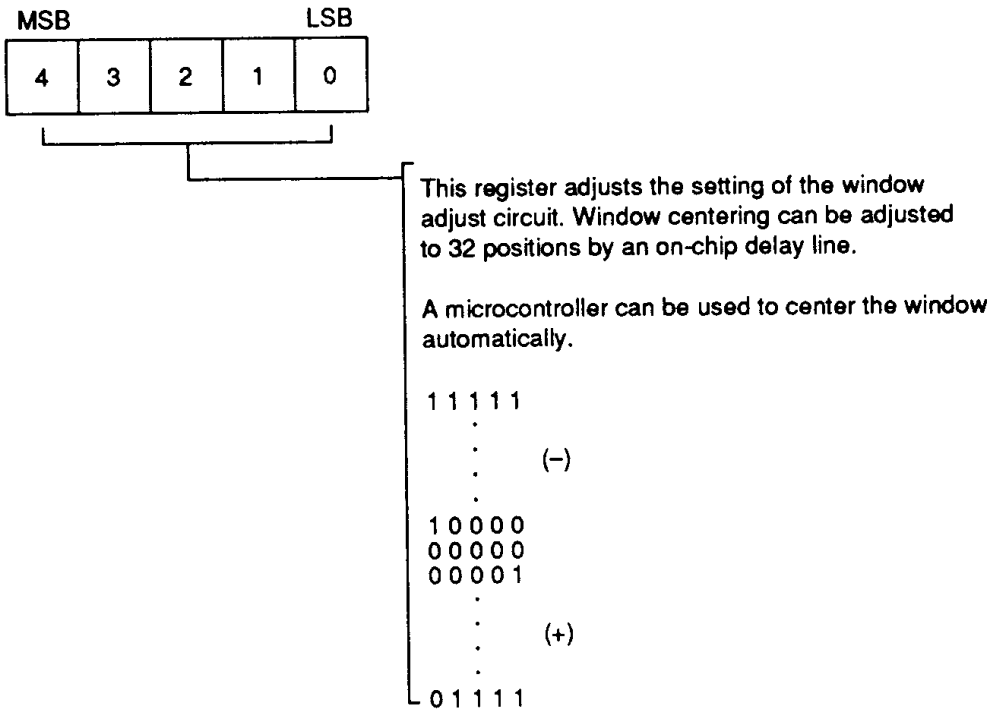
.
.
.
.

1 1 1 1 1 Maximum transfer rate (double speed)

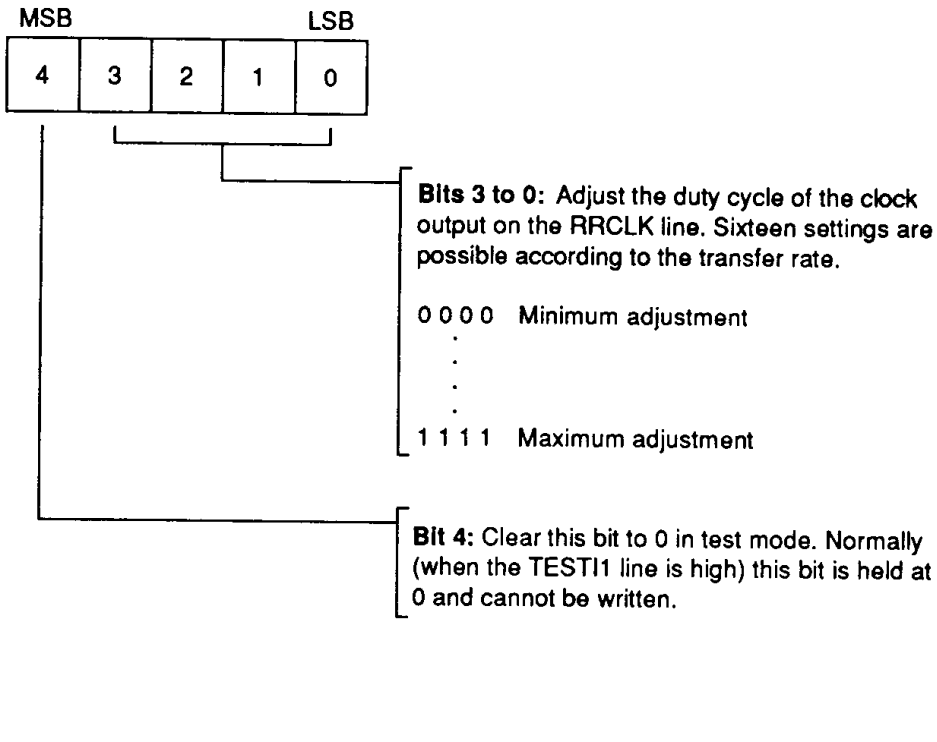
Register 1: Gain Control Register (GAC)



Register 2: Window Adjust Register (WAJ)



Register 3: Duty Control Register (DTC)



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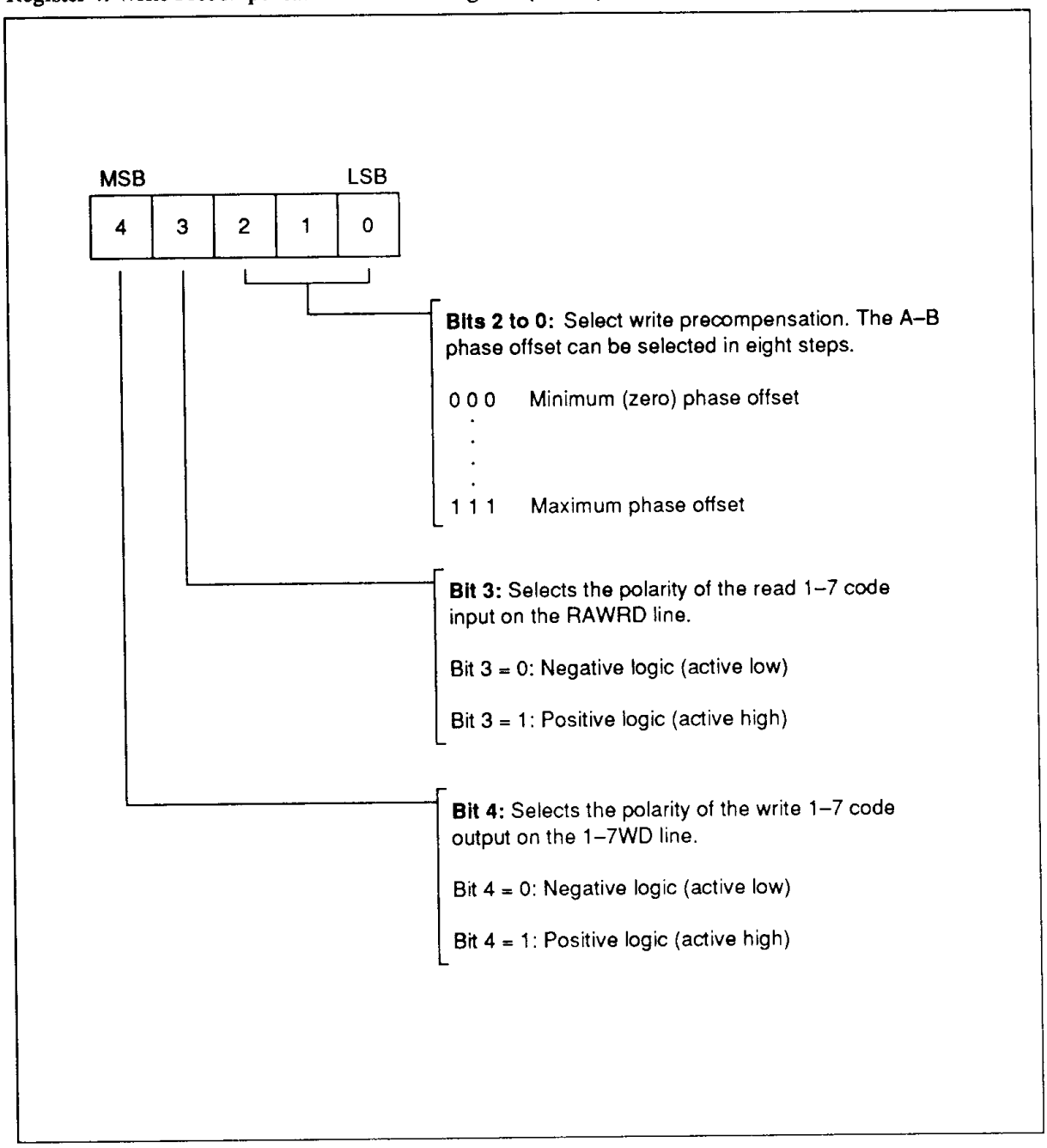
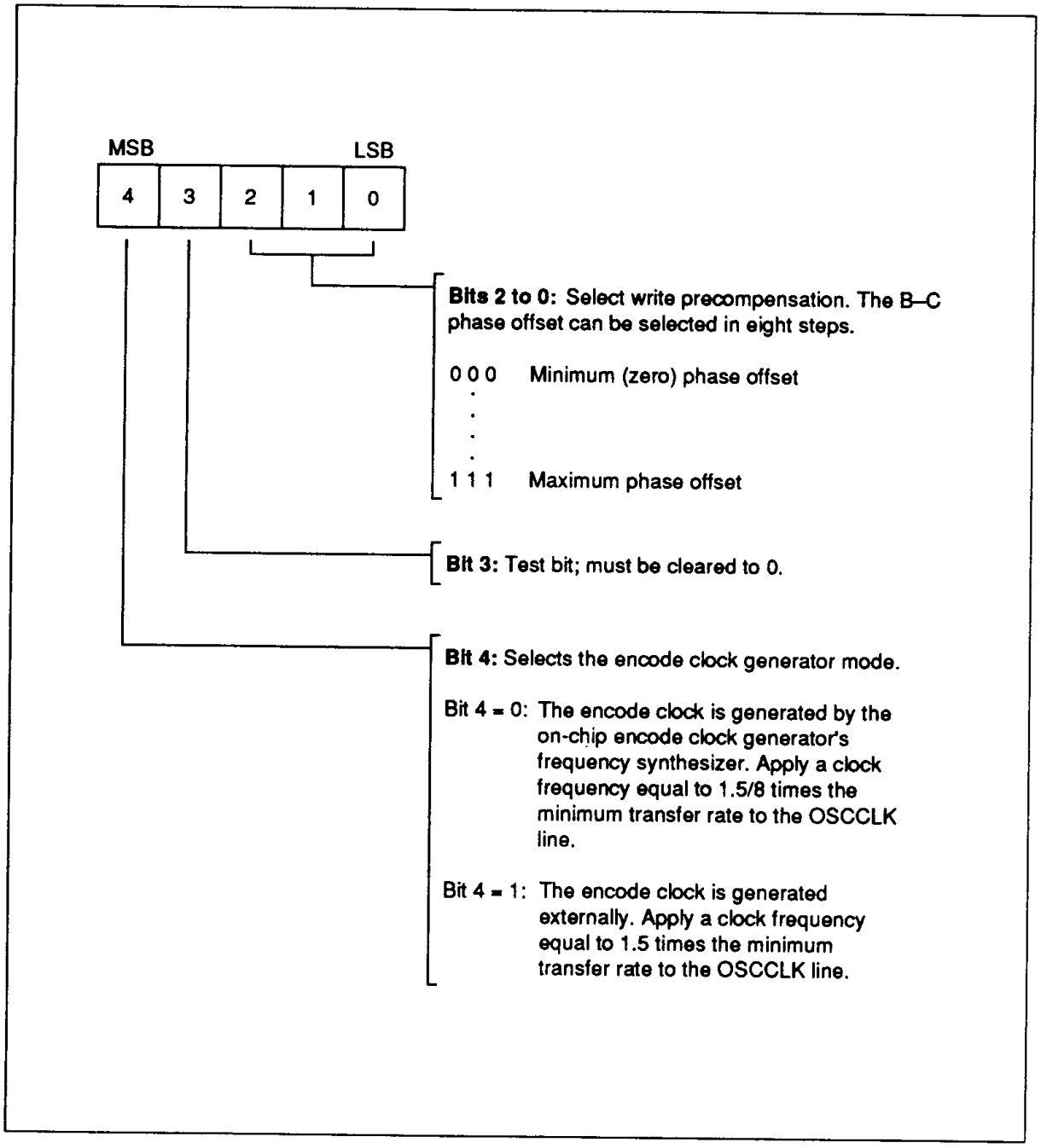
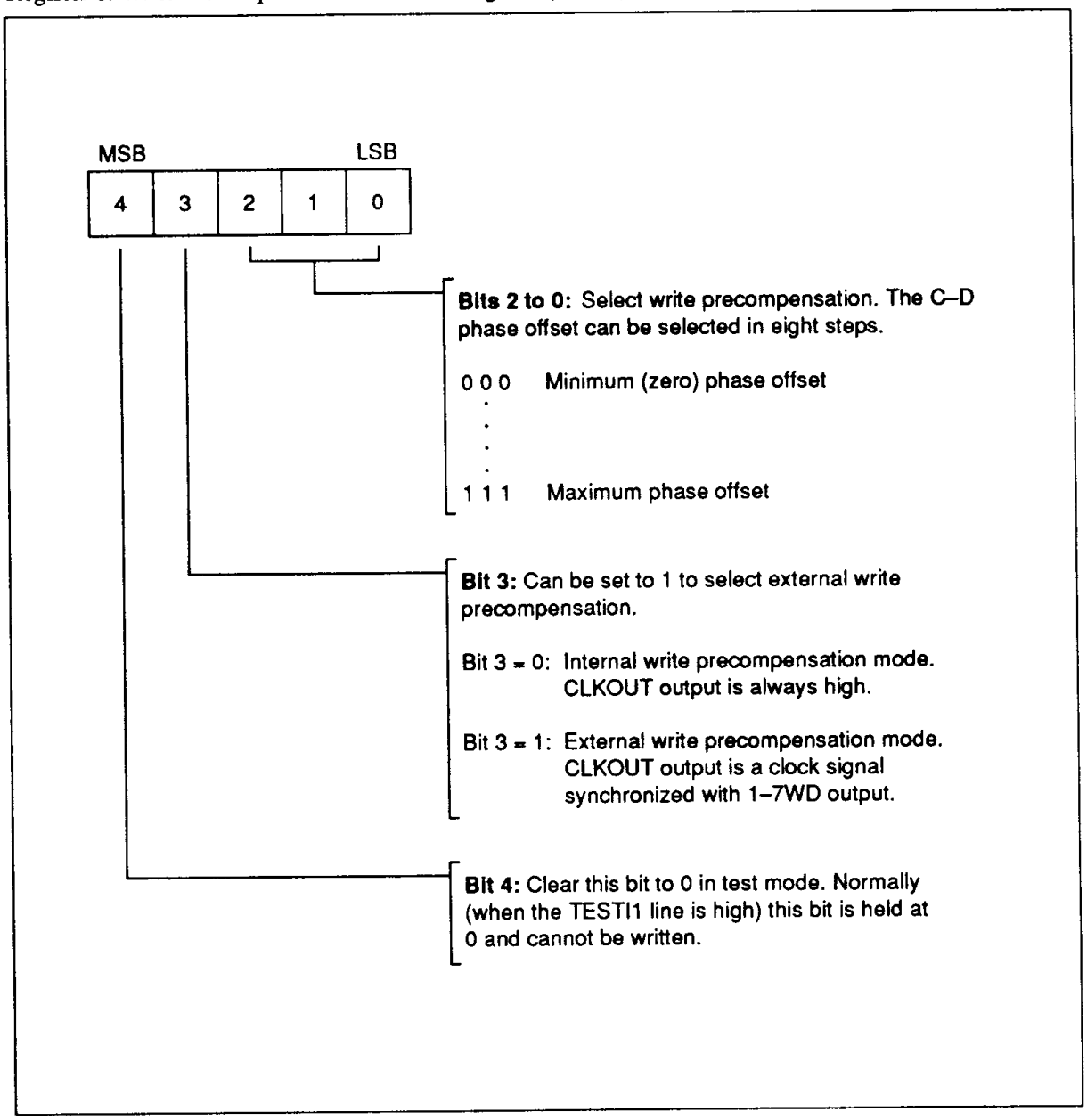
Register 4: Write Precompensation Control 0 Register (WPC0)



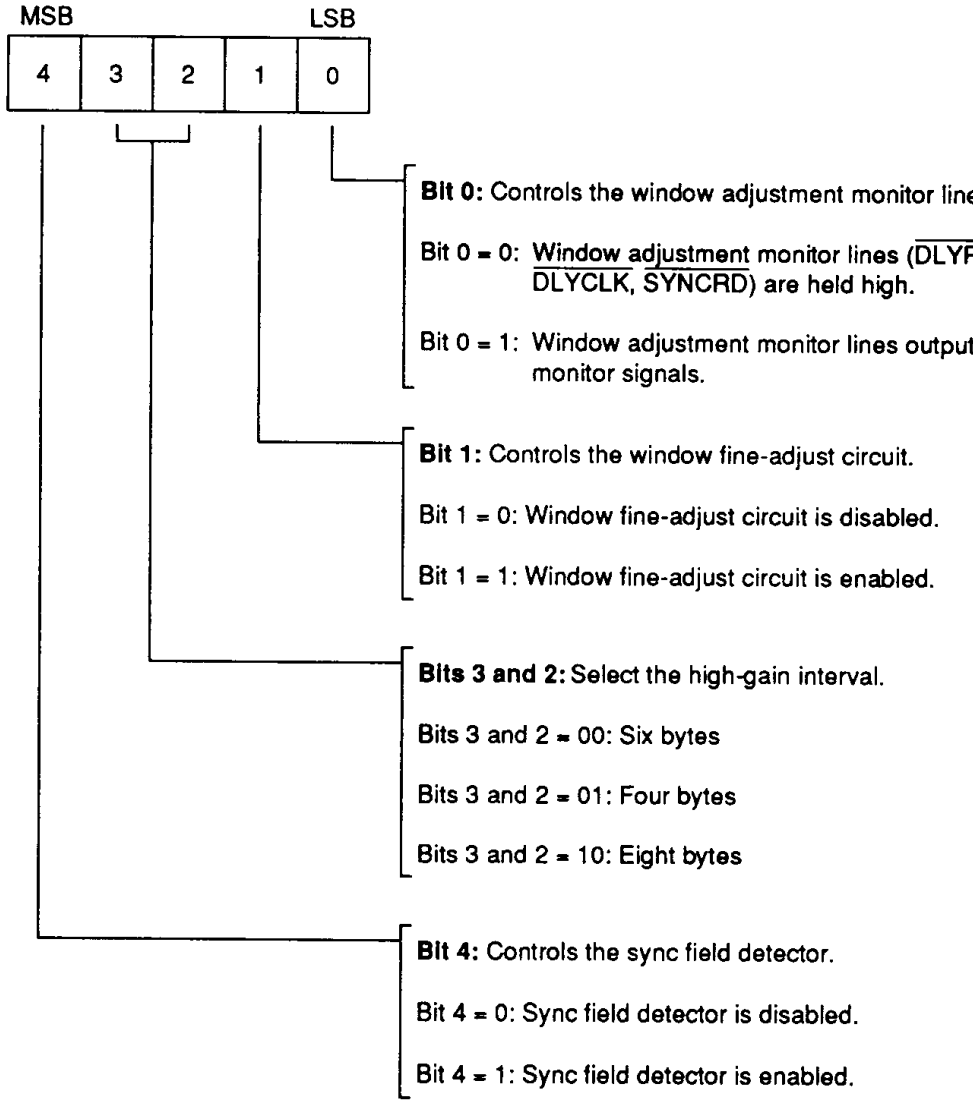
Register 5: Write Precompensation Control 1 Register (WPC1)



Register 6: Write Precompensation Control 2 Register (WPC2)



Register 7: Mode Control Register (MDC)



1-7 Encoder/Decoder

The encoder converts an NRZ signal to 1-7 coded data. The decoder converts 1-7 coded data to an NRZ signal. See the conversion table.
The NRZ signal is inverted before conversion to 1-7 code. The disk controller must write 0000... in the sync area. The 3T pattern written in the sync area (100100...) will be decoded to 0000....
The polarity of the 1-7 code can be selected by bit 3 in register WPC0.

Conversion Table

Last bit of previous code	Data bits		Code bits
	Current	Next	
0	10	0x	101
0	10	1x	010
0	11	00	010
0	11	$\overline{00}$	100
0	00	0x	001
0	00	1x	000

Last bit of previous code	Data bits		Code bits
	Current	Next	
0	01	0x	001
0	01	1x	000
1	00	0x	001
1	00	1x	010
1	01	00	010
1	01	$\overline{00}$	000

$\overline{00}$: Not 00
x: Don't care

1-7 Code Polarity Selection

1-7 Code Input Polarity Selection

WPC0 Register

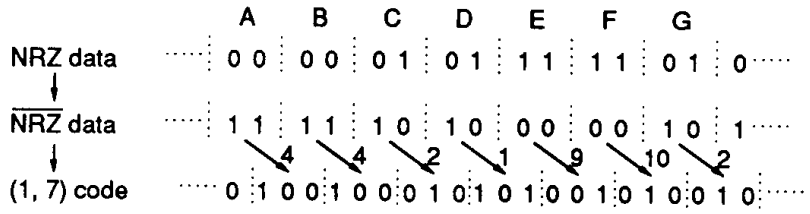
4	3	2	1	0	1-7 code input on RAWRD line
—	0	—	—	—	Negative logic (active low)
—	1	—	—	—	Positive logic (active high)
MSB				LSB	

1-7 Code Output Polarity Selection

WPC0 Register

4	3	2	1	0	1-7 code output on 1-7WD line
0	—	—	—	—	Negative logic (active low)
1	—	—	—	—	Positive logic (active high)
MSB				LSB	

An example of the conversion of an NRZ signal to (1, 7) coded data is given below.



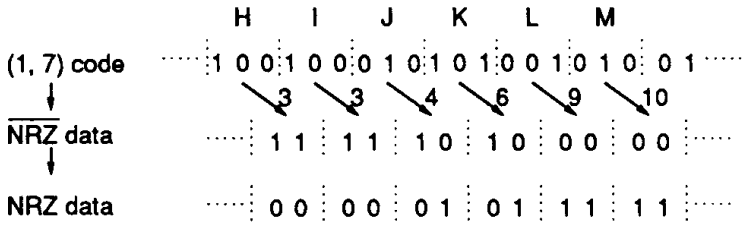
The NRZ data is inverted before it is converted into (1, 7) code. For example, when the above NRZ B data ('00') is converted, it is first inverted to give the NRZ data '11', then the last bit ('0') of the result of converting A ('100') and the next NRZ data status C '01' (C = '10') dictate that 4 is selected from the conversion table, so that the B data '00' is converted into the (1, 7) code '100'.

Conversion Table

	1, 7 code bits			
No.	**Previous**	**Current**	**Next**	**NRZ data bits**
1	X 1 0	0 0 0	X X X	0 0
2	X 0 0	0 0 0	X X X	0 1
3	X X X	1 0 0	X X X	1 1
4	X X 0	0 1 0	$\overline{0\,0}$ X	1 0
5	X X 0	0 1 0	0 0 X	1 1
6	X X X	1 01	X X X	1 0
7	X 0 0	0 0 1	X X X	0 1
8	X 1 0	0 0 1	X X X	0 0
9	X X 1	0 0 1	X X X	0 0
10	X X 1	0 1 0	$\overline{0\,0}$ X	0 0
11	X X 1	0 1 0	0 0 X	0 1
12	X X 1	0 0 0	X X X	0 1

x: Don't care
$\overline{0\,0}$: Not 0 0

An example of the conversion of (1, 7) coded data to an NRZ signal is given below.

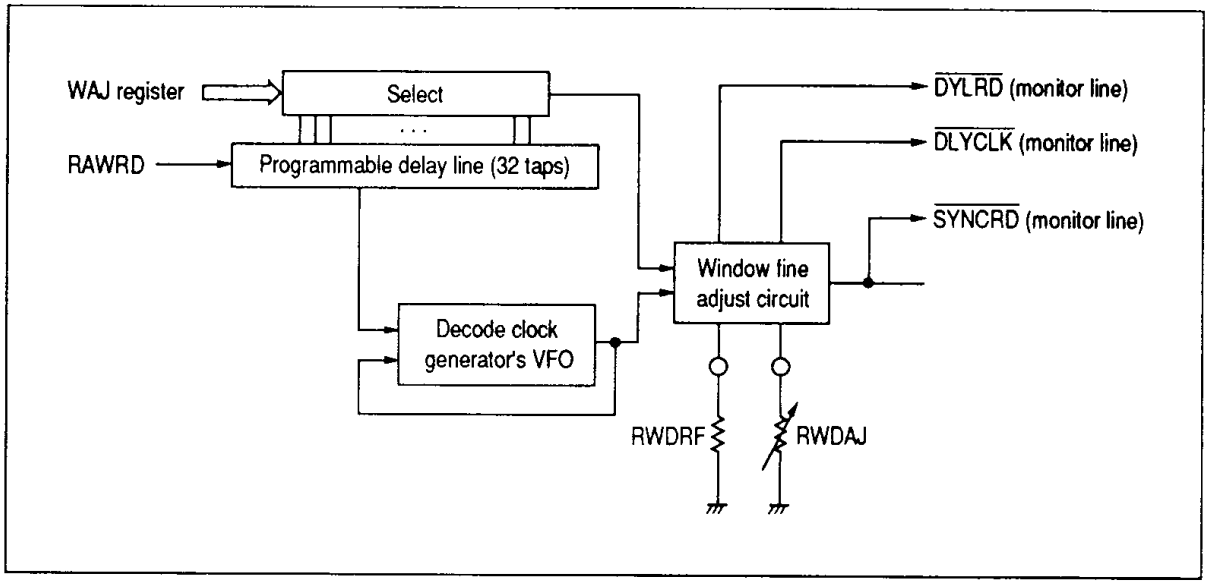


For example, when the above (1, 7) coded I = '100' data is converted into NRZ data, the previous status H = '100' and the next status J = '010' dictate that 3 is selected from the conversion table, so the data is converted into the NRZ data '11'. This is inverted and output as the NRZ data '00'

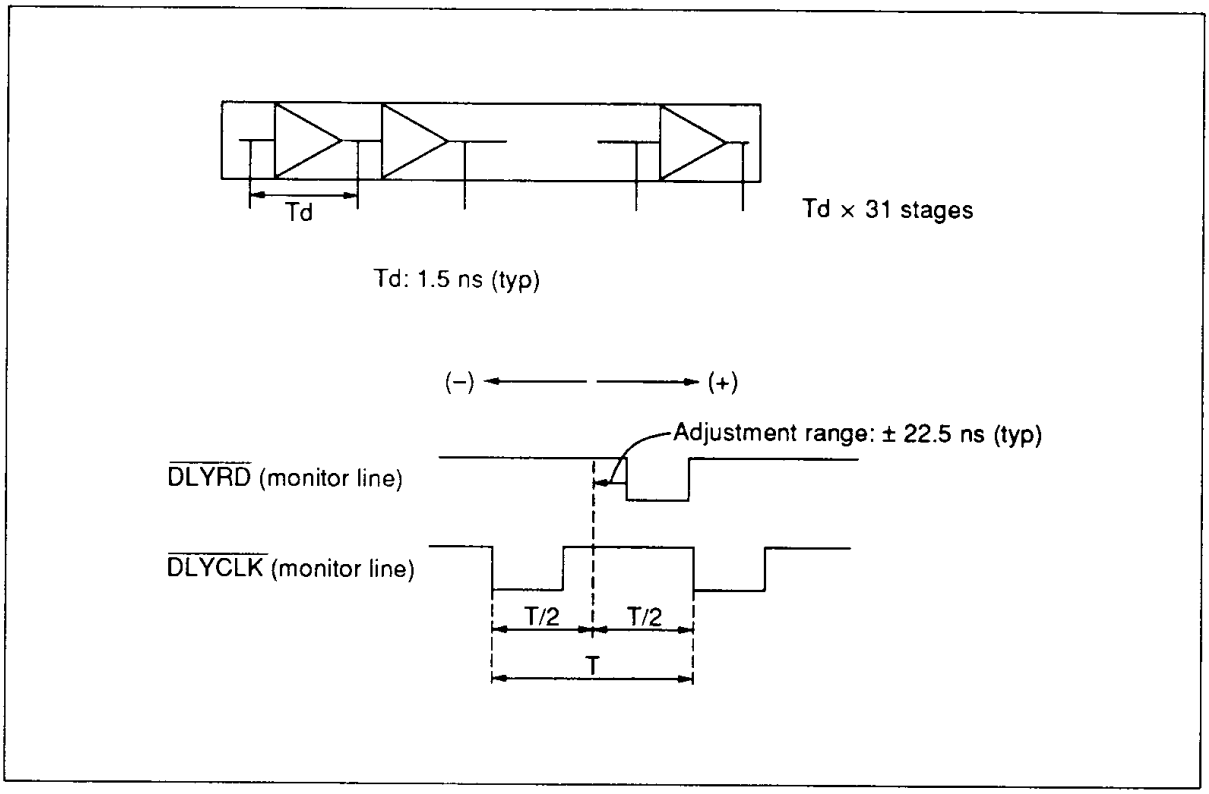
Window Adjust Circuit

The decode window is centered by means of a programmable, on-chip delay line. The centering is adjusted by setting one of 32 values in the WAJ register. This can be done under microcontroller control for automatic centering. If more precise adjustment is required, the window fine-adjust circuit enables you to perform continuous adjustment while monitoring the signal waveform.

Circuit Configuration



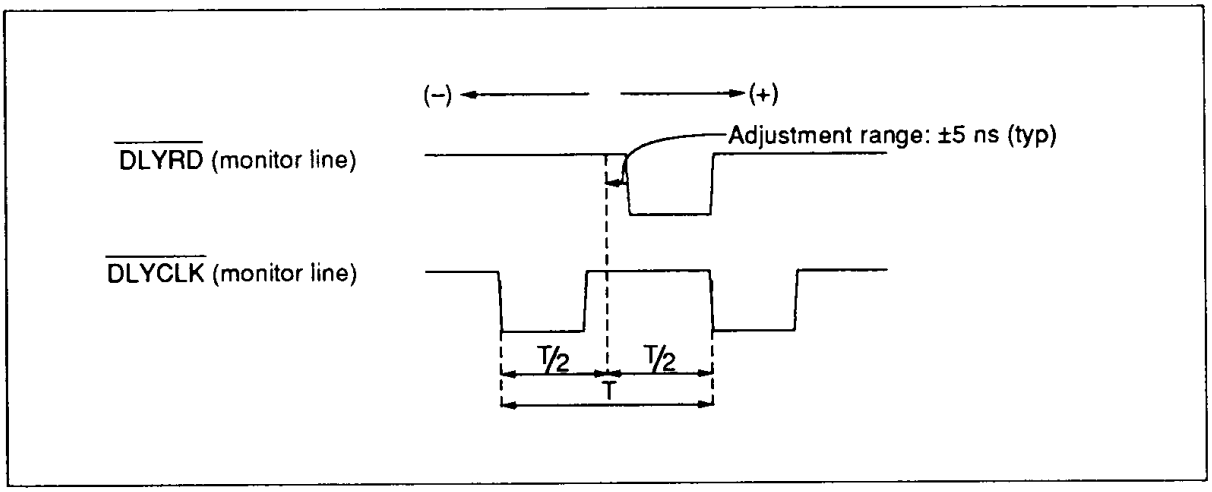
Programmable Delay Line



WAJ Register					Delay line tap
4	3	2	1	0	No.
1	1	1	1	1	−16
1	0	0	0	1	−2
1	0	0	0	0	−1
0	0	0	0	0	0

WAJ Register					Delay line tap
4	3	2	1	0	No.
0	0	0	0	1	+1
0	0	0	1	0	+2
0	1	1	1	1	+15

Window Fine-Adjust Circuit



Line	Resistance
RWDRF	10 – 20 kΩ (reference)
RWDAJ	10 – 20 kΩ (adjustment)

Notes: 1. The adjustment is determined by the relative resistances of the resistor connected to the RWDRF line and the resistor connected to the RWDAJ line. Any combination of resistances can be used.
2. When the adjustment exceeds the tap interval (1.6 ns) on the delay line, stability can be improved by changing the delay line tap selection and reducing the adjustment.

Window Adjustment Mode

MDC Register

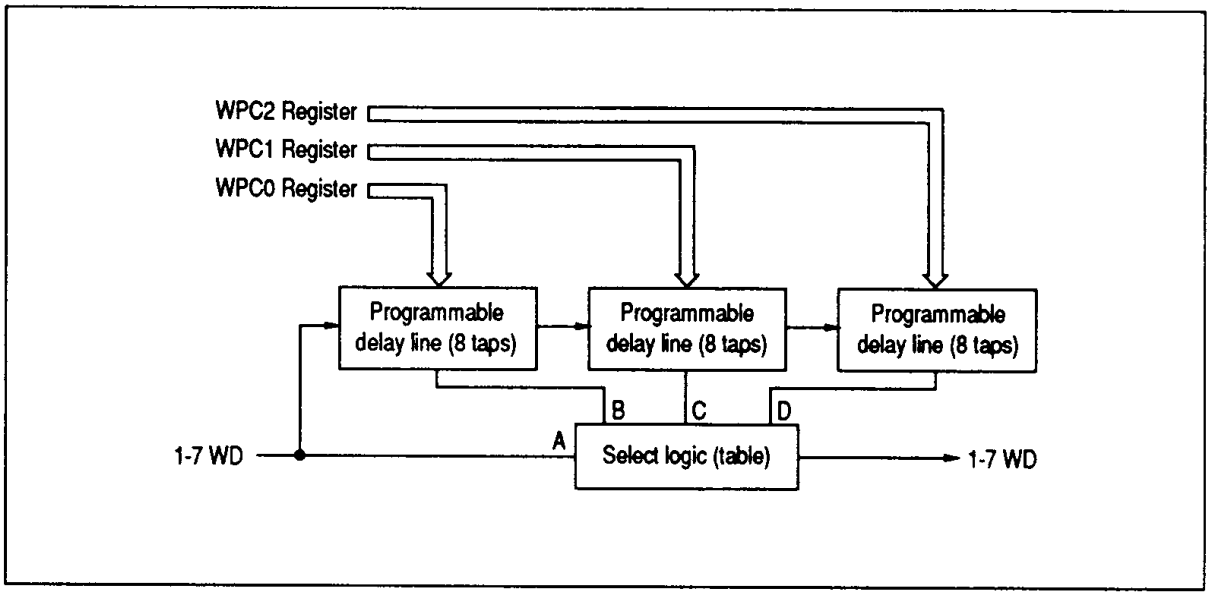
4	3	2	1	0	Window adjustment mode
—	—	—	0	0	Delay line only, monitor lines off
—	—	—	0	1	Delay line only, monitor lines on
—	—	—	1	0	Delay line and fine-adjustment circuit, monitor lines off
—	—	—	1	1	Delay line and fine-adjustment circuit, monitor lines on
MSB				LSB	

Write Precompensation Circuit

The write precompensation circuit contains data divided into four blocks according to combinations of the number of 0 bits between adjacent 1 bits. Settings in registers WPC0, WPC1, and WPC2 can establish phase offsets of up to 10 ns (typ) between the blocks, in eight steps each.

Write precompensation can also be performed externally, using a clock signal output on the CLKOUT line in synchronization with the output on the 1-7WD line.

Circuit Configuration



Table

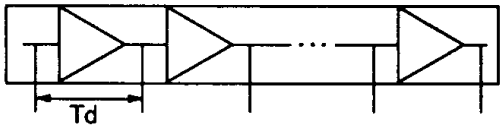
n \ m	1	2	3	4	5	6	7
1	C	A					
2	D	B					
3							
4							
5							
6							
7							

$$\overbrace{10\cdots0}^{n}\ 1\ \overbrace{0\cdots01}^{m}$$

Last 3 This 4 Next 5

n: Number of 0s between this 1 bit and last 1 bit
m: Number of 0s between this 1 bit and next 1 bit

Programmable Delay Line



Td x 7 stages

Td: 1.5 ns (typ)

WPC0 register

4	3	2	1	0	A-B phase offset (unit: Td)
—	—	0	0	0	0
—	—	1	1	1	7

MSB LSB

WPC1 register

4	3	2	1	0	B-C phase offset (unit: Td)
—	—	0	0	0	0
			|		|
—	—	1	1	1	7
MSB				LSB	

WPC2 register

4	3	2	1	0	C-D phase offset (unit: Td)
—	—	0	0	0	0
			|		|
—	—	1	1	1	7
MSB				LSB	

External Write Precompensation Mode

The external write precompensation mode is selected by setting bit 3 of the WPC2 register to 1. A clock signal synchronized with the 1-7WD output is then output on the CLKOUT line.

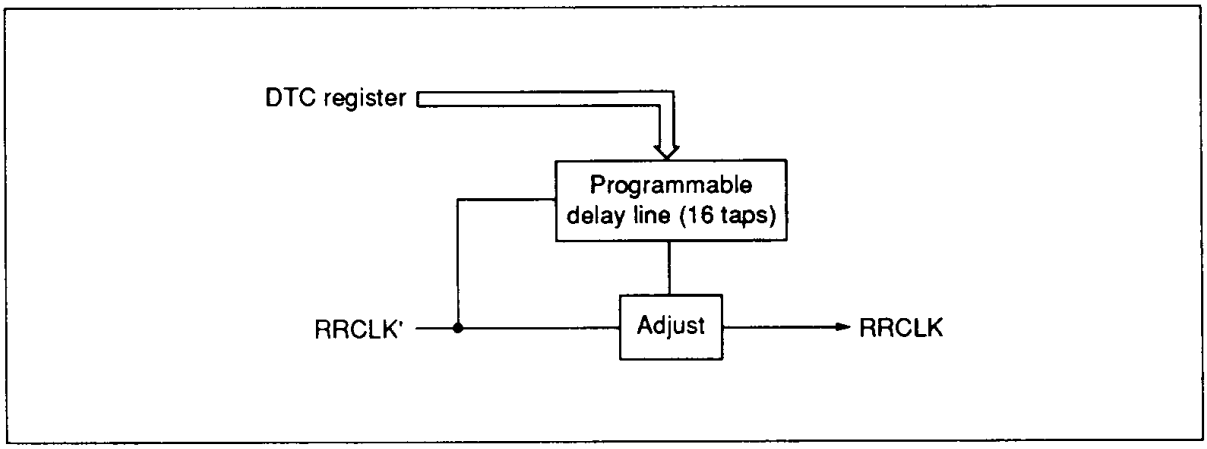
WPC2 register

4	3	2	1	0	Write precompensation mode
—	0	—	—	—	Internal write precompensation mode (CLKOUT off)
—	1	—	—	—	External write precompensation mode (CLKOUT on)
MSB				LSB	

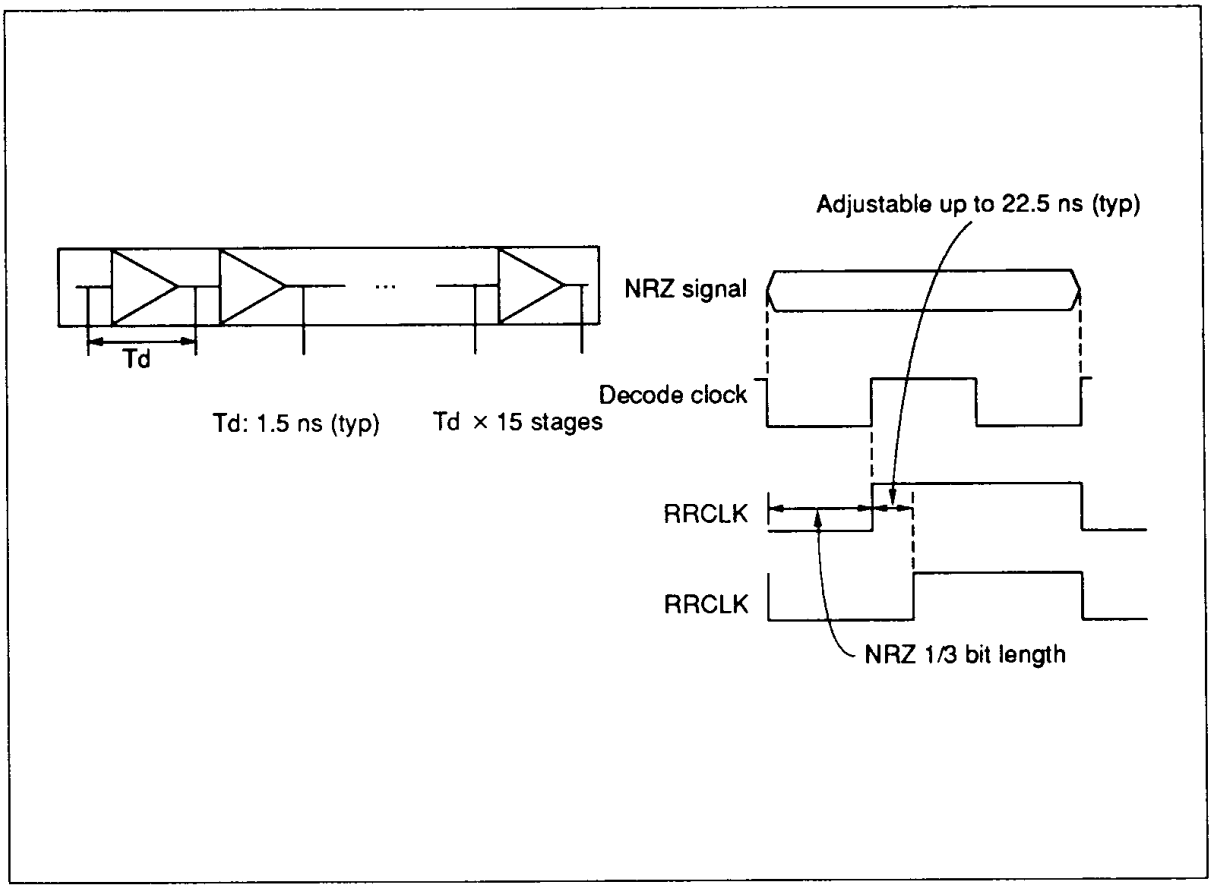
Duty Adjustment Circuit

The read clock and reference clock output to the disk controller are multiplexed and output on the RRCLK line. The duty cycle of the clock output on the RRCLK line can be adjusted by setting the DTC register.

Circuit Configuration



Programmable Delay Line



DTC register

4	3	2	1	0	Adjustment (unit: Td)
—	0	0	0	0	0
—	1	1	1	1	15
MSB				LSB	

Adjustment Examples

Table 11 shows adjustment values (n0) that minimize |Derror| (defined below) for several transfer rates in the vicinity of a 50% duty cycle.

$$Derror = \frac{T}{6} - 1.5 \times n0$$

T: Length of 1 NRZ bit

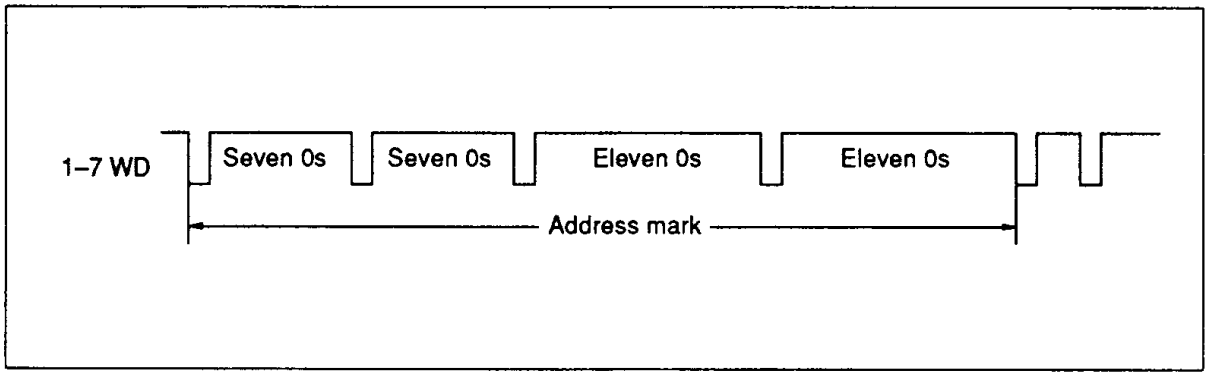
Transfer rate (Mbps)	NRZ Bit length T (ns)	Adjustment value n0	Adjustment size (typ) (ns)	DTC register 3	2	1	0	Duty cycle (%)
10	100.0	11	16.5	1	0	1	1	50.2
15	66.7	7	10.5	0	1	1	1	50.9
20	50.0	6	9.0	0	1	1	0	48.7
30	33.3	3	4.5	0	0	1	1	51.7

Address Mark Generator and Detector

For soft sectoring, on-chip circuits can generate and detect address marks. Address marks are written at the beginning of sectors.

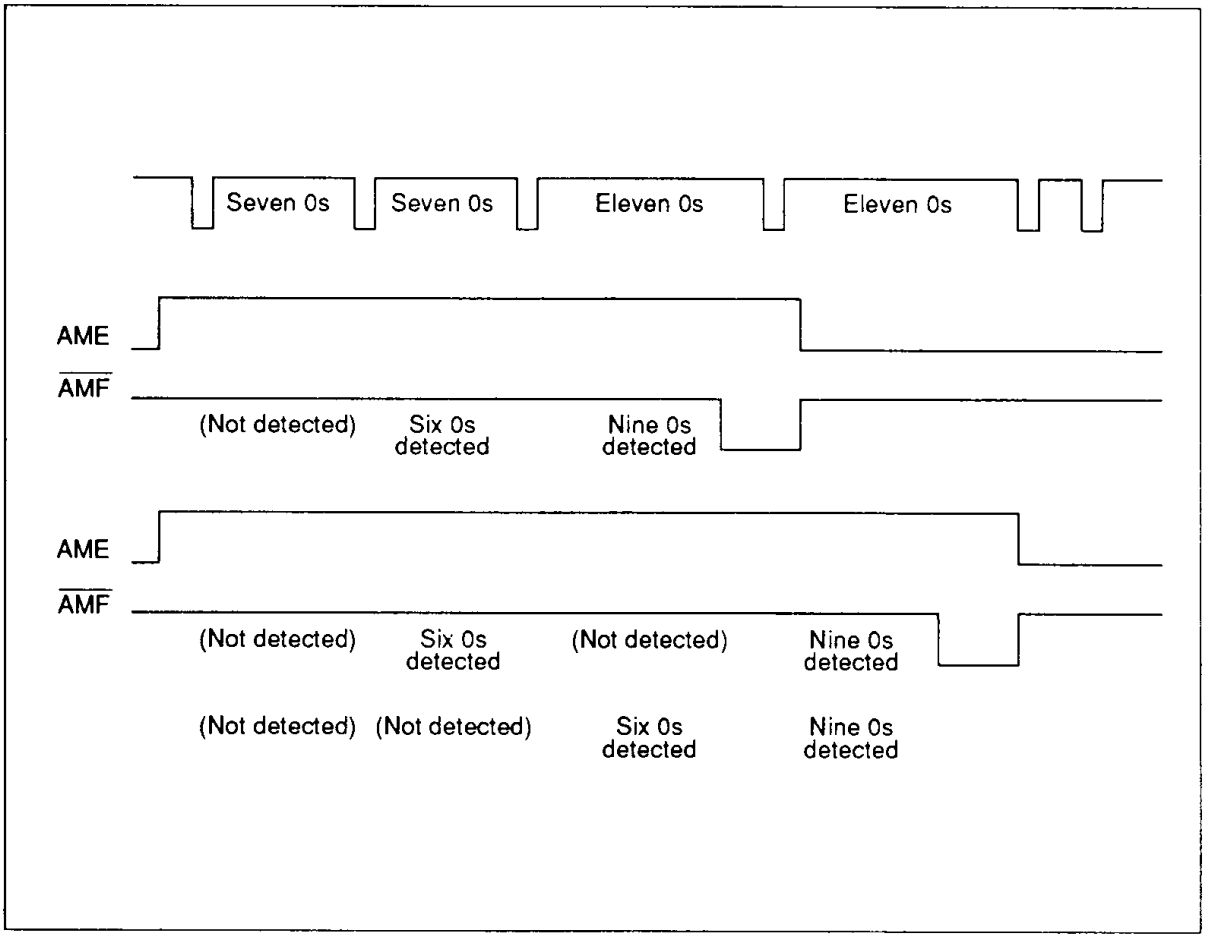
Address Mark Generation

- When the WG line is high, if the AME line is driven high for 1 to 3 byte lengths, the address mark pattern shown below is output on the 1-7WD line.
- Input on the NRZWD line should be 00....



Address Mark Detection

- When the WG line is low, address mark detection begins when the AME line is driven high.
- When six consecutive 0 bits are detected, the detector next looks for nine consecutive 0 bits.
- When nine consecutive 0 bits are detected, the $\overline{AMF}$ line is driven low.
- When the $\overline{AMF}$ line goes low, the disk controller should drive AME low to reset the $\overline{AMF}$ line to the high state.
- After six consecutive 0 bits are detected, if five 1 bits are input before nine consecutive 0 bits are detected, the detector starts looking for six consecutive 0 bits again.
- The $\overline{AMF}$ signal may be output at either of two times, as shown below.



Sync Field Detector

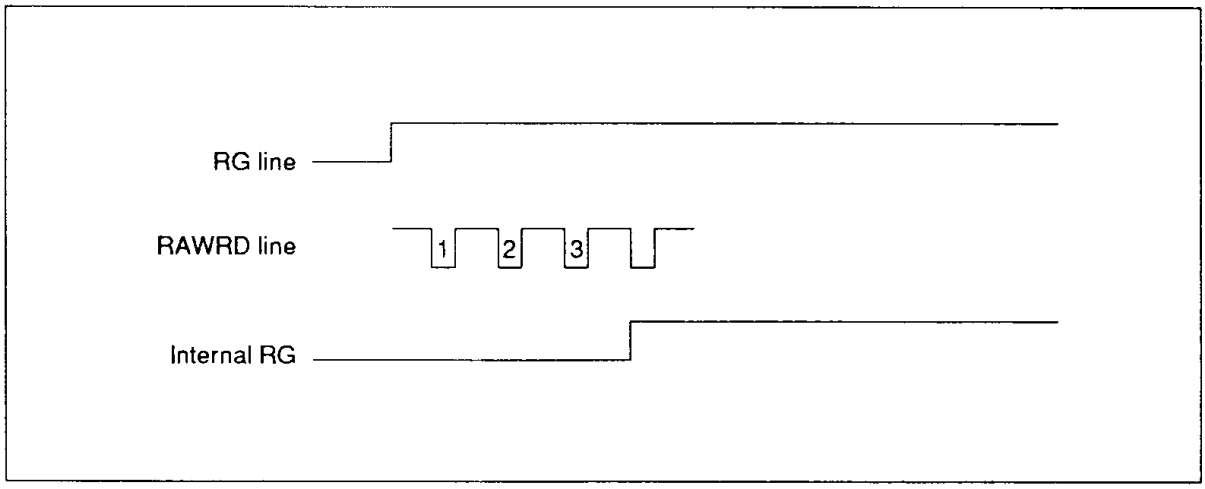
An on-chip sync field detector can ensure that read gating begins in a sync field. After the RG line goes high, the sync field detector waits until three consecutive 3T patterns are detected, then activates the internal RG line.

The RG detector should be enabled whenever soft sectoring is used. Set bit 4 in the MDC register. The high-gain period can be set to last four, six, or eight bytes after the internal RG signal is goes active. Bits 2 and 3 in register MDC select the high-gain period.

Sync Field Detector Enabled

MDC register

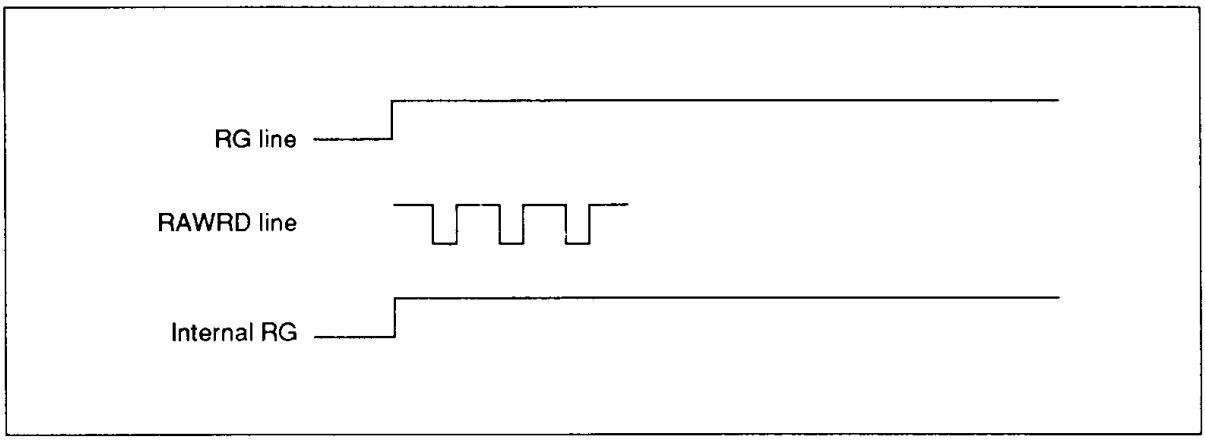
4	3	2	1	0	Format
1	—	—	—	—	Hard-sectored format or soft-sectored format
MSB				LSB	



Sync Field Detector Disabled

MDC register

4	3	2	1	0	Format
0	—	—	—	—	Hard-sectored format
MSB				LSB	



High-Gain Period

MDC register

4	3	2	1	0	High-gain period
—	0	0	—	—	6 Bytes
—	0	1	—	—	4 Bytes
—	1	0	—	—	8 Bytes
MSB				LSB	

Test Mode

The clock signals output by the encode clock generator's frequency synthesizer and the decode clock generator's VFO can be monitored directly by setting the chip to test mode. (In normal mode, these clock signals are divided and output from RRCLK.) The clock signals can be locked to the VCO center frequencies set by the resistors connected to the RSVCO and RFVCO lines by driving the $\overline{\text{RESET}}$ line low. The monitored clock frequency is 1.5 times the data transfer rate.

Setting Procedure

- Drive the TESTI1 line low.
- Set bit 4 in the GAC register to 1. This causes the clock signal from the encode clock generator's frequency synthesizer to be output on the TESTO0 line, and the clock signal from the decode clock generator's VFO on the TESTO3 line.

  Bit 4 in the DTC register and bit 4 in the WPC2 register must be cleared to 0. (See note)
- Drive the $\overline{\text{RESET}}$ line low. The encode clock output on the TESTO0 line will be locked to the center frequency set for the minimum data transfer rate by the resistor connected to the RSVCO line. The decode clock output on the TESTO3 line will be locked to the center frequency set for the minimum data transfer rate by the resistor connected to the RFVCO line.
- When the TESTI1 line is driven high, bit 4 in the GAC register is reset and normal mode resumes.

Note: During normal operation (when the TESTI1 line is high), bit 4 of these registers is held at 0 and cannot be written.

GAC register

D4	D3	D2	D1	D0
1	—	—	—	—
MSB				LSB

WPC2 register

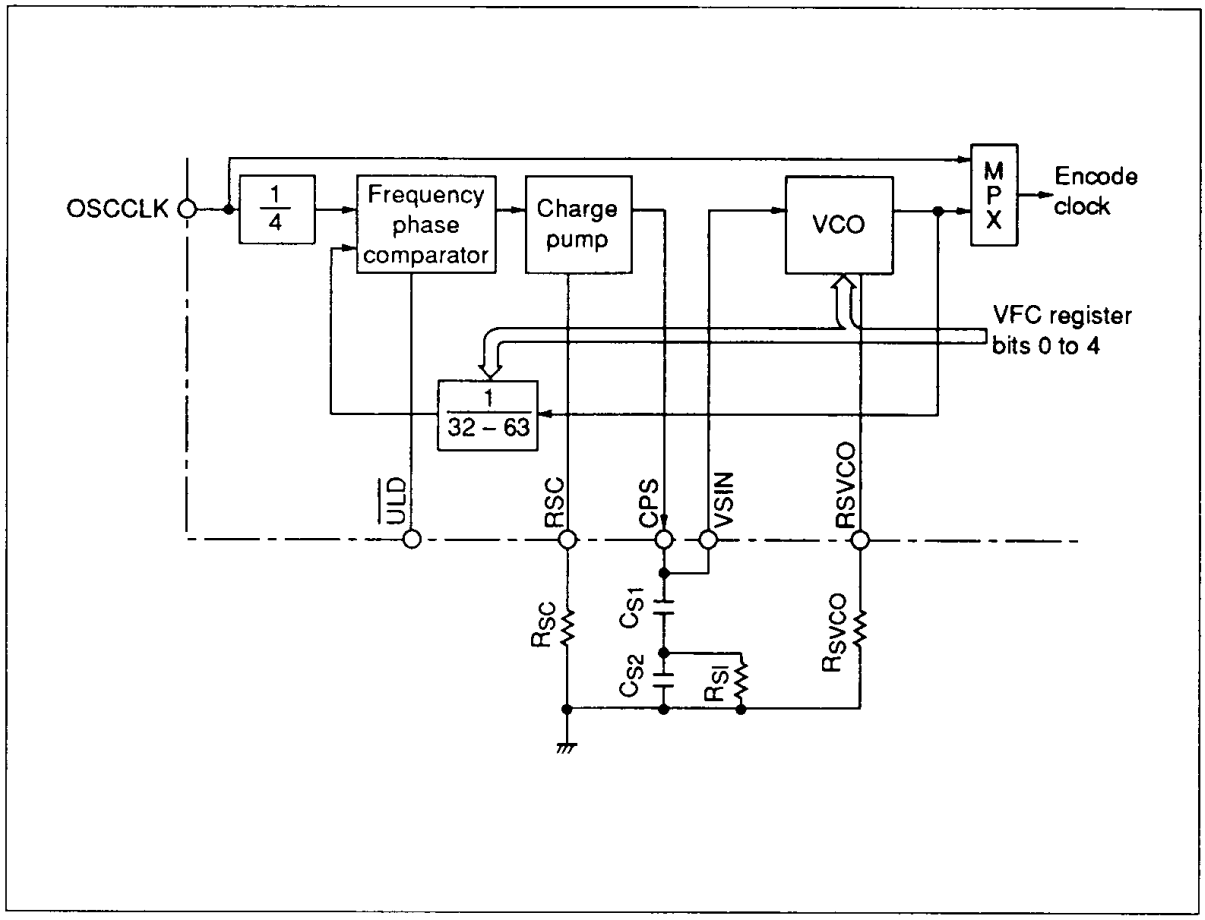
D4	D3	D2	D1	D0
0	—	—	—	—
MSB				LSB

DTC register

D4	D3	D2	D1	D0
0	—	—	—	—
MSB				LSB

Encode Clock Generator's Frequency Synthesizer

Block Diagram



Function

- A PLL-type frequency synthesizer generates the encode clock.
- The encode clock frequency can be set by bits 0 to 4 of register VFC to a value N/32 times the minimum data transfer rate (innermost track on the disk), where $32 \leq N \leq 63$.
- The lock/unlock function ($\overline{ULD}$ line) can prevent data from being written when a drive fault occurs.
- Direct, external input of the encode clock (at 1.5 times the transfer rate) is also possible without using the on-chip frequency synthesizer.
- The VCO center frequency can be selected by bits 0 to 4 of register VFC, so a single external resistor covers the entire setting range.

Operation

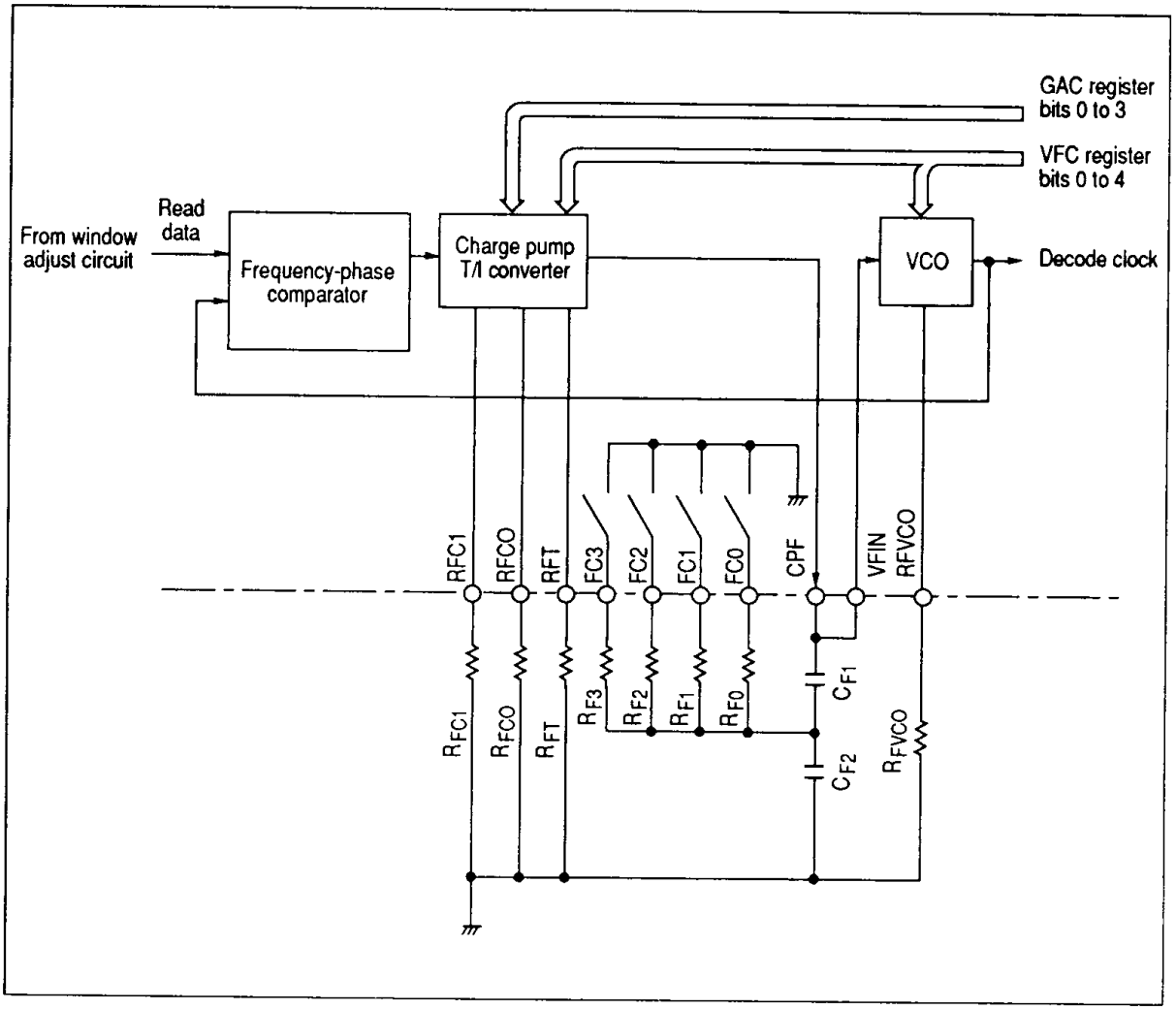
- Input a reference clock to OSCCLK at 1.5/8 times the drive's minimum transfer rate.
- This signal is internally divided by four and input to the frequency-phase comparator at 1/32 the normally required encoder clock rate.
- The VCO clock is divided by 1/32 to 1/63, depending on bits 0 to 4 of register VFC, and input to the frequency-phase comparator.

$$f_{VCO(W)} = \frac{N}{32} \times f_{LOW} \qquad 32 \leq N \leq 63$$

$f_{VCO(W)}$: VCO output frequency
f_{LOW}: Encoder clock frequency corresponding to minimum transfer rate

Decode Clock Generator's VFO

Block Diagram



Function

- The phase of the VCO clock is synchronized with the read data from the window adjust circuit.
- The frequency-phase comparator operates in the frequency-phase comparison mode while acquiring phase lock in the sync field, and in phase comparison mode during synchronization in the data field.
- The charge pump and T/I converter circuits both operate while phase lock is being acquired. During synchronization, only the T/I converter operates.
- The VFO is synchronized with the encode clock until the read gate signal (RG) is asserted.
- The VCO center frequency can be changed by rewriting bits 0 to 4 of the VFC register, so zone bit recording can be implemented with only a single external resistor.
- The charge pump can provide two output currents, the values of which are controlled by external resistors R_{FC0} and R_{FC1}. Bit 3 in register GAC selects either of these two currents.
- The T/I converter provides one of eight output currents as selected by bits 0 to 2 of register GAC.
- The loop filter attenuation ζ can be selected by bit 3 of register GAC (two selections). Independent settings can be made for high gain and normal gain.

Calculation of PLL Constants

I. Encode Clock Generator's Frequency Synthesizer

1. VCO center frequency f_{OW}

$$f_{OW} = \frac{(2.8125 \times 10^9) \cdot N}{R_{SVCO}} \quad (Hz) \qquad \text{(I.1)}$$

2. VCO gain K_{OW}

$$K_{OW} = (5.215 \times 10^8) - \sqrt{\frac{N}{R_{SVCO}}} \quad \left(\frac{rad}{s \cdot V}\right) \qquad \text{(I.2)}$$

3. Charge pump current I_{CW}

$$I_{CW} = \frac{1.0}{R_{SC}} \quad (A) \qquad \text{(I.3)}$$

4. Characteristic frequency ω_{nW}

$$\omega_{nW} = \sqrt{\frac{K_{OW} \geq I_{CW}}{2\pi N \cdot C_{S1}}} \quad \left(\frac{rad}{s}\right) \qquad \text{(I.4)}$$

5. Attenuation ζ_W

$$\zeta_W = \frac{(C_{S1} + C_{S2})}{2} \cdot R_{S1} \cdot \omega_{nW} \qquad \text{(I.5)}$$

II. Decode Clock Generator's VFO

1. VCO center frequency f_{OR}

$$f_{OR} = \frac{(2.8125 \times 10^9) \cdot N}{R_{FVCO}} \quad (Hz) \qquad \text{(II.1)}$$

2. VCO gain K_{OR}

$$K_{OR} = (1.015 \times 10^9) \cdot \sqrt{\frac{N}{R_{FVCO}}} \quad \left(\frac{rad}{s \cdot V}\right) \qquad \text{(II.2)}$$

3. Charge pump current I_{CR}

$$I_{CR} = \frac{3.0}{R_{FC}} \quad (A) \qquad \text{(II.3)}$$

where R_{FC} = RFC0 when GAC register bit 3 = 0
RFC1 when GAC register bit 3 = 1

4. T/I converter external resistance RFT

$$R_{FT} = 4 \cdot R_{FVCO} \quad \text{..... (II.4)}$$

5. T/I converter current I_{TR}

$$I_{TR} = (1.5625 \times 10^{-3}) \cdot \frac{N \cdot L}{R_{FT}} \quad (A) \quad \text{..... (II.5)}$$

where $1 \leq L \leq 8$

6. Characteristic frequency (high gain) ω_{nRH}

$$\omega_{nRH} = \sqrt{\frac{K_{OR} \cdot \left(\frac{I_{CR}}{6} + I_{TR}\right)}{\pi \cdot C_{F1}}} \quad \left(\frac{rad}{s}\right) \quad \text{..... (II.6)}$$

7. Characteristic frequency (normal gain) ω_{nRN}

$$\omega_{n\,RH} = \sqrt{\frac{K_{OR} \cdot I_{TR}}{\pi \cdot C_{F1}}} \quad \left(\frac{rad}{s}\right) \quad \text{..... (II.7)}$$

8. Attenuation (high gain) ζ_{RH}

$$\zeta_{RH} = \frac{(C_{F1} + C_{F2})}{2} \cdot \frac{1}{\frac{1}{R_{FA}} + \frac{1}{R_{FB}}} \cdot \omega_{nRH} \quad \text{..... (II.8)}$$

where R_{FA} and R_{FB} = RF2 and RF3 when GAC register bit 3 = 0
RF0 and RF1 when GAC register bit 3 = 1

9. Attenuation (normal gain) ζ_{RN}

$$\zeta_{RN} = \frac{(C_{F1} + C_{F2})}{2} \cdot R_{FA} \cdot \omega_{nRN} \quad \text{..... (II.9)}$$

where R_{FA} = RF2 when GAC register bit 3 = 0
RF0 when GAC register bit 3 = 1

Table 1 VCO Oscillation Frequency and Transfer Speed for Settings of Register VFC

	VFC register							Example: R_{FVCO} and R_{SVCO} = 3 kΩ	
	Bits						VCO oscillation frequency and transfer speed ratio	VCO center frequency (MHz)	Transfer speed (Mbps)
	4	3	2	1	0	N			
1	0	0	0	0	0	32	1.00000	30.0000	20.000
2	0	0	0	0	1	33	1.03125	30.9375	20.625
3	0	0	0	1	0	34	1.06250	31.8750	21.250
4	0	0	0	1	1	35	1.09375	32.8125	21.875
5	0	0	1	0	0	36	1.12500	33.7500	22.500
6	0	0	1	0	1	37	1.15625	34.6875	23.125
7	0	0	1	1	0	38	1.18750	35.6250	23.750
8	0	0	1	1	1	39	1.21875	36.5625	24.375
9	0	1	0	0	0	40	1.25000	37.5000	25.000
10	0	1	0	0	1	41	1.28125	38.4375	25.625
11	0	1	0	1	0	42	1.31250	39.3750	26.250
12	0	1	0	1	1	43	1.34375	40.3125	26.875
13	0	1	1	0	0	44	1.37500	41.2500	27.500
14	0	1	1	0	1	45	1.40625	42.1875	28.125
15	0	1	1	1	0	46	1.43750	43.1250	28.750
16	0	1	1	1	1	47	1.46875	44.0625	29.375
17	1	0	0	0	0	48	1.50000	45.0000	30.000
18	1	0	0	0	1	49	1.53125	45.9375	30.625
19	1	0	0	1	0	50	1.56250	46.8750	31.250
20	1	0	0	1	1	51	1.59375	47.8125	31.875
21	1	0	1	0	0	52	1.62500	48.7500	32.500
22	1	0	1	0	1	53	1.65625	49.6875	33.125
23	1	0	1	1	0	54	1.68750	50.6250	33.750
24	1	0	1	1	1	55	1.71875	51.5625	34.375

VCO Oscillation Frequency and Transfer Speed for Settings of Register VFC (cont)

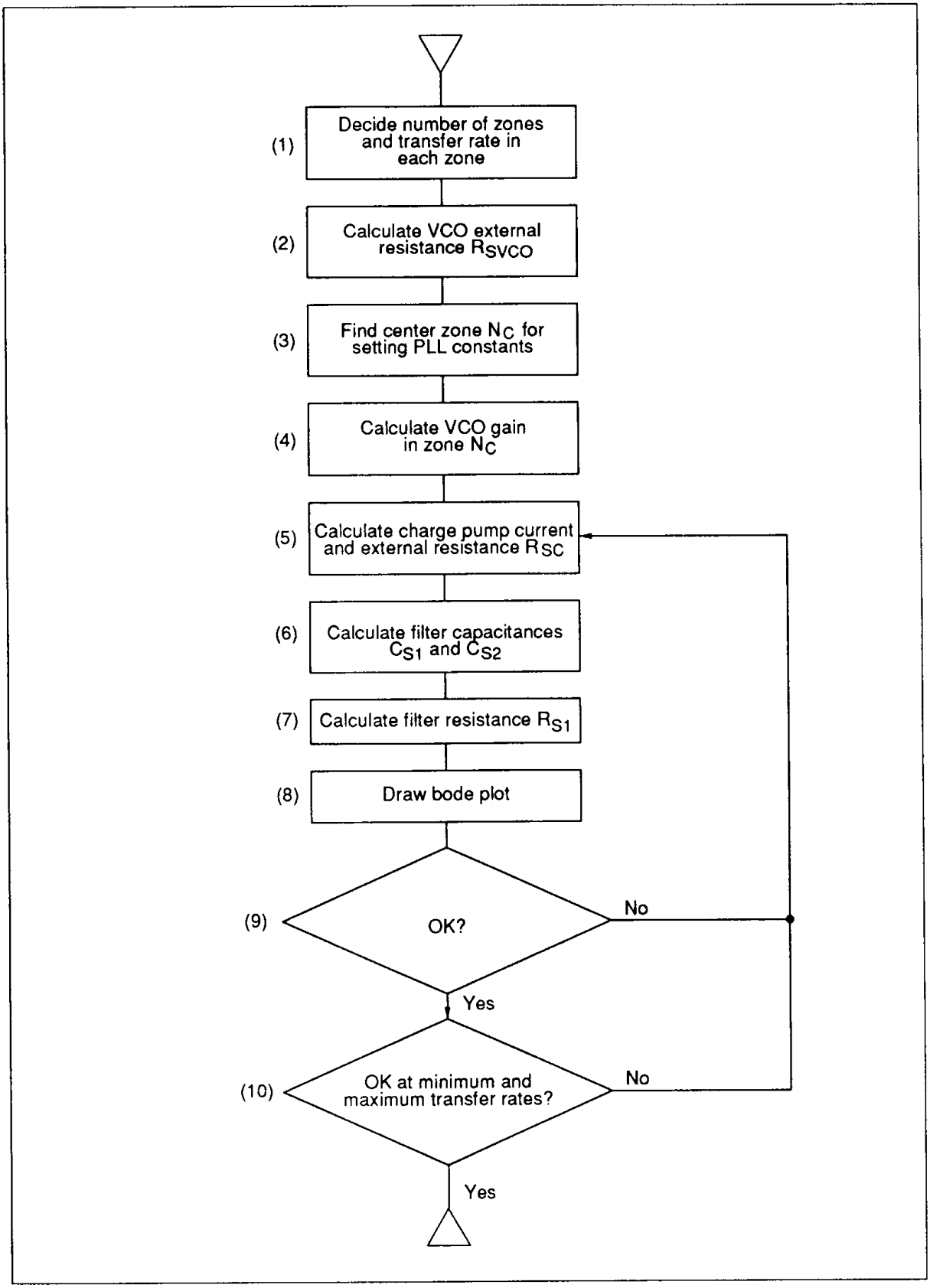
	VFC register Bits							Example: R_{FVCO} and R_{SVCO} = 3 kΩ	
	4	3	2	1	0	N	VCO oscillation frequency and transfer speed ratio	VCO center frequency (MHz)	Transfer speed (Mbps)
25	1	1	0	0	0	56	1.75000	52.5000	35.000
26	1	1	0	0	1	57	1.78125	53.4375	35.625
27	1	1	0	1	0	58	1.81250	54.3750	36.250
28	1	1	0	1	1	59	1.84375	55.3125	36.875
29	1	1	1	0	0	60	1.87500	56.2500	37.500
30	1	1	1	0	1	61	1.90625	57.1875	38.125
31	1	1	1	1	0	62	1.93750	58.1250	38.750
32	1	1	1	1	1	63	1.96875	59.0625	39.375

Table 2 T/I Output Current Settings in Register GAC

	GAC register Bits					Example: R_{FT} = 12 kΩ
	2	1	0	L	T/I output current ratio	T/I output current (μA)
1	0	0	0	1	1	4.17
2	0	0	1	2	2	8.33
3	0	1	0	3	3	12.5
4	0	1	1	4	4	16.7
5	1	0	0	5	5	20.8
6	1	0	1	6	6	25.0
7	1	1	0	7	7	29.2
8	1	1	1	8	8	33.3

Note: VFC register bits 4 to 0: 00000 (N = 32)

1. Flowchart of Procedure for Setting Encoder Clock Generator's Frequency Synthesizer Constants



1.1 Flowchart Explanation

(1) Decide number of zones and transfer rate in each zone

The HD153021F uses a frequency synthesizer to generate the reference clock, so the value of the transfer rate is quantized. If the lowest rate corresponds to N = 32, the available rates are given by the formula:

$$TR_N = \frac{N}{32} TRmin, \quad 32 \leq N \leq 63$$

where, TR_N: Transfer rates in different zones
TRmin: Minimum transfer rate (innermost track)

(2) Calculate VCO external resistance R_{SVCO}

Use equation (I.1) to calculate the external resistance R_{SVCO} that makes the VCO oscillate at 1.5 times the minimum transfer rate (N = 32)

(3) Find center zone (TRcen)

Calculate the midpoint (TRcen) between the minimum transfer rate (TRmin) and maximum transfer rate (TRmax), and from the zones selected in step (1), find the value of N (N_C) that comes closest to TRcen.

$$TRcen = \frac{TRmin + TRmax}{2}$$

(4) VCO gain K_{OW}

Use equation (I.2) to calculate the VCO gain ζ in the center zone ($N = N_C$).

(5) Charge pump current I_{CW}

Select the charge pump current within the following range:

$I_{CW} \leq 200$ (μA)

Calculate the necessary external resistance R_{SC} from equation (I.3).
This data sheet recommends I_{CW} = 100 μA, provided the desired loop characteristics can be obtained with this value.

(6) Filter capacitances C_{S1} and C_{S2}

Decide the phase-lock acquisition time Taq, considering the change in characteristic frequency from zone to zone and the head seek time. The value used in this data sheet is:

Taq = 0.9 (ms)

The following formula gives an estimate of the acquisition time:

$\omega_{nW} \cdot Taq = 5.4$

Substitute the values of K_{OW} and I_{CW} into equation (I.4) and combine with the formula above to calculate the filter capacitance C_{S1}. To suppress jitter and allow a phase margin, the following value is recommended for C_{S2}:

$$C_{S2} = \frac{1}{65} C_{S1}$$

(7) Filter resistance R_{S1}

To ensure loop stability, set the attenuation to approximately:

$\zeta_W = 1.5$

Substitute this value into equation (I.5) to calculate the filter resistance R_{S1}.

(8) Bode plot

Calculate the open-loop transfer function G(s) and draw a Bode plot.

(9) OK?

Decide whether the open-loop and closed-loop characteristics are satisfactory.

(10) OK at TRmin and TRmax?

Repeat steps (8) and (9) for the minimum and maximum transfer rates.

1.2 Example of Settings

The preceding calculations are shown below for a sample HD153021F application.

(1) Decide number of zones and transfer rate in each zone

Zone	Transfer rate	N	VFC register 4 3 2 1 0
I	20.000	32	0 0 0 0 0
II	21.875	35	0 0 0 1 1
III	23.750	38	0 0 1 1 0
IV	25.625	41	0 1 0 0 1
V	27.500	44	0 1 1 0 0
VI	29.375	47	0 1 1 1 1
VII	31.875	51	1 0 0 1 1

(2) VCO external resistance R_{SVCO}

$$R_{SVCO} = \frac{2.8125 \times 10^9 \times 32}{3.0 \times 10^7} = 3.0 \quad (k\Omega)$$

(3) Center zone (TRcen)

$$TRcen = \frac{(20.000 + 31.875) \times 10^6}{2} = 25.9375 \times 10^6 \quad (bps)$$

Closest value of N is $N_C = 41$.

(4) VCO gain K_{OW}

$$K_{OW} = 5.215 \times 10^8 \times \sqrt{\frac{41}{3.0 \times 10^7}} = 61.0 \quad \left(\frac{Mrad}{s \cdot V}\right)$$

(5) Charge pump current I_{CW} and external resistance R_{SC}

$$I_{CW} = 100 \quad (\mu A)$$

$$R_{SC} = \frac{1.0}{1.0 \times 10^{-4}} = 10 \quad (k\Omega)$$

(6) Filter capacitances C_{S1} and C_{S2}

$$\omega_{nW} = \frac{5.4}{9.0 \times 10^{-4}} = 6.0 \quad \left(\frac{krad}{s}\right)$$

$$C_{S1} = \frac{6.1 \times 10^{7} \times 1.0 \times 10^{-4}}{2\pi \times 41 \times (6.0 \times 10^{3})^{2}} \cong 0.68 \quad (\mu F)$$

$$C_{S2} = \frac{6.8 \times 10^{-7}}{65} \cong 0.01 \quad (\mu F)$$

(7) Filter resistance R_{S1}

$$\omega_{nW} = \sqrt{\frac{6.1 \times 10^{7} \times 1.0 \times 10^{-4}}{2\pi \times 41 \times 6.8 \times 10^{-7}}} = 5.9 \quad \left(\frac{krad}{s}\right)$$

$$R_{S1} = \frac{1.5 \times 2}{(6.8 \times 10^{-7} + 1.0 \times 10^{-8}) \times 5.9 \times 10^{3}} = 750 \quad (\Omega)$$

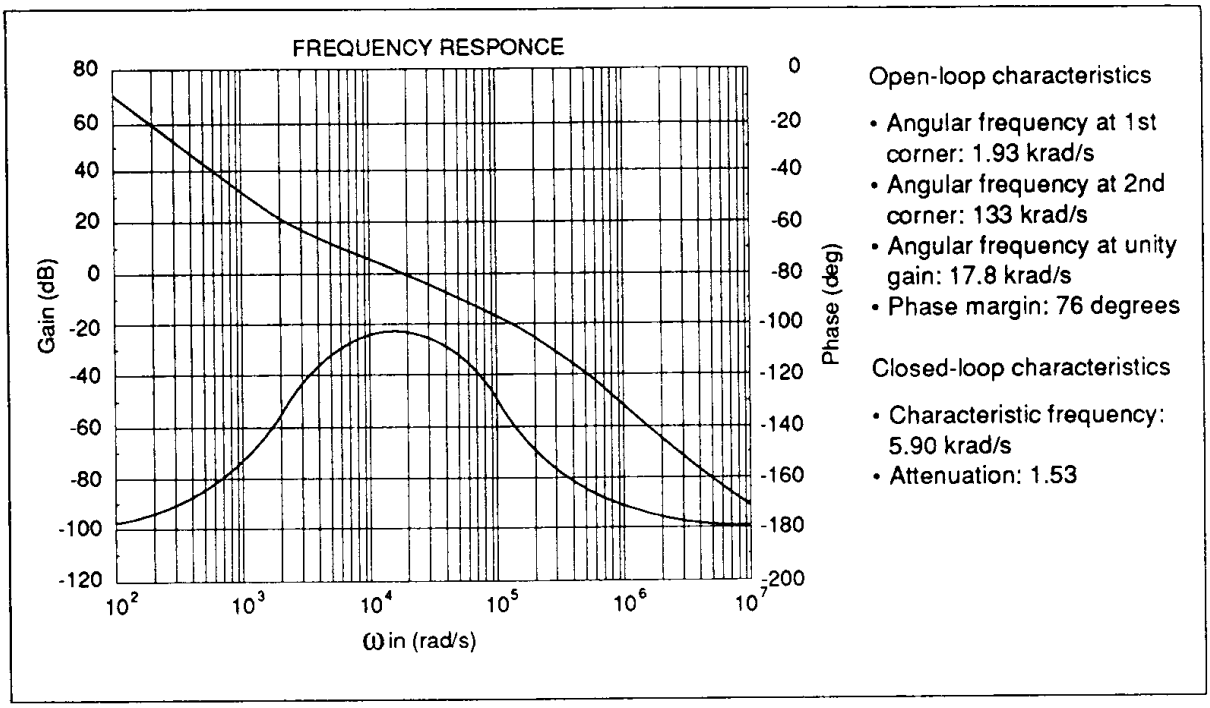
at which

$$\zeta_{W} = \frac{(6.8 \times 10^{-7} + 1.0 \times 10^{-8})}{2} \times 750 \times 5.9 \times 10^{3} = 1.52$$

(8) Bode plot

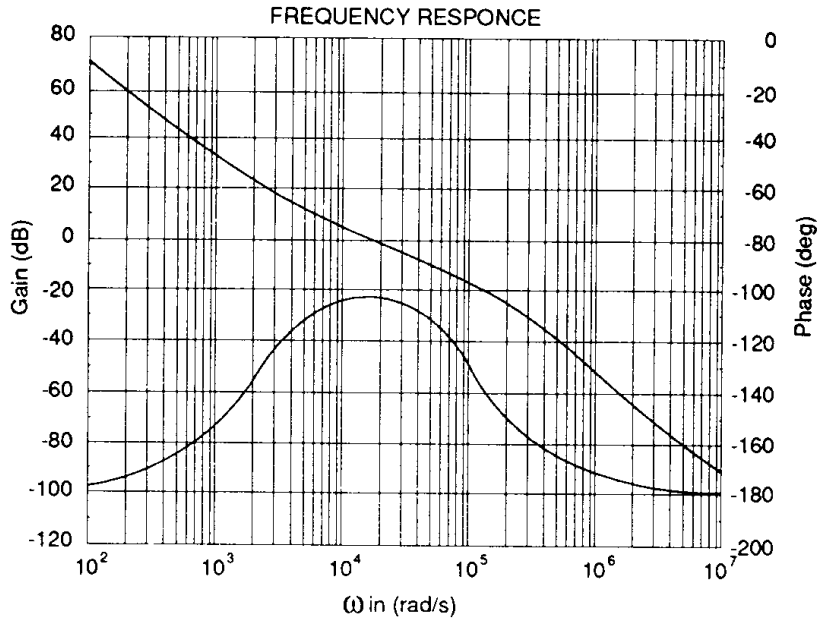
The open-loop frequency response is shown below. (N = 41)

(9) OK?



(10) OK at TRmin and TRmax?

(a) TRmin (N = 32)



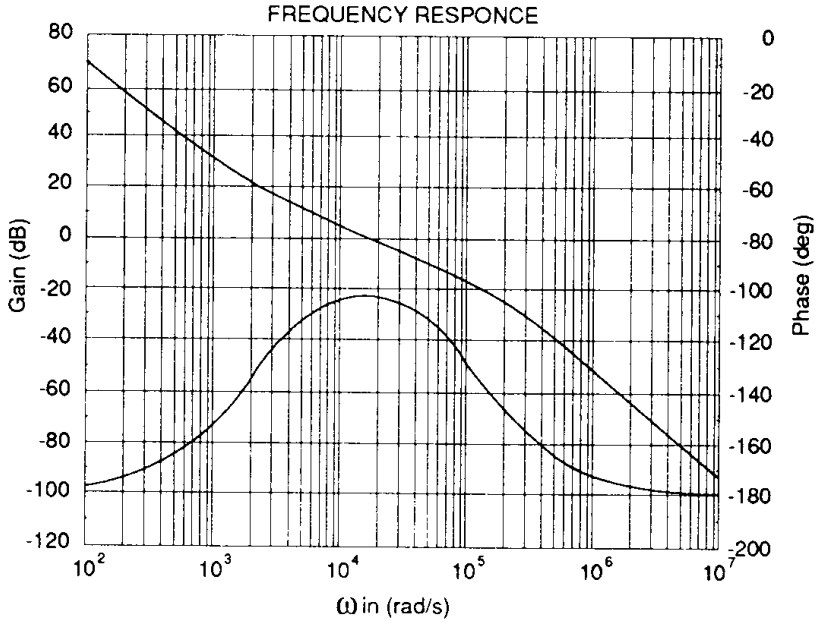
Open-loop characteristics

- Angular frequency at 1st corner: 1.93 krad/s
- Angular frequency at 2nd corner: 133 krad/s
- Angular frequency at unity gain: 20.4 krad/s
- Phase margin: 76 degrees

Closed-loop characteristics

- Characteristic frequency: 6.28 krad/s
- Attenuation: 1.62

(b) TRmax (N = 51)



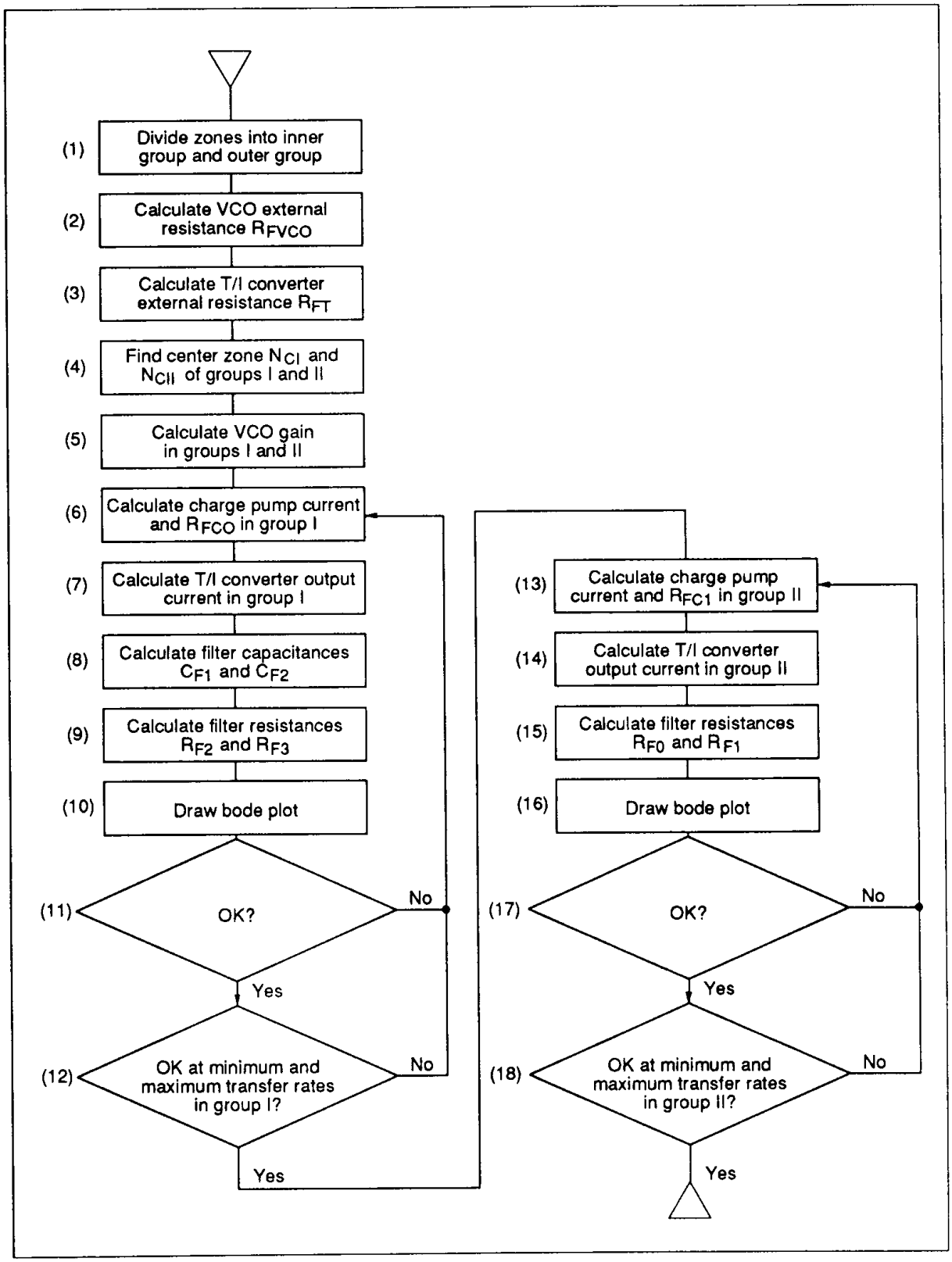
Open-loop characteristics

- Angular frequency at 1st corner: 1.93 krad/s
- Angular frequency at 2nd corner: 133 krad/s
- Angular frequency at unity gain: 16.2 krad/s
- Phase margin: 76 degrees

Closed-loop characteristics

- Characteristic frequency: 5.59 krad/s
- Attenuation: 1.45

2. Flowchart of Procedure for Setting Encoder Clock Generator's VFO Constants



2.1 Flowchart Explanation

(1) Divide zones into groups

Divide the zones selected in step 1.1.(1) into two groups (I and II) having equal frequency ranges. Divide the groups at the following transfer rate TGgr:

$$TRgr = \sqrt{TRmin \cdot TRmax}$$

(2) VCO external resistance R_{FVCO}

Use equation (II.1) to calculate the external resistance R_{FVCO} that makes the VCO oscillate at 1.5 times the minimum transfer rate (N = 32)
Note: In general, R_{FVCO} should have the same resistance value as R_{SVCO}

(3) T/I converter external resistance R_{FT}

Calculate R_{FT} from equation (II.4).

(4) Center zones TR_{CI} and TR_{CII} of groups I and II

Find N_{CI} and N_{CII} in groups I and II by the same method as in step 1.1.(3).

(5) VCO gain K_{OR} in groups I and II

Use equation (II.2) to calculate the VCO gain K_{OR} at the center zones ($N = N_{CI}$ and $N = N_{CII}$) in groups I and II.

(6) Charge pump current I_{CR} in group I

Select the charge pump current within the following range:

$$I_{CR} \leq 3.0 \quad (mA)$$

Calculate the necessary external resistance R_{FC0} from equation (II.3).
This data sheet recommends I_{CR} = 2.0 mA, provided the desired loop characteristics can be obtained with this value.

(7) T/I converter output current I_{TR} in group I

Decide the ratio A_G between high gain and normal gain, and use equation (II.5) to calculate a value of L ($1 \leq L \leq 8$) that gives the following relationship:

$$I_{TR} = \frac{I_{CR}}{6\,(A_G - 1)}$$

See table 2 for the relationship between L and register GAC.

(8) Filter capacitances C_{F1} and C_{F2}

Decide the phase-lock acquisition time Taq in the center zone N_{CI} of group I, considering the high-gain interval specified in the MDC register.
The following formula gives an estimate of the acquisition time:

$$\omega_{nRH} \cdot Taq = 5.7$$

Combine this formula with equation (II.6) to calculate the filter capacitance C_{F1}.
To suppress jitter and allow a phase margin, the following value is recommended for C_{F2}:

$$C_{F2} = \frac{1}{45} C_{F1}$$

Substitute the value of C_{F1} into equation (II.7) to calculate the normal-gain characteristic frequency ω_{nRN}.

(9) Filter resistances R_{F2} and R_{F3}

For quick acquisition, set the high-gain attenuation ζ_{RH} to approximately:

$$\zeta_{RH} \cong 0.8$$

For stability, set the normal-gain attenuation ζ_{RN} to approximately:

$$\zeta_{RN} \cong 1.0$$

Substitute these values into equations (II.8) and (II.9) to calculate the filter resistances R_{F2} and R_{F3}.

(10) Bode plot

Calculate the open-loop transfer function G(s) and draw a Bode plot.

(11) OK?

Decide whether the open-loop and closed-loop characteristics are satisfactory.

(12) OK at TRmin and TRmax?

Repeat steps (10) and (11) for the minimum and maximum transfer rates in group I.

(13) Charge pump current I_{CR} in group II

Select the charge pump current within the following range:

$I_{CR} \leq 4.0$ (mA)

Decide the phase-lock acquisition time Taq in the center zone N_{CII} of group II, considering the high-gain interval specified in the MDC register.
The following formula gives an estimate of the acquisition time:

$\omega_{n\,RH} \cdot Taq = 5.7$

Combine this formula with equation (II.6) to calculate the charge pump current I_{CR}. Use the value calculated in step (7) for I_{TR}.
Substitute the value of the charge pump current I_{CR} into equation (II.3) to calculate the necessary resistance R_{FC1}.

(14) T/I converter output current I_{TR} in group I

Decide the ratio A_G between high gain and normal gain, and use equation (II.5) to calculate a value of L ($1 \leq L \leq 8$) that gives the following relationship:

$$I_{TR} = \frac{I_{CR}}{6\,(A_G - 1)}$$

See table 2 for the relationship between L and register GAC.
Next, substitute the charge pump current I_{CR} and T/I converter current I_{TR} into equations (II.6) and (II.7) and calculate the high-gain and normal-gain characteristic frequencies ω_{nRH} and ω_{nRN}.

(15) Filter resistances R_{F0} and R_{F1}

For quick acquisition, set the high-gain attenuation ζ_{RH} to approximately:

$\zeta_{RH} \cong 0.8$

For stability, set the normal-gain attenuation ζ_{RN} to approximately:

$\zeta_{RN} \cong 1.0$

Substitute these values into equations (II.8) and (II.9) to calculate the filter resistances R_{F0} and R_{F1}.

(16) Bode plot

Calculate the open-loop transfer function G(s) and draw a Bode plot.

(17) OK?

Decide whether the open-loop and closed-loop characteristics are satisfactory.

(18) OK at TRmin and TRmax?

Repeat steps (16) and (17) for the minimum and maximum transfer rates in group II.

2.2 Example of Settings

The preceding calculations are shown below for a sample HD153021F application.

(1) Divide zones into groups

$$TRgr = \sqrt{20.000 \times 10^6 \times 31.875 \times 10^6} = 25.249 \times 10^6 \quad \text{(bps)}$$

The zones divide into two groups as follows:

Group	Zone	Transfer rate (Mbps)	N	VFC register
I	1	20.000	32	0 0 0 0 0
	2	21.875	35	0 0 0 1 1
	3	23.750	38	0 0 1 1 0
II	4	25.625	41	0 1 0 0 1
	5	27.500	44	0 1 1 0 0
	6	29.375	47	0 1 1 1 1
	7	31.875	51	1 0 0 1 1

(2) VCO external resistance R_{FVCO}

$$R_{FVCO} = \frac{2.8125 \times 10^9 \times 32}{3.0 \times 10^7} = 3.0 \quad (k\Omega)$$

(3) T/I converter external resistance R_{FT}

$$R_{FT} = 4 \times 3.0 \times 10^3 = 12 \quad (k\Omega)$$

(4) Center zones TR_{CI} and TR_{CII} of groups I and II

$$TR_{CI} = \frac{(20.000 + 23.750) \times 10^6}{2} = 21.875 \times 10^6 \quad \text{(bps)}$$

$$TR_{CII} = \frac{(25.625 + 31.875) \times 10^6}{2} = 28.750 \times 10^6 \quad \text{(bps)}$$

From table 1, the closest values of N are:

Group	N_C	Transfer rate (Mbps)	VFC Register
I	35	21.875	0 0 0 1 1
II	46	28.750	0 1 1 1 0

(5) VCO gain K_{OR} in groups I and II

$$K_{ORI} = 1.015 \times 10^9 \times \sqrt{\frac{35}{3.0 \times 10^3}} = 110 \quad \left(\frac{\text{Mrad}}{\text{s} \cdot \text{V}}\right)$$

$$K_{ORII} = 1.015 \times 10^9 \times \sqrt{\frac{46}{3.0 \times 10^3}} = 126 \quad \left(\frac{\text{Mrad}}{\text{s} \cdot \text{V}}\right)$$

(6) Charge pump current I_{CR} in group I

$$I_{CR} = 2.0 \quad (\text{mA})$$

$$R_{FC0} = \frac{3.0}{2 \times 10^{-3}} = 1.5 \quad (\text{k}\Omega)$$

(7) T/I converter output current I_{TR} in group I

$$A_G = 14$$

Therefore:

$$I_{TR} = \frac{2 \times 10^{-3}}{6 \times (14 - 1)} = 25.6 \quad (\mu\text{A})$$

Substituting this value into equation (2.5):

$$25.6 \times 10^{-6} = 1.5625 \times 10^{-3} \times \frac{35 \times L}{12 \times 10^3}$$

$$L \equiv 6$$

Which gives I_{TR} as follows:

$$I_{TR} = 1.5625 \times 10^{-3} \times \frac{35 \times 6}{12 \times 10^3} = 27.3 \quad (\mu\text{A})$$

(8) Filter capacitances C_{F1} and C_{F2}

The high-gain interval in this application is 6 bytes.

MDC Register

Bit	3	2
Value	0	0

The phase-lock acquisition time Taq is:

$$Taq = \frac{8}{21.875 \times 10^6} \times 6 = 2.2 \quad (\mu s)$$

The characteristic frequency ω_{nRH} is accordingly:

$$\omega_{nRH} = \frac{5.7}{2.2 \times 10^{-6}} = 2.6 \quad \left(\frac{Mrad}{s}\right)$$

Therefore:

$$2.6 \times 10^6 = \sqrt{\frac{110 \times 10^6 \times \left(\frac{2.0 \times 10^{-3}}{6} + 27.3 \times 10^{-6}\right)}{3.14 \times C_{F1}}}$$

$$C_{F1} = 1800 \quad (pF)$$

C_{F2} is therefore:

$$C_{F2} = \frac{1800 \times 10^{-12}}{45} \cong 39 \quad (pF)$$

The normal-gain characteristic frequency ω_{nRN} is:

$$\omega_{nRN} = \sqrt{\frac{110 \times 10^6 \times 27.3 \times 10^{-6}}{3.14 \times 1800 \times 10^{-12}}} \cong 730 \quad \left(\frac{krad}{s}\right)$$

(9) Filter resistances R_{F2} and R_{F3}

$$R_{F2} = 1.0 \times \frac{2}{(1800 + 39) \times 10^{-12}} \times \frac{1}{730 \times 10^3} = 1.5 \quad (k\Omega)$$

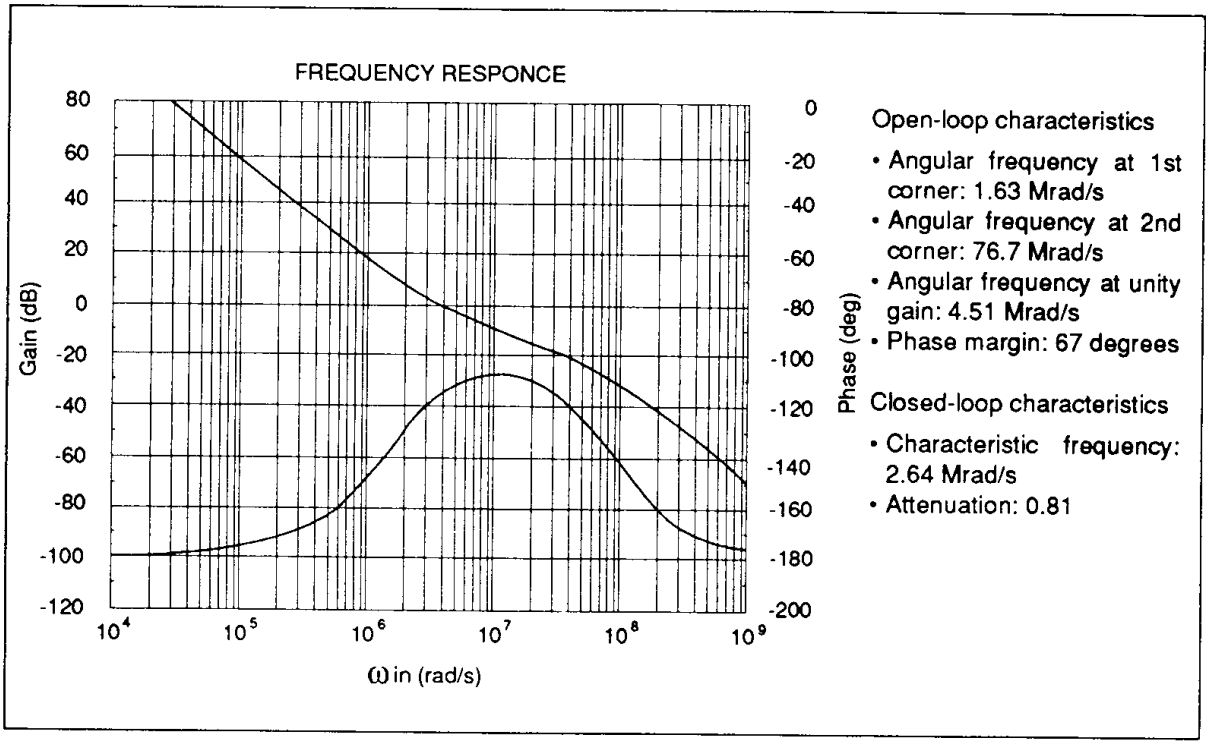
$$0.8 = \frac{(1800 + 39) \times 10^{-12}}{2} \times \frac{1}{\frac{1}{1.5 \times 10^3} + \frac{1}{R_{F3}}} \times 2.6 \times 10^6$$

$$R_{F3} = 430 \quad (\Omega)$$

(10), (11) Bode plot

N = 35

(High gain)



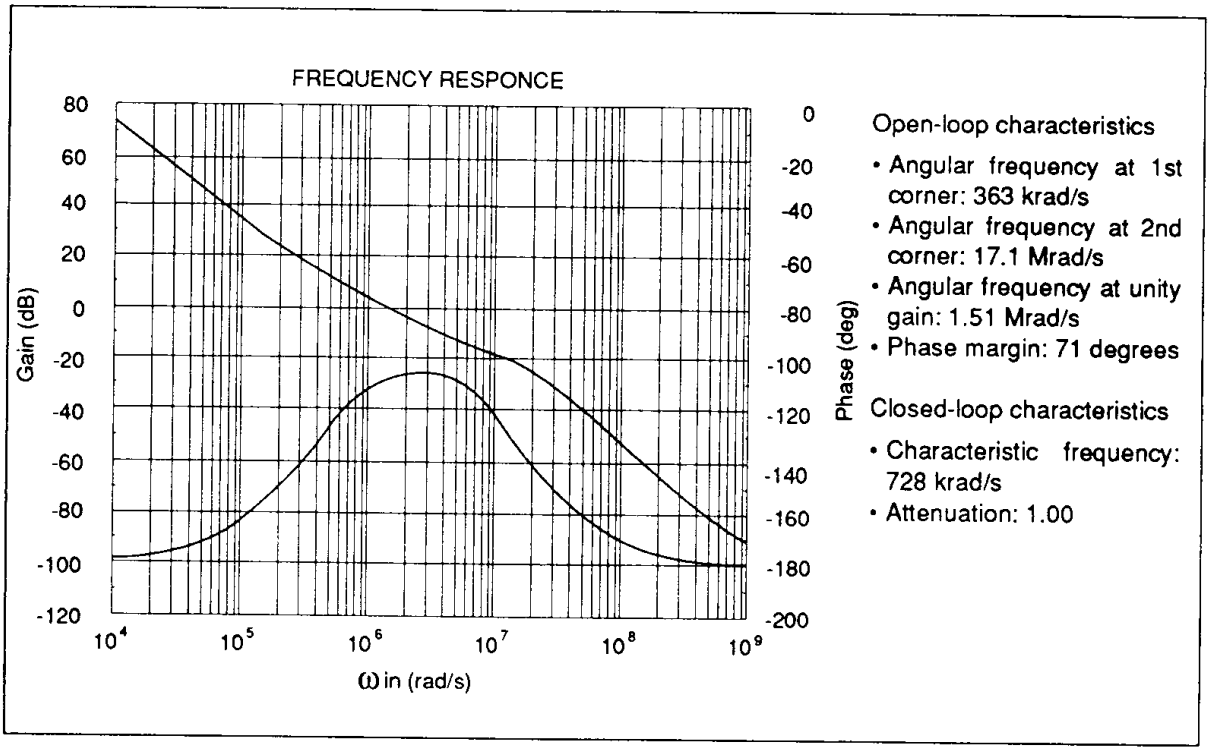
Open-loop characteristics

- Angular frequency at 1st corner: 1.63 Mrad/s
- Angular frequency at 2nd corner: 76.7 Mrad/s
- Angular frequency at unity gain: 4.51 Mrad/s
- Phase margin: 67 degrees

Closed-loop characteristics

- Characteristic frequency: 2.64 Mrad/s
- Attenuation: 0.81

(Normal gain)



Open-loop characteristics

- Angular frequency at 1st corner: 363 krad/s
- Angular frequency at 2nd corner: 17.1 Mrad/s
- Angular frequency at unity gain: 1.51 Mrad/s
- Phase margin: 71 degrees

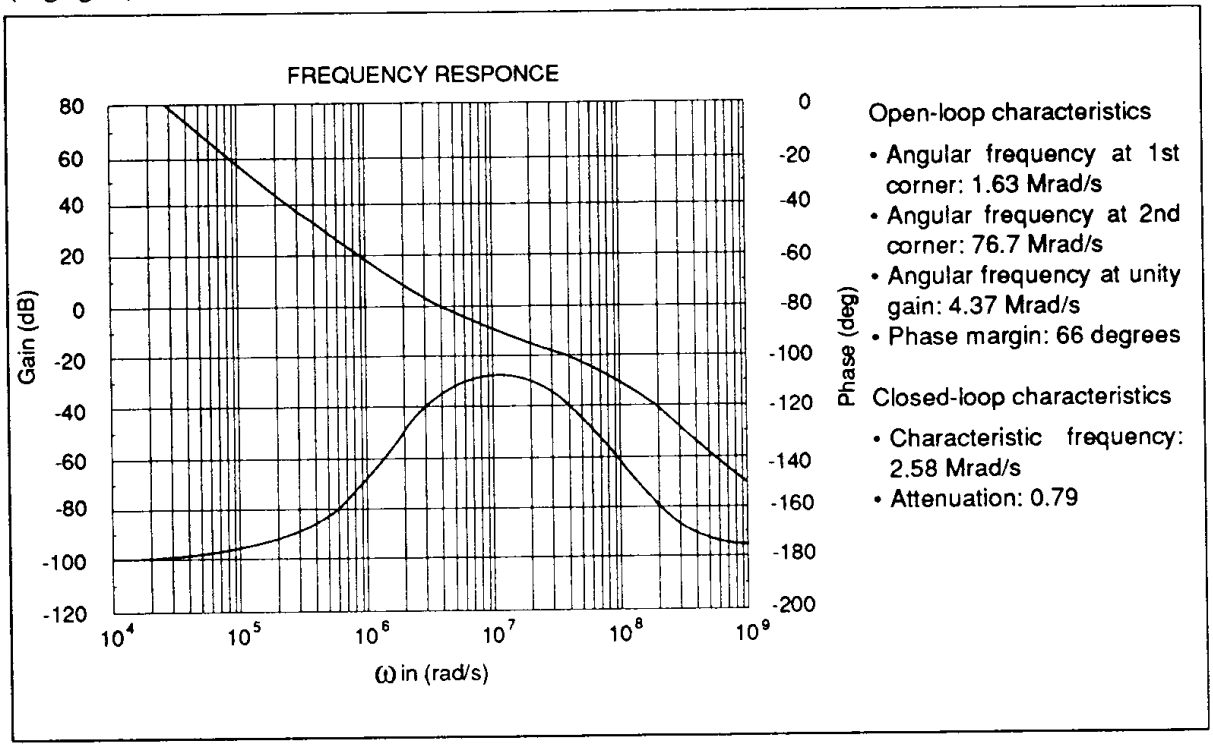
Closed-loop characteristics

- Characteristic frequency: 728 krad/s
- Attenuation: 1.00

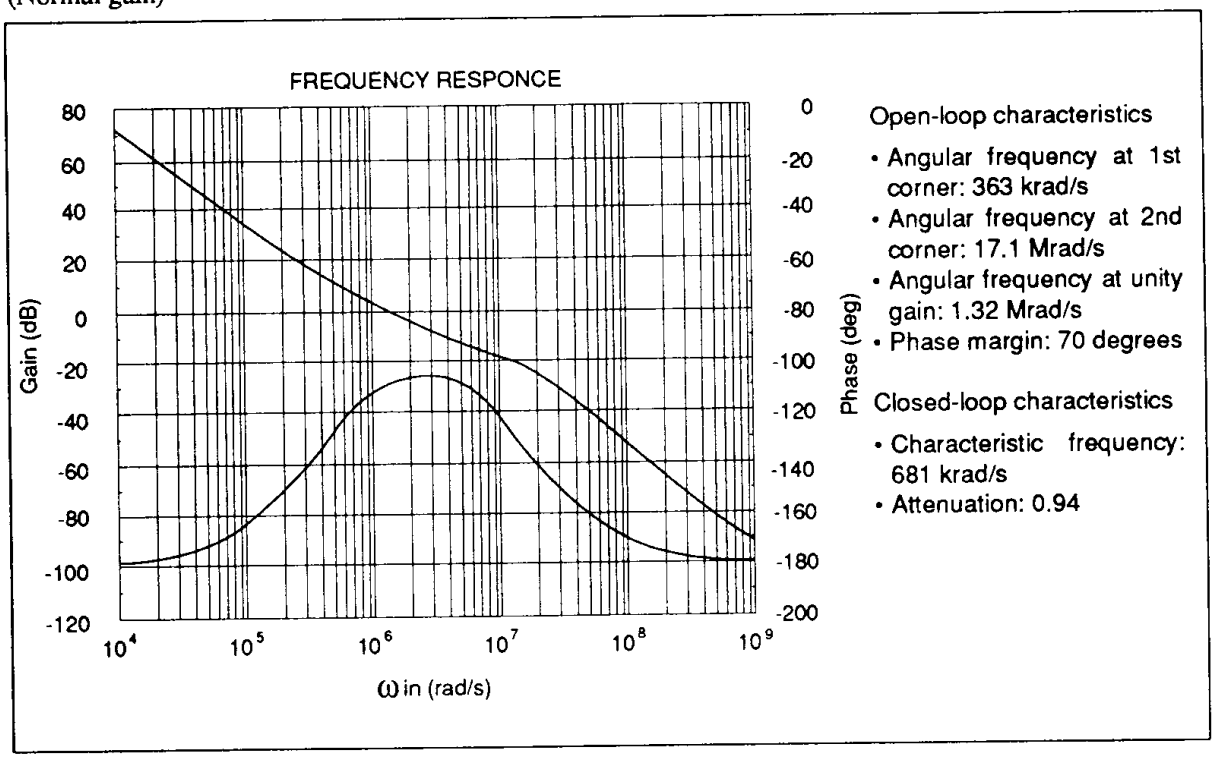
(12) OK at TRmin and TRmax?

TRmin, N = 32

(High gain)

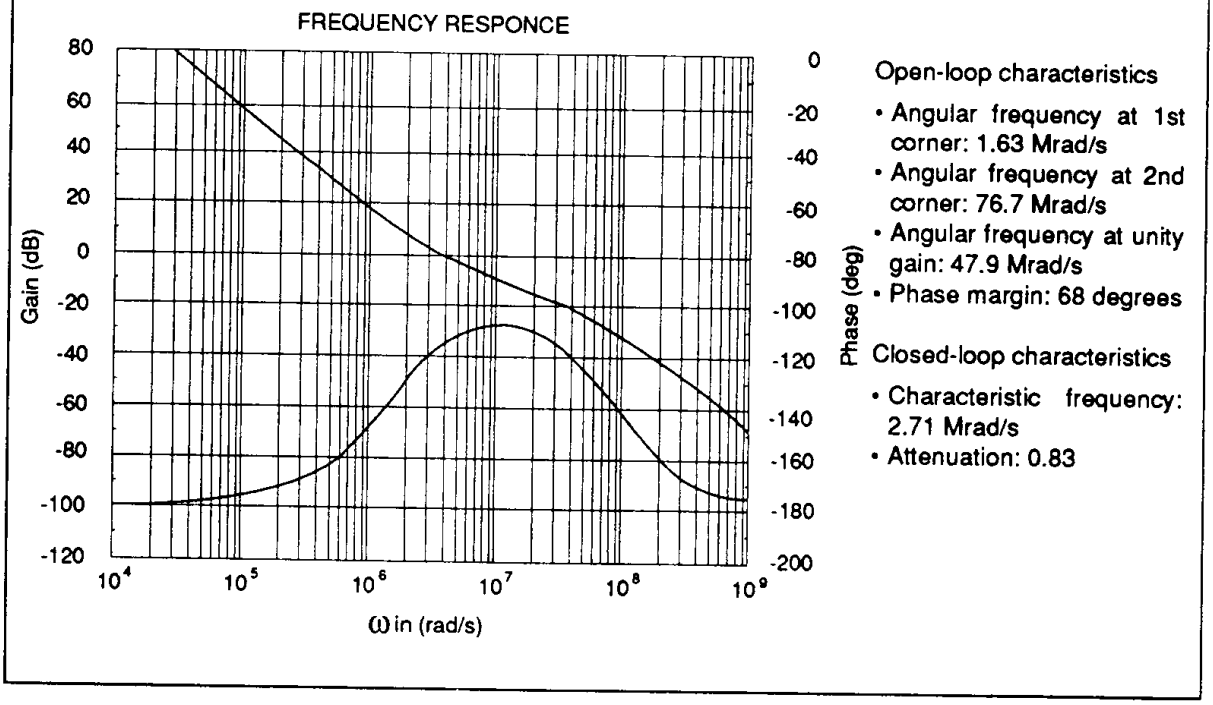


(Normal gain)

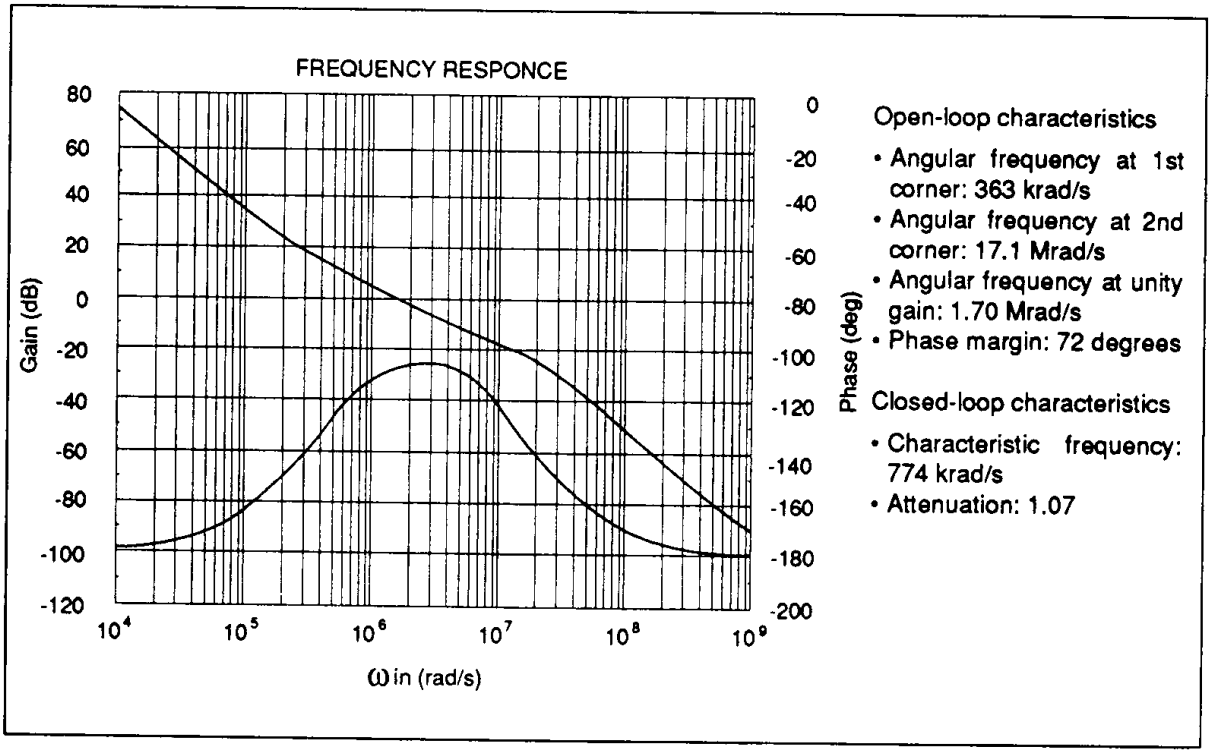


TRmax, N = 38

(High gain)



(Normal gain)



(13) Charge pump current I_{CR} in group II

The high-gain interval in this application is 6 bytes.

MDC Register

Bit	3	2
Value	0	0

The phase-lock acquisition time Taq is:

$$Taq = \frac{8}{28.750 \times 10^6} \times 6 = 1.7 \quad (\mu s)$$

The characteristic frequency ω_{nRH} is accordingly:

$$\omega_{nRH} = \frac{5.7}{1.7 \times 10^{-6}} = 3.4 \quad \left(\frac{Mrad}{s}\right)$$

Therefore:

$$3.4 \times 10^6 = \sqrt{\frac{126 \times 10^6 \times \left(\frac{I_{CR}}{6} + 27.3 \times 10^{-6}\right)}{3.14 \times 1800 \times 10^{-12}}}$$

$$I_{CR} = 2.9 \quad (mA)$$

Hence:

$$R_{FC1} = \frac{3.0}{2.9 \times 10^{-3}} = 1.0 \quad (k\Omega)$$

(14) T/I converter output current I_{TR} in group I

$$A_G = 14$$

Therefore:

$$I_{TR} = \frac{3 \times 10^{-3}}{6 \times (14 - 1)} = 38.5 \quad (\mu A)$$

Substituting this value into equation (II.5):

$$38.5 \times 10^{-6} = 1.5625 \times 10^{-3} \times \frac{46 \times L}{12 \times 10^3}$$

$$L = 7$$

Which gives I_{TR} as follows:

$$I_{TR} = 1.5625 \times 10^{-3} \times \frac{46 \times 7}{12 \times 10^3} = 41.9 \quad (\mu A)$$

(15) Filter resistances R_{F0} and R_{F1}

First calculate the high-gain and normal-gain characteristic frequencies:

$$\omega_{nRH} = \sqrt{\frac{126 \times 10^6 \times \left(\frac{3 \times 10^{-3}}{6} + 41.9 \times 10^{-6}\right)}{3.14 \times 1800 \times 10^{-12}}} = 3.48 \quad \left(\frac{Mrad}{s}\right)$$

$$\omega_{n\,RN} = \sqrt{\frac{126 \times 10^6 \times 41.9 \times 10^{-6}}{3.14 \times 1800 \times 10^{-12}}} = 966 \quad \left(\frac{krad}{s}\right)$$

Then:

$$1.0 = \frac{1839 \times 10^{-12}}{2} \times R_{F0} \times 966 \times 10^3$$

$$R_{F0} = 1.1 \quad (k\Omega)$$

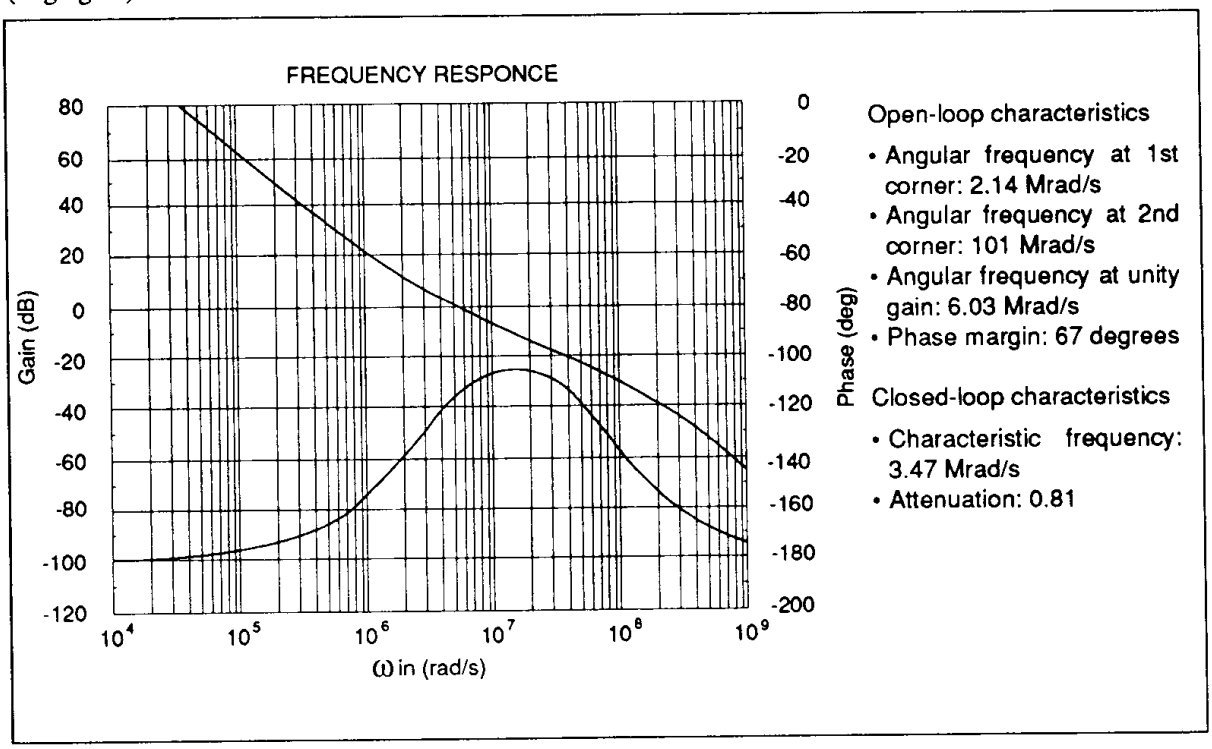
$$0.8 = \frac{1839 \times 10^{-12}}{2} \times \frac{1}{\frac{1}{1.1 \times 10^3} + \frac{1}{R_{F1}}} \times 3.48 \times 10^6$$

$$R_{F1} = 330 \quad (\Omega)$$

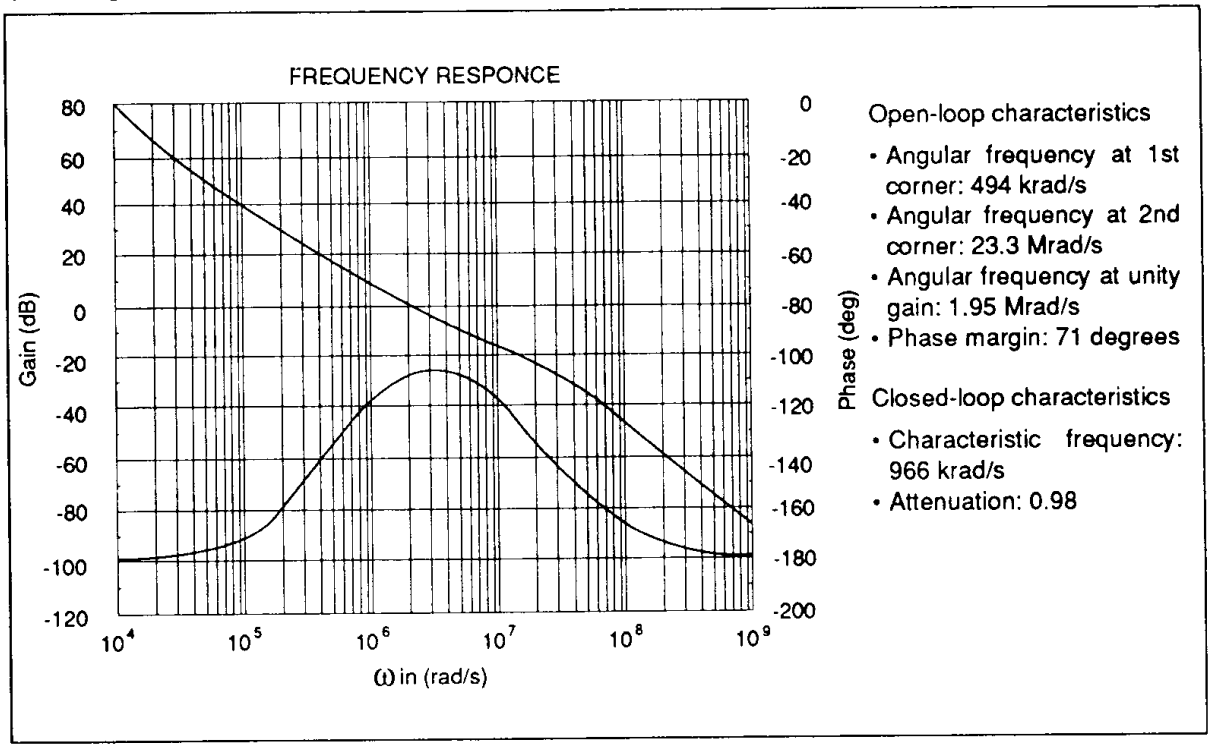
(16), (17) Bode plot

N = 46

(High gain)



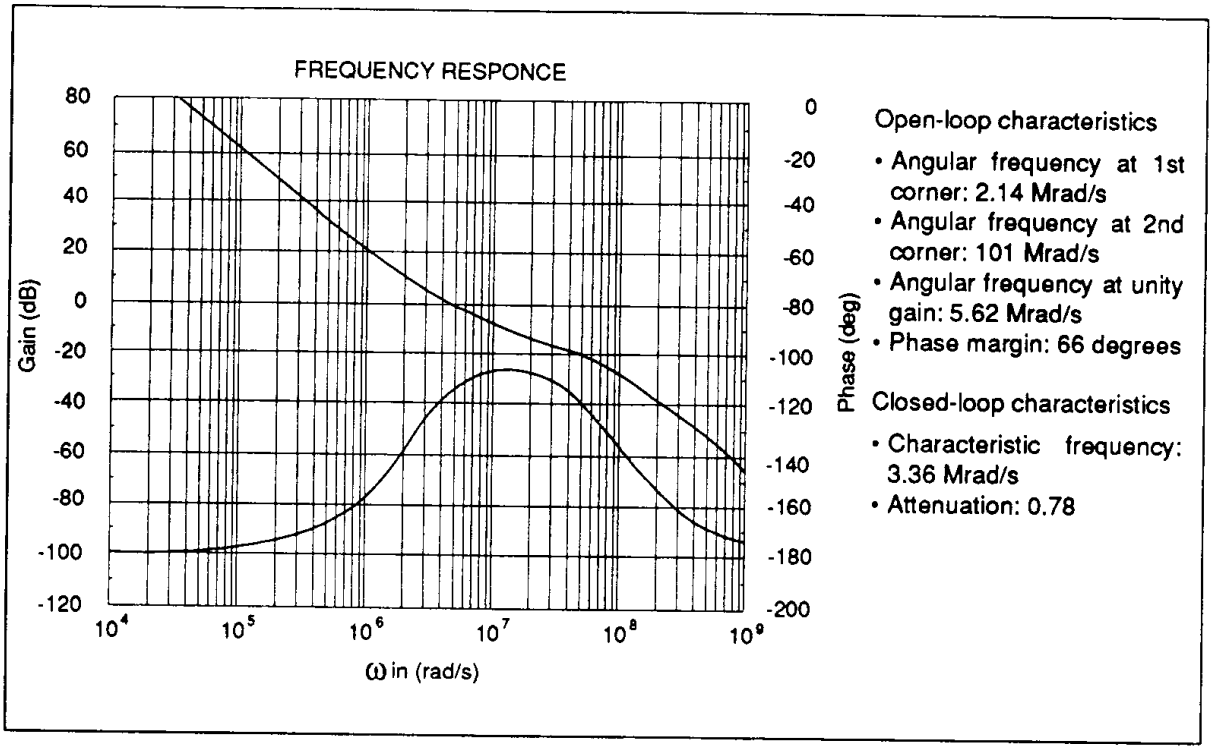
(Normal gain)



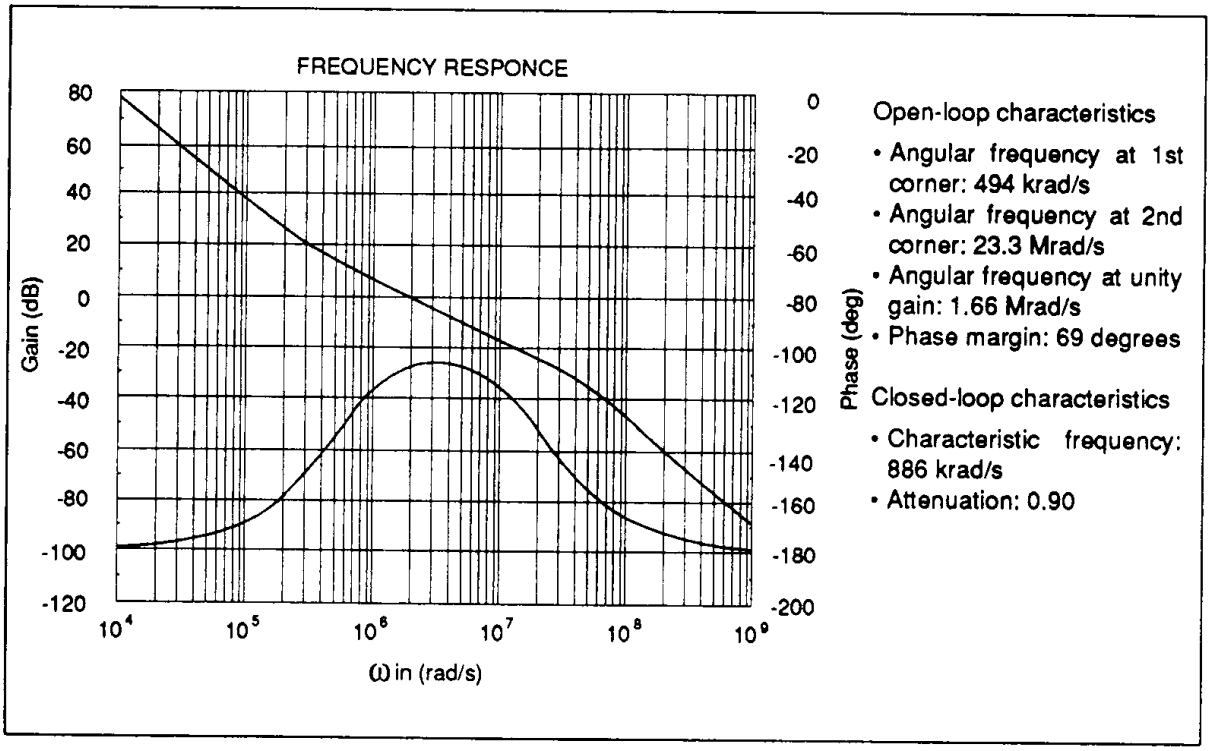
(18) OK at TRmin and TRmax?

TRmin, N = 41

(High gain)

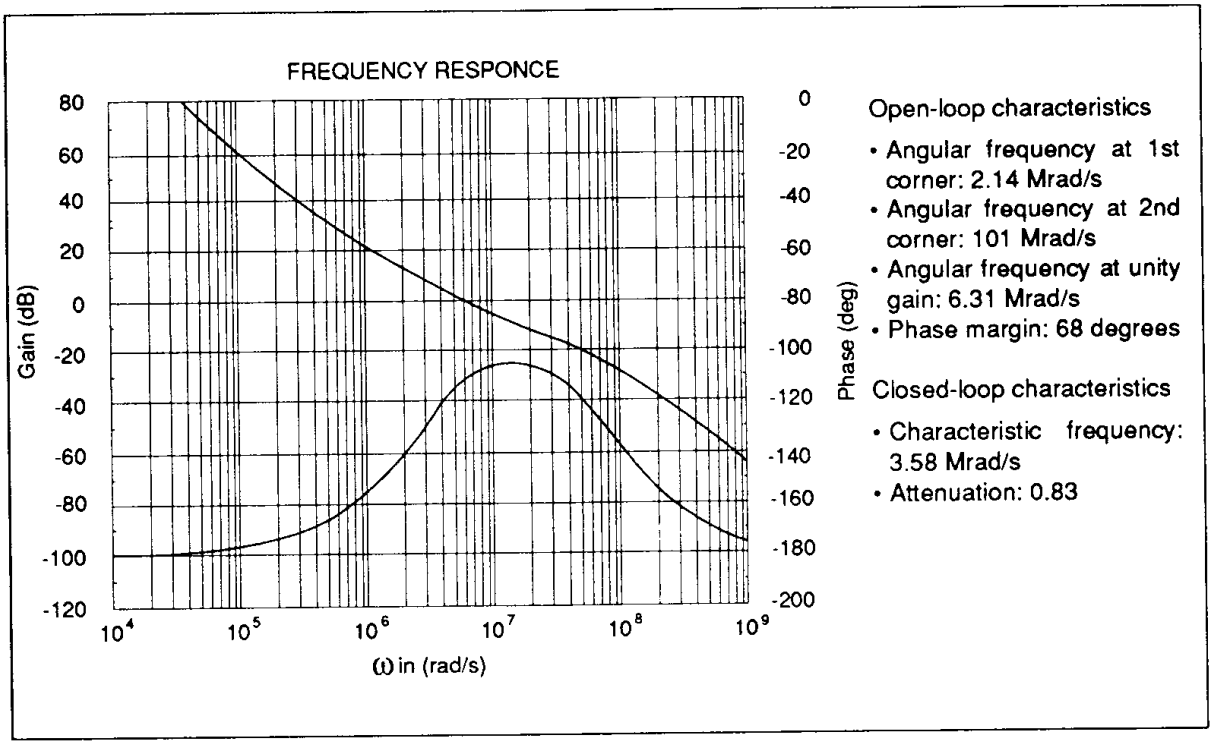


(Normal gain)

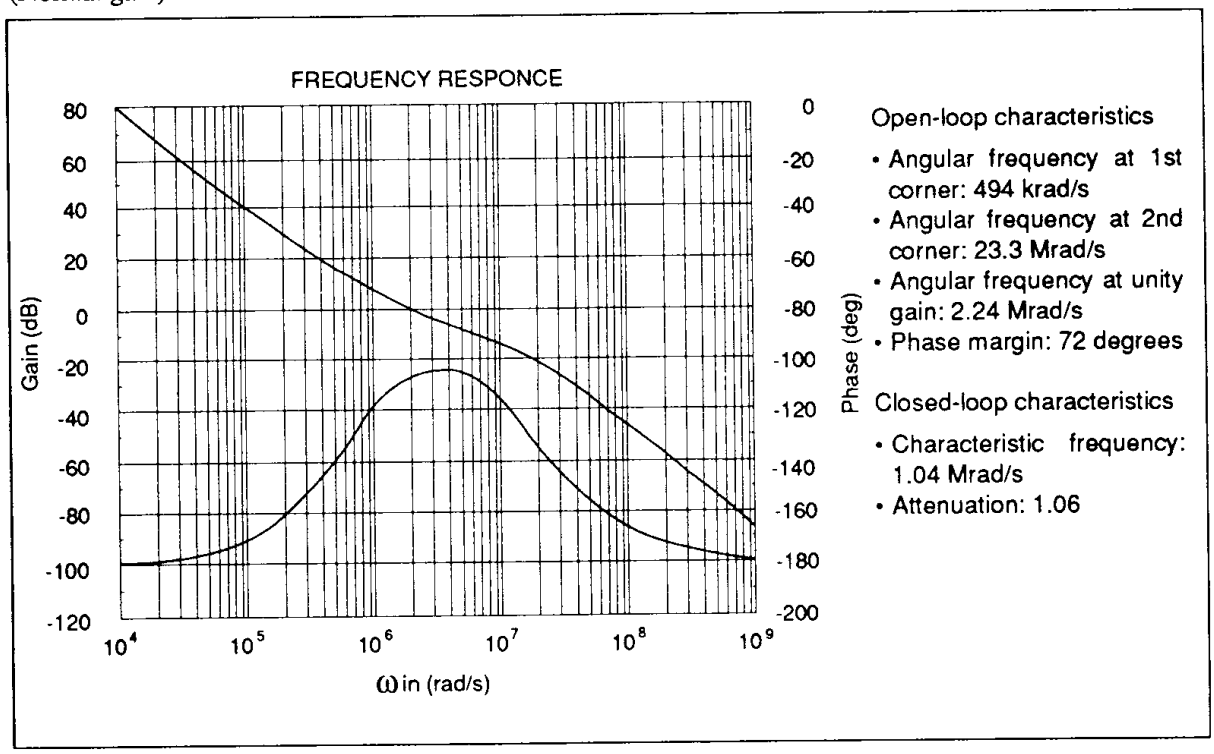


TRmax, N = 51

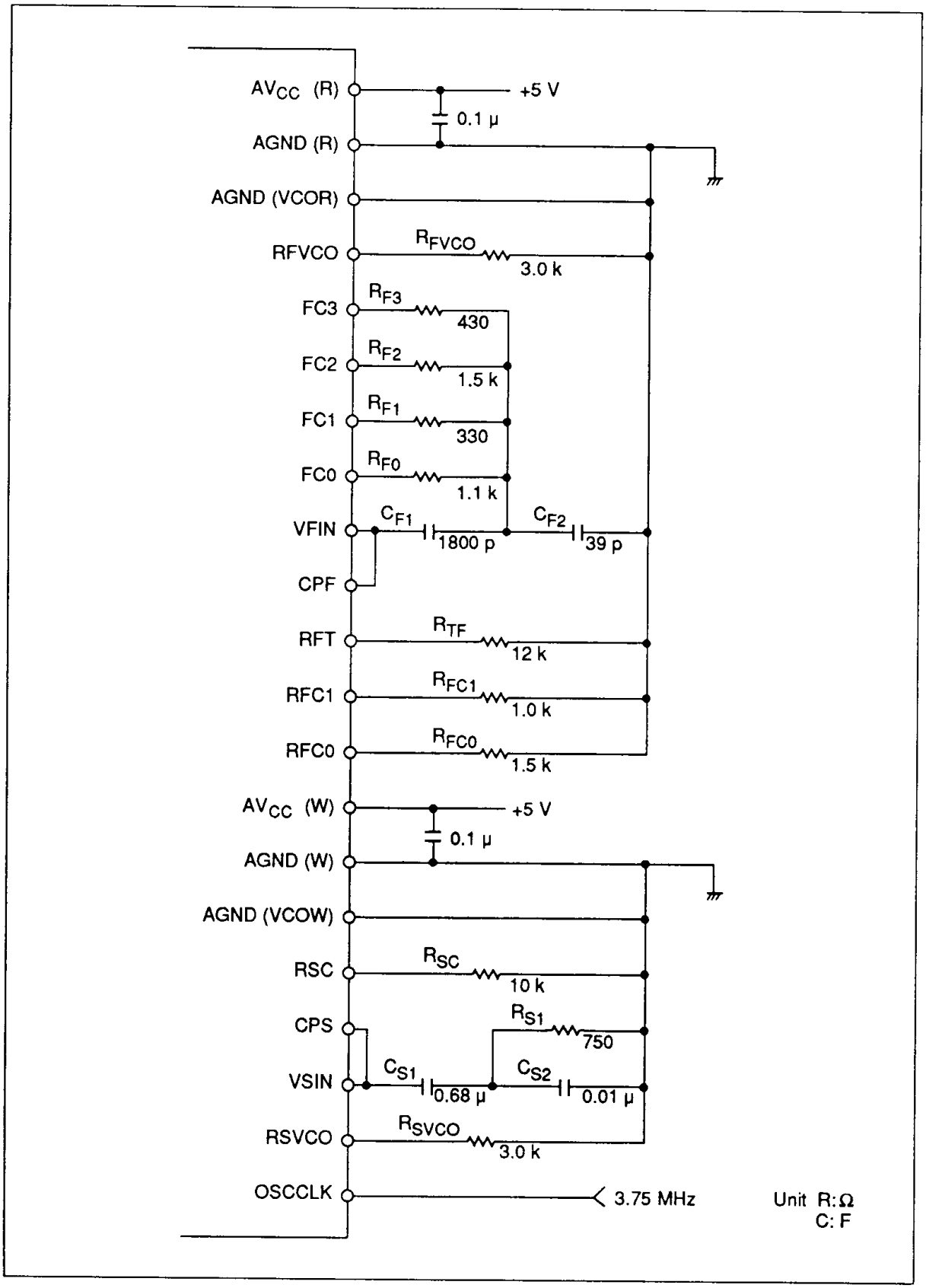
(High gain)



(Normal gain)



Example of External Components Connected to PLL



Absolute Maximum Ratings (Type QFP-80A, Ta = 25°C)

Description	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	7	V	DV_{CC1}, $AV_{CC(R)}$ DV_{CC2}, $AV_{CC(W)}$
Input voltage	V_I	5.5	V	*1
Output voltage	V_O	5.5	V	*2
Allowable loss	P_T			
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes: 1. RG, AME, $\overline{STBY}$, WCLK, $\overline{RESET}$, NRZWD, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$, D0, D1, D2, D3, D4, A0, A1, A2, OSCCLK, WG
2. $\overline{DLYRD}$, $\overline{SYNCRD}$, $\overline{DLYCLK}$, RRCLK, NRZWD, D0, D1, D2, D3, D4, CLKOUT, 1-7WD, $\overline{ULD}$, $\overline{AMF}$

Electrical Characteristics (Ta = 25°C)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Supply Voltage	V_{CC}	4.75	5.00	5.25	V		DV_{CC1}, FV_{CC}, DV_{CC2}, SV_{CC}
Input voltage	V_{IH}	2.0	—	—	V		*1
		4.0	—	4.2			*1'
	V_{IL}	—	—	0.8	V		*1
		3.4	—	3.6			*1'
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	*1
	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V, V_I = 0.4 V	*1
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} = –400 µA	*2
	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA	*2
Output short-circuit current	I_{OS}	–20	—	–120	mA	V_{CC} = 5.25 V	*2
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	*1

Electrical Characteristics (Ta = 25°C) (cont)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Off-state output current	I_{OZH}	—	—	20	µA		NRZRD
	I_{OZL}	—	—	–20	µA		NRZRD
Current consumption	I_{CC}	—	90	120	mA	V_{CC} = 5.25 V, with recommended constants for 20 Mbps	DV_{CC1}, FV_{CC}, DV_{CC2}, SV_{CC}
Write charge pump output current	I_{CIW}	–90	–100	–110	µA	V_{CC} = 5.0 V, RSC = 30 k, V_{CPS} = 2.5 V	CPS
	I_{CDW}	90	100	110	µA		
Read charge pump output current	I_{CIR}	–1.8	–2.0	–2.2	mA	V_{CC} = 5.0 V, V_{CPF} = 2.5 V, RFC0 = 1.5 k, GAC reg. bit 3 = 0	CPF
	I_{CDR}	1.8	2.0	2.2	mA		
	I_{CIR}	–3.0	–3.3	–3.6	mA	V_{CC} = 5.0 V, V_{CPF} = 2.5 V, RFC1 = 910, GAC reg. bit 3 = 1	CPF
	I_{CDR}	3.0	3.3	3.6	mA		
T/I converter output current	I_{TI}	—	10.4	—	µA	*3	CPF
	I_{TO}	—	0	—	µA	*4	
T/I converter output current	I_{TD}	—	–10.4	—	µA	*5	CPF
Standby current	I_{SB}	—	2.5	4.0	mA	$\overline{STBY}$ = 0	DV_{CC1}, DV_{CC2}, $AV_{CC(R)}$, $AV_{CC(W)}$

Notes:
1. RG, AME, $\overline{STBY}$, WCLK, $\overline{RESET}$, NRZWD, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$, D0, D1, D2, D3, D4, A0, A1, A2, OSCCLK, WG
1'. RAWRD (ECL input)
2. $\overline{DLYRD}$, $\overline{SYNCRD}$, $\overline{DLYCLK}$, RRCLK, NRZWD, D0, D1, D2, D3, D4, CLKOUT, 1-7WD, $\overline{ULD}$, $\overline{AMF}$
3. V_{CC} = 5.0 V, V_{CPF} = 2.5 V, RFT = 12 k, GAC register bits 2 to 0 = 100, VFC register bits 4 to 0 = 00000, phase offset π/2 (rad)
4. V_{CC} = 5.0 V, V_{CPF} = 2.5 V, RFT = 12 k, GAC register bits 2 to 0 = 100, VFC register bits 4 to 0 = 00000, phase offset 0 (rad)
5. V_{CC} = 5.0 V, V_{CPF} = 2.5 V, RFT = 12 k, GAC register bits 2 to 0 = 100, VFC register bits 4 to 0 = 00000, phase offset –π/2 (rad)

Electrical Characteristics (Ta = 25°C)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Reset time	t_{RS}	50	—	—	ns		$\overline{\text{RESET}}$
NRZ read data setup time	t_{SNR}	10	—	—	ns	32 Mbps, duty adjusted	NRZRD
		5	—	—	ns	32 Mbps,non-adjusted	
NRZ read data hold time	t_{HNR}	10	—	—	ns	32 Mbps, duty adkisted	
		10	—	—	ns	32 Mbps non-adjusted	
Read data input pulse width	t_W	10.4	20.8	31.2	ns	32 Mbps	RAWRD
Decode time	t_{DD}	—	10	—	DCLK		NRZRD
NRZ write data setup time	t_{SNW}	5	—	—	ns		NRZWD
NRZ write data hold time	t_{HNW}	5	—	—	ns		NRZWD
Encode time	t_{ED}	—	13	—	ECLK	With write precompensation	1-7 WD
		—	17	—	ECLK	Without write precompensation	
1-7 Write data setup time	t_{SCW}	5	—	—	ns	32 Mbps	1-7 WD
1-7 Write data hold time	t_{HCW}	5	—	—	ns	32 Mbps	1-7 WD
Reference clock to read clock switch time	t_{RER}	—	—	53 77 101	RAWRD Pulse	32 Mbps	RRCLK
Read clock to reference clock switch time	t_{RRE}	—	—	5	ECLK		RRCLK
Address mark write time	t_{AMW}	1	—	40	ECLK		AME
Address mark write enable time	t_{AML}	—	—	—			1-7 WD
Address mark detect disable time	t_{AFL}	—	—	20	ns		$\overline{\text{AMF}}$
Address mark length	t_{AM}	—	40	—	ECLK		1-7 WD

ECLK: encode clock
DCLK: decode clock

Electrical Characteristics (Ta = 25°C) (cont)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Write precompensation delay A to B	t_{AB}	—	0	—	ns	Min. delay setting	1-7 WD
		—	10.5	—	ns	Max. delay setting	
Write precompensation delay B to C	t_{BC}	—	0	—	ns	Min. delay setting	1-7 WD
		—	10.5	—	ns	Max. delay setting	
Write precompensation delay C to D	t_{CD}	—	0	—	ns	Min. delay setting	1-7 WD
		—	10.5	—	ns	Max. delay setting	
Duty cycle of read and reference clocks		45	—	55	%	32 Mbps, adjusted	RRCLK
		—	66.7	—	%	32 Mbps, non-adjusted	
Duty cycle of oscillator clock input		30	—	70	%	32 Mbps, adjusted	OSCCLK
		45	—	55	%	32 Mbps, non-adjusted	
Standby recovery time		10	—	—	ms		$\overline{STBY}$
Data transfer rate		10	—	32	Mbps		
Register write cycle	t_{WC}	50	—	—	ns		A0 to 2
Address setup time	t_{AS}	40	—	—	ns		A0 to 2
Address hold time	t_{AH}	0	—	—	ns		A0 to 2
Write chip select time	t_{CW}	40	—	—	ns		$\overline{CS}$
Write enable time	t_{WW}	40	—	—	ns		$\overline{WE}$
Register data setup time	t_{DS}	20	—	—	ns		D0 to 4
Register data hold time	t_{DH}	0	—	—	ns		D0 to 4
Register read cycle	t_{RC}	50	—	—	ns		A0 to 2
Address access time	t_{AA}	—	—	50	ns		D0 to 4
Read chip select time	t_{CR}	40	—	—	ns		$\overline{CS}$
Read enable time	t_{RR}	40	—	—	ns		$\overline{RE}$
Read enable delay	t_{RE}	0	—	40	ns		$\overline{RE}$

Electrical Characteristics (Ta = 25°C) (cont)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Read disable delay	t_{RD}	5	—	20	ns		$\overline{RE}$
Read chip select disable delay	t_{CD}	5	—	20	ns		$\overline{CS}$
Register output hold time	t_{RH}	0	—	20	ns		A0 to 2
Max. frequency of write VCO		70	—	—	MHz		
Center frequency of write VCO		28.5	30	31.5	MHz	V_{CC} = 5 V, RSVCO = 3 k	
Upper clamp frequency of write VCO		34.5	36	37.5	MHz	V_{CC} = 5 V, RSVCO = 3 k	
Lower clamp frequency of write VCO		22.5	24	25.5	MHz	V_{CC} = 5 V, RSVCO = 3 k	
VCO gain		43.2	54	64.8	Mrad/s•V	V_{CC} = 5 V, VFIN = 2.5 V, RSVCO = 3 k	
Max. frequency of read VCO		70	—	—	MHz		
Center frequency of read VCO		28.5	30	31.5	MHz	V_{CC} = 5 V, RFVCO = 3 k	
Upper clamp frequency of read VCO		37.5	39	40.5	MHz	V_{CC} = 5 V, RFVCO = 3 k	
Lower clamp frequency of read VCO		19.5	21	22.5	MHz	V_{CC} = 5 V, RFVCO = 3 k	
VCO gain		80	100	120	Mrad/s•V	V_{CC} = 5 V, VFIN = 2.5 V, RFVCO = 3 k	
Write phase-lock acquisition time		—	—	2.0	ms	20 Mbps, recommended constants	
Write capture range		±10	—	—	%	20 Mbps, recommended constants	
Write lock range		±10	—	—	%	20 Mbps, recommended constants	

Electrical Characteristics (Ta = 25°C) (cont)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Application terminal
Read phase-lock acquisition time		—	—	6	Byte	20 Mbps, recommended constants	
Read capture range		±15	—	—	%	20 Mbps, recommended constants	
Read lock range		±15	—	—	%	20 Mbps, recommended constants	
Read window margin loss		—	—	3.3	ns	20 Mbps, recommended constants	

Timing Charts

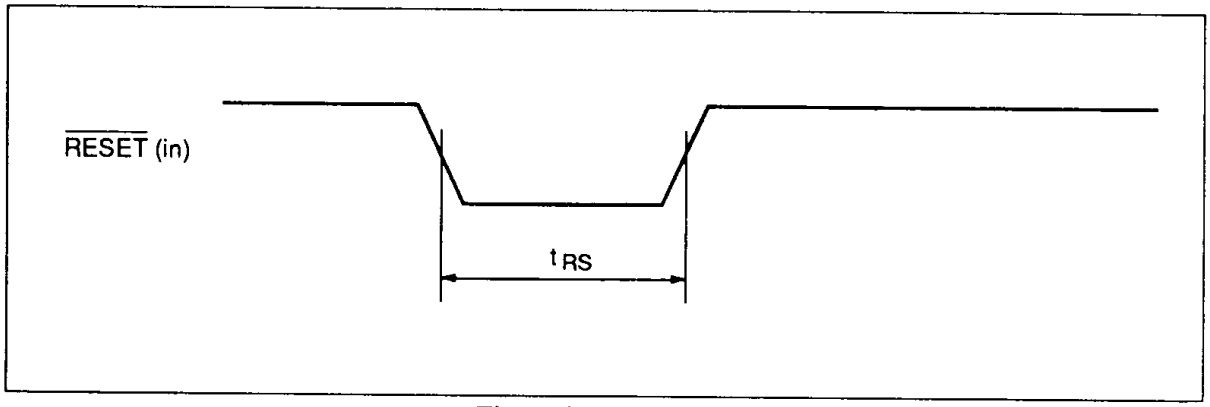


Figure 1 Reset Input

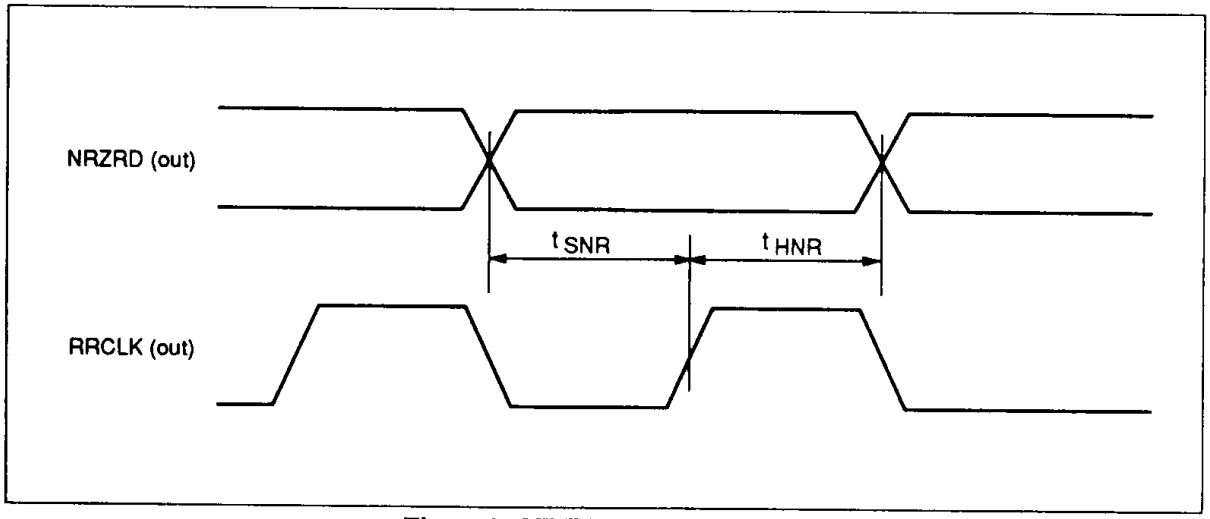


Figure 2 NRZ Read Data Output

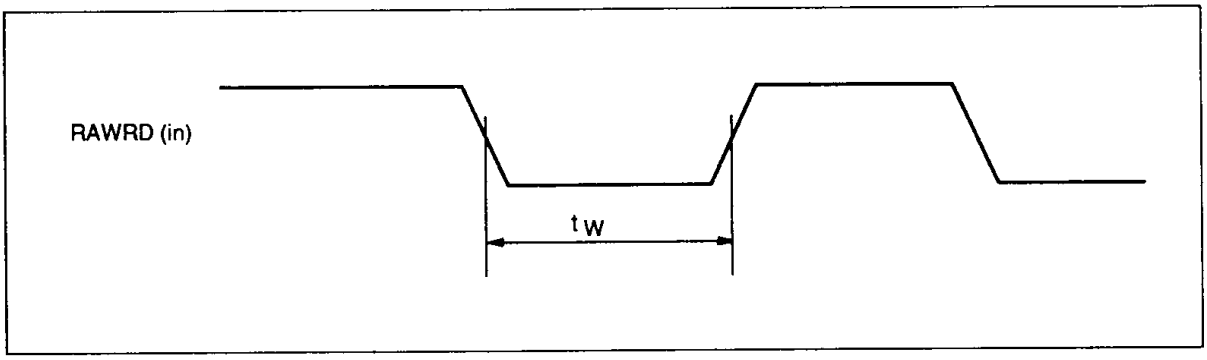


Figure 3 1-7 Code Read Data Input

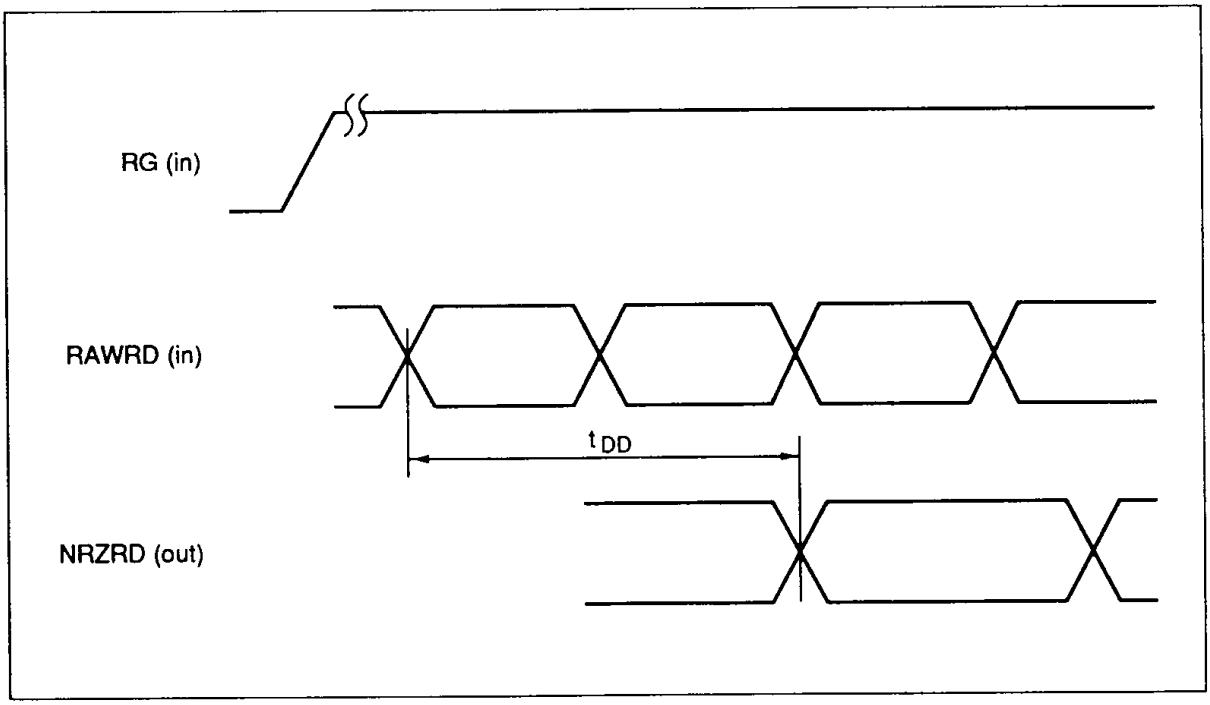


Figure 4 Decode

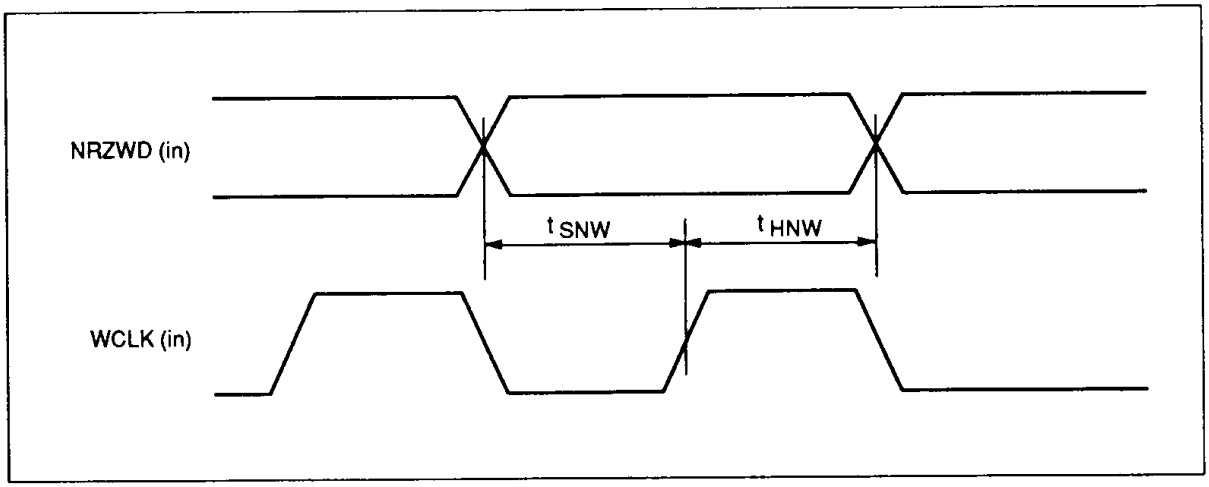


Figure 5 NRZ Write Data Input

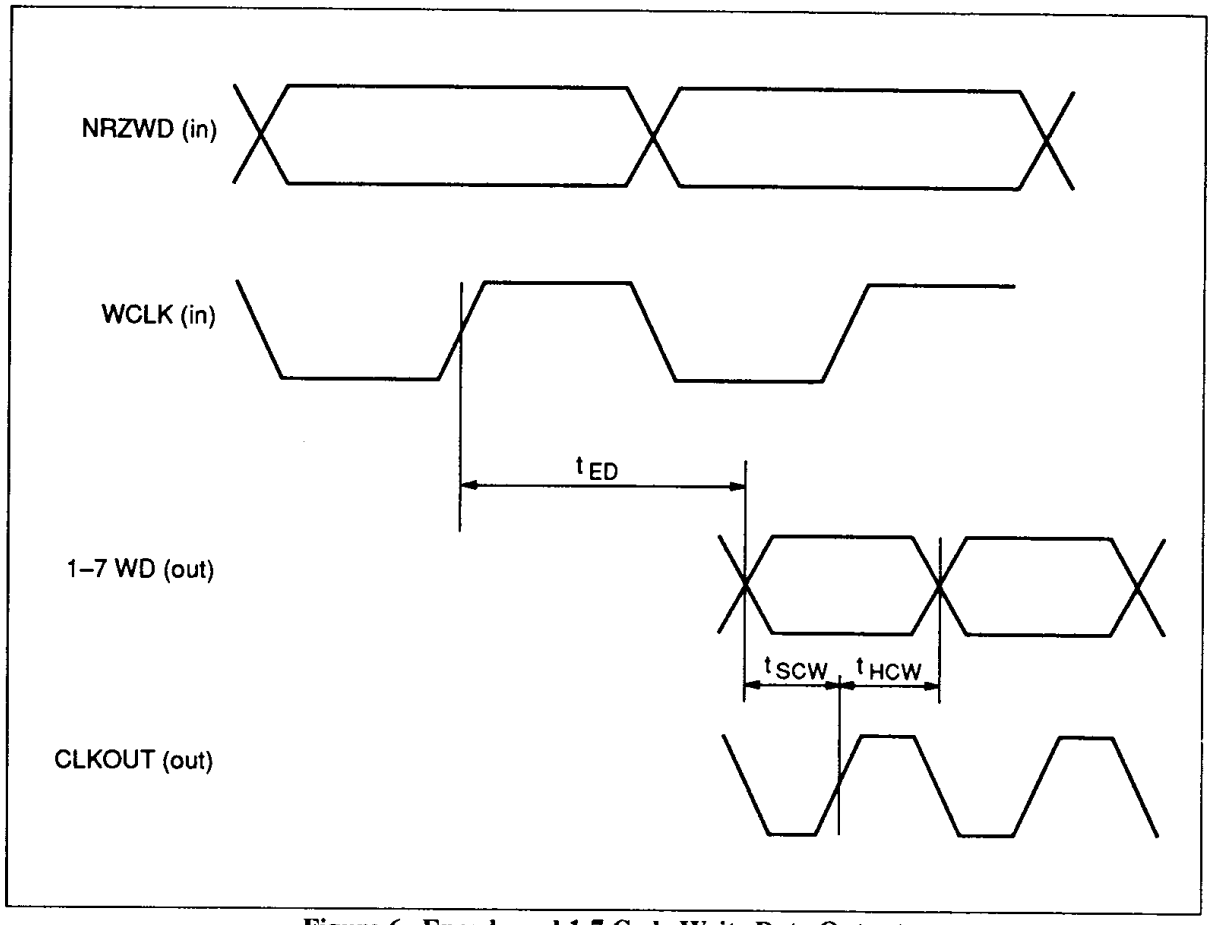


Figure 6 Encode and 1-7 Code Write Data Output

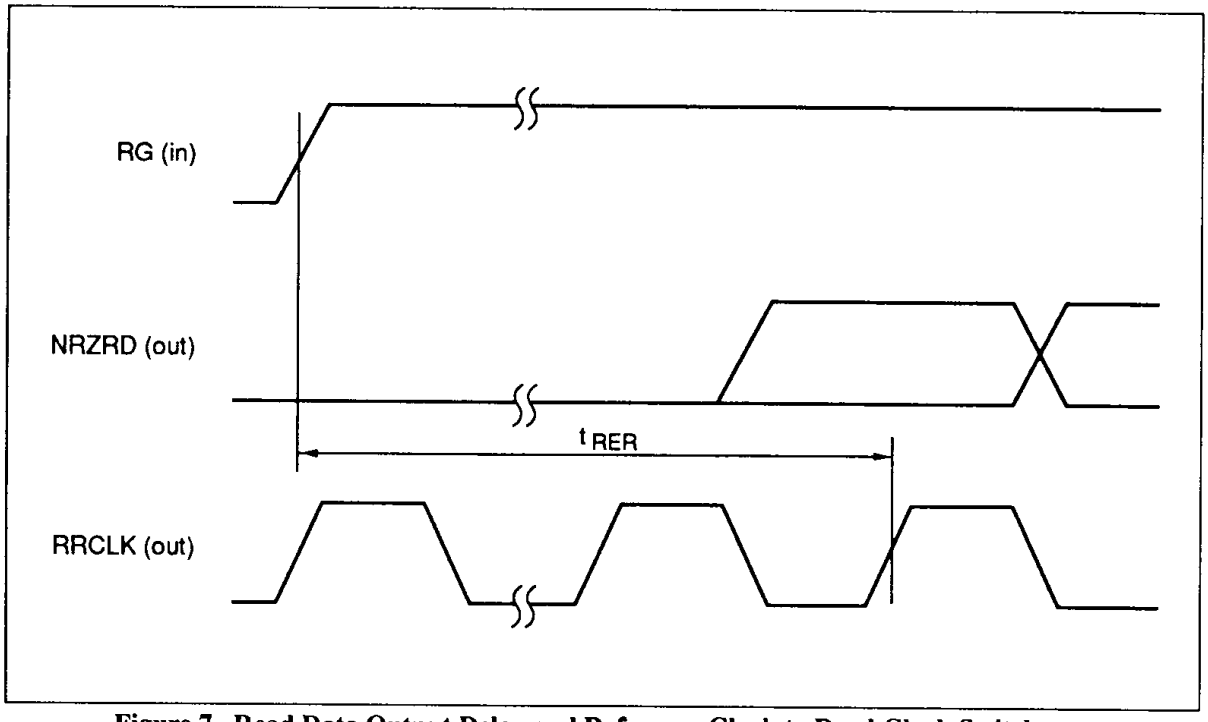


Figure 7 Read Data Output Delay and Reference Clock to Read Clock Switchover

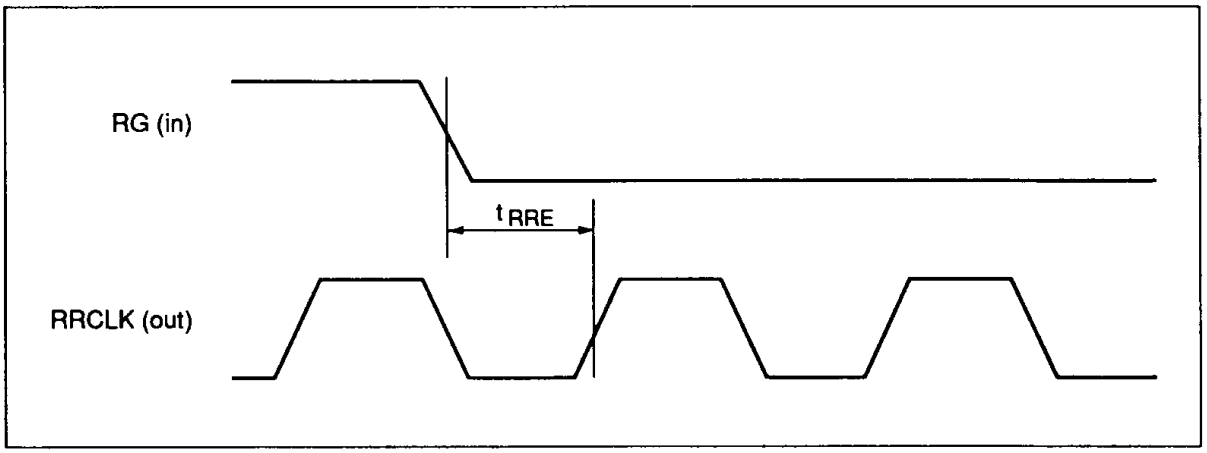


Figure 8 Read Clock to Reference Clock Switchover

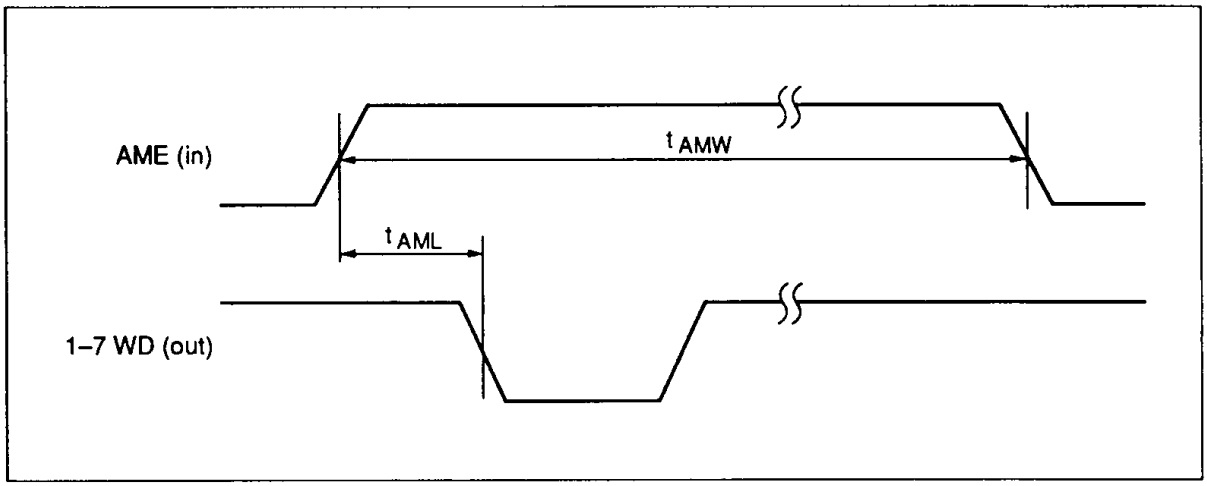


Figure 9 Address Mark Generation

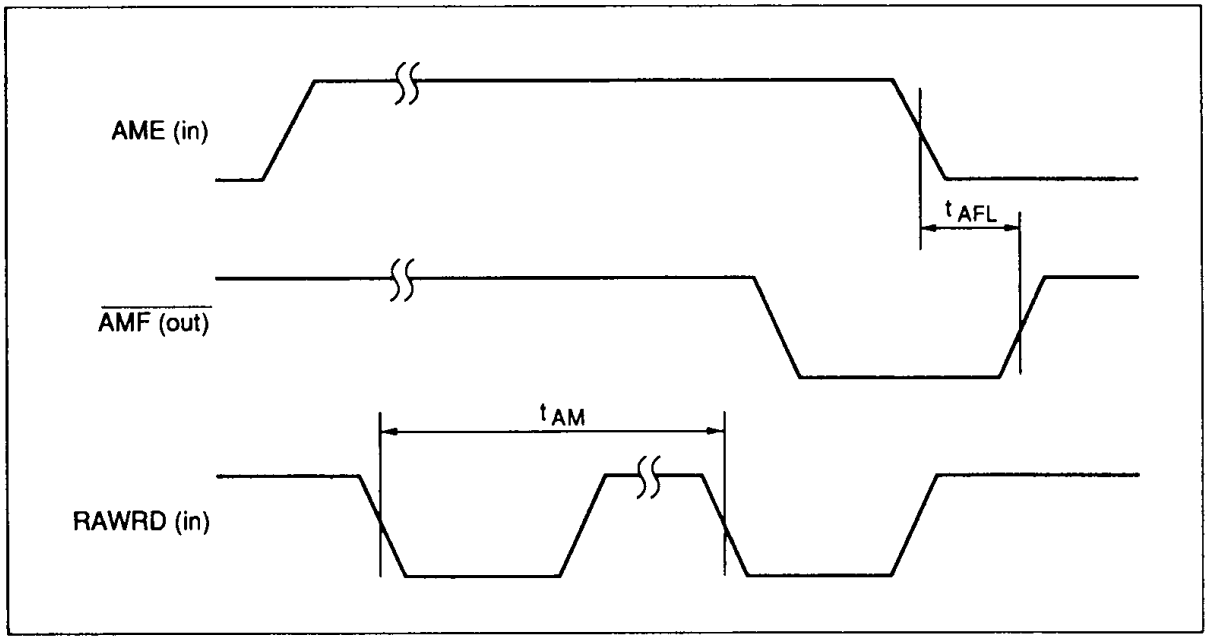


Figure 10 Address Mark Detection

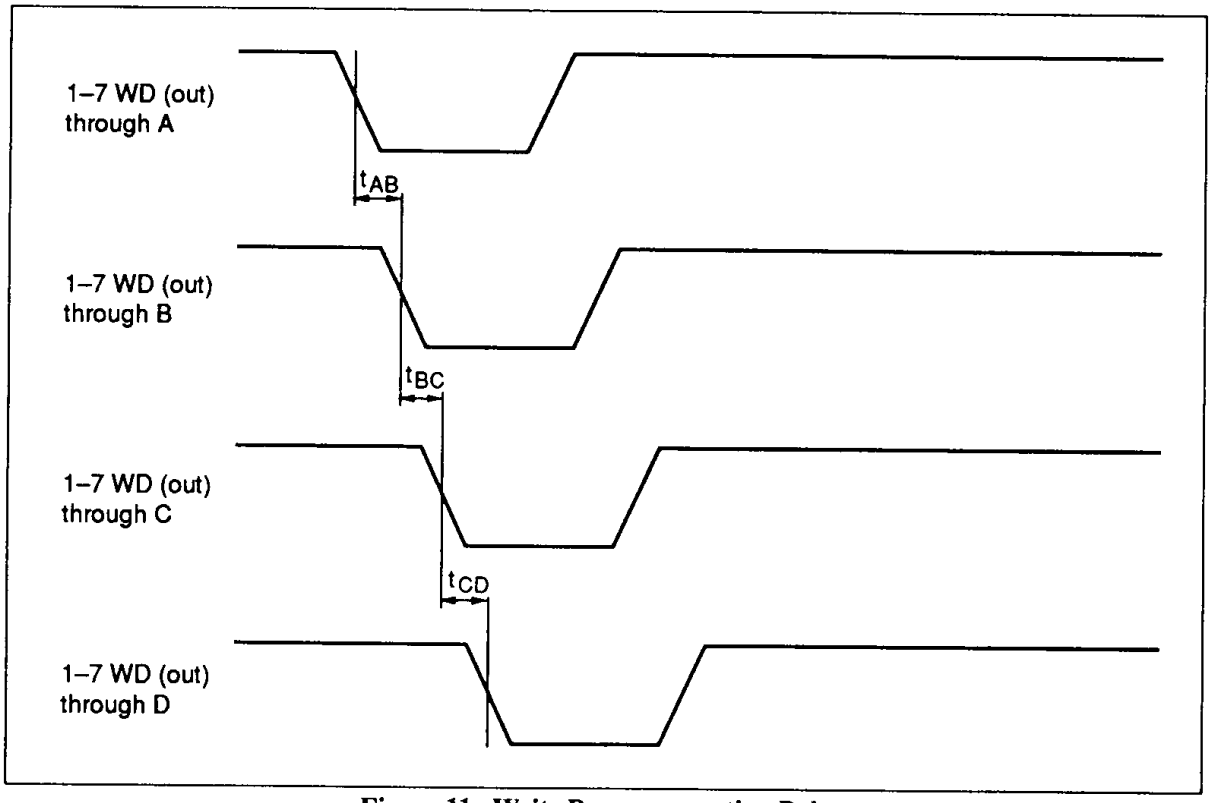


Figure 11 Write Precompensation Delay

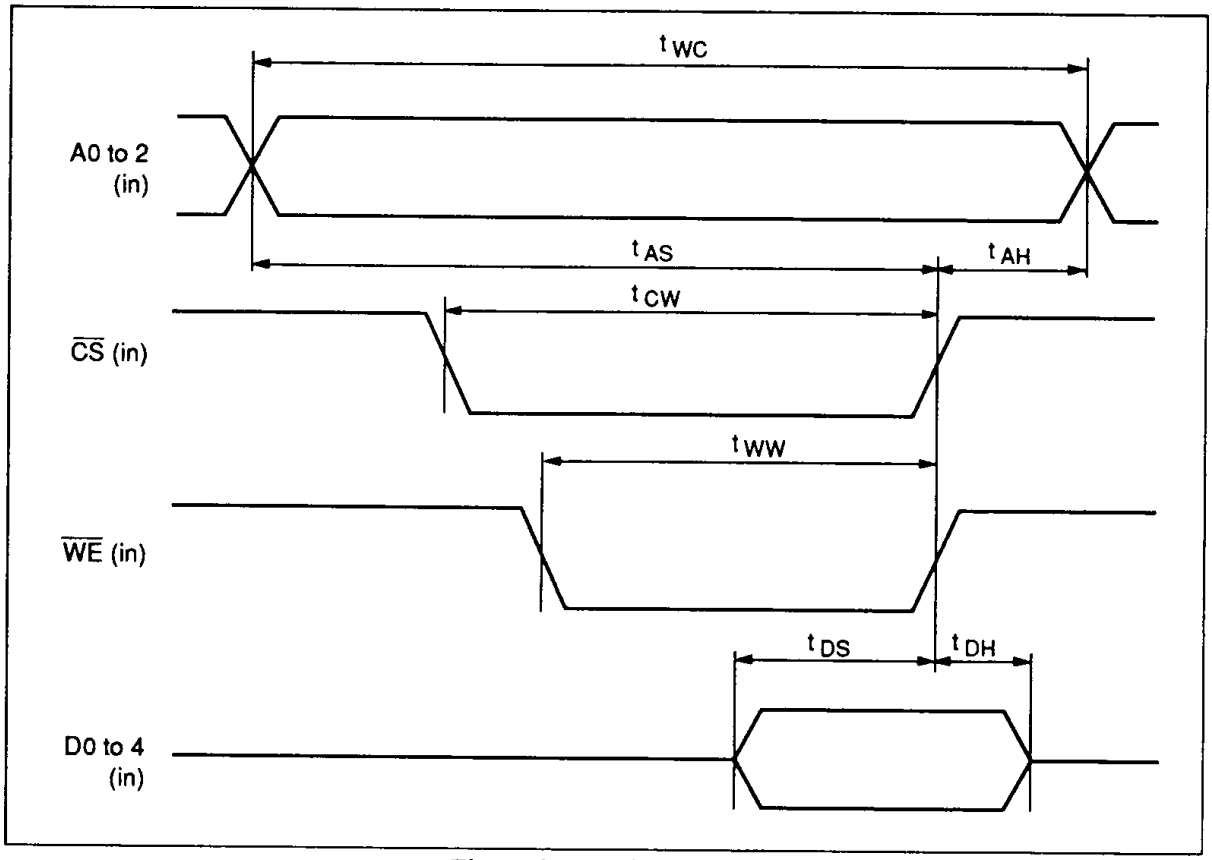


Figure 12 Register Write

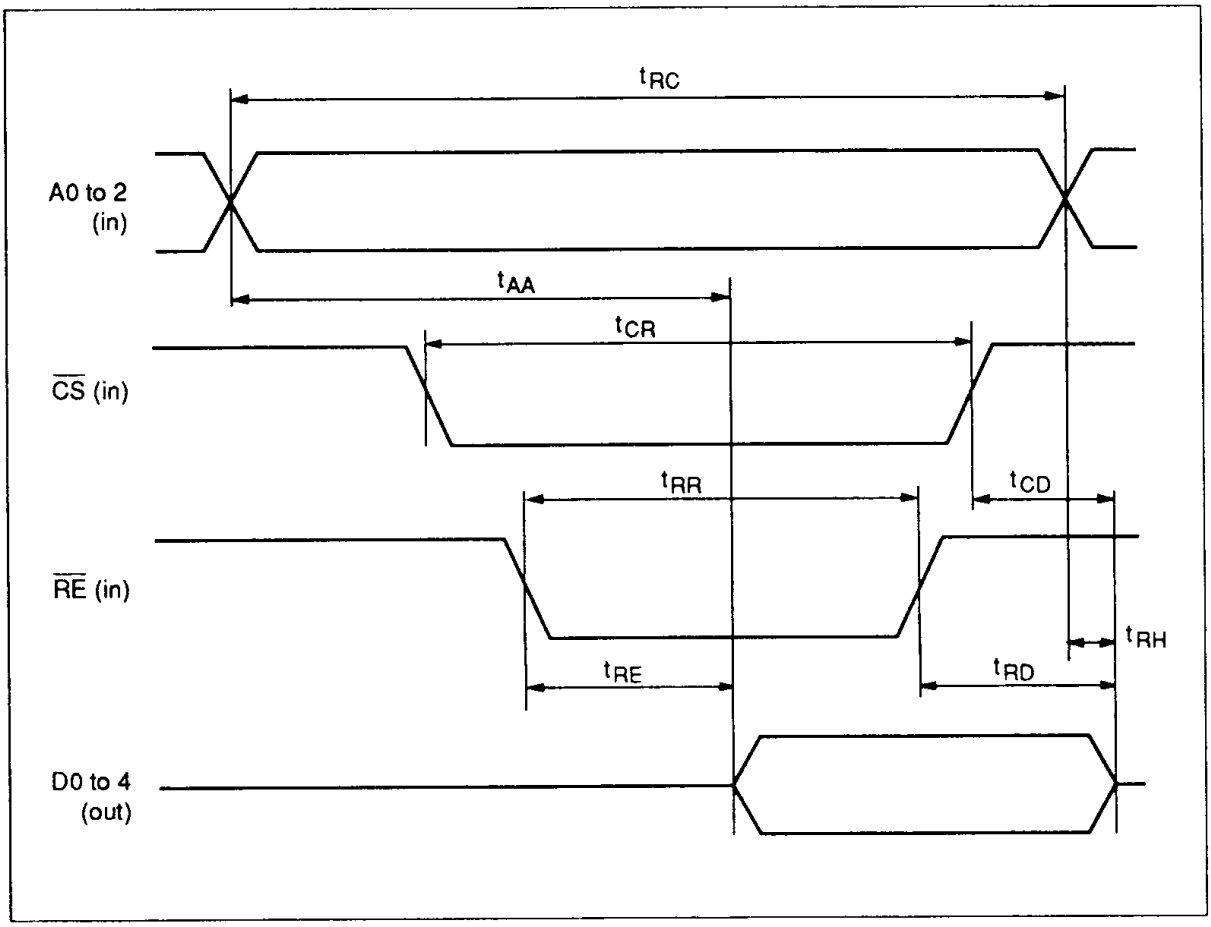
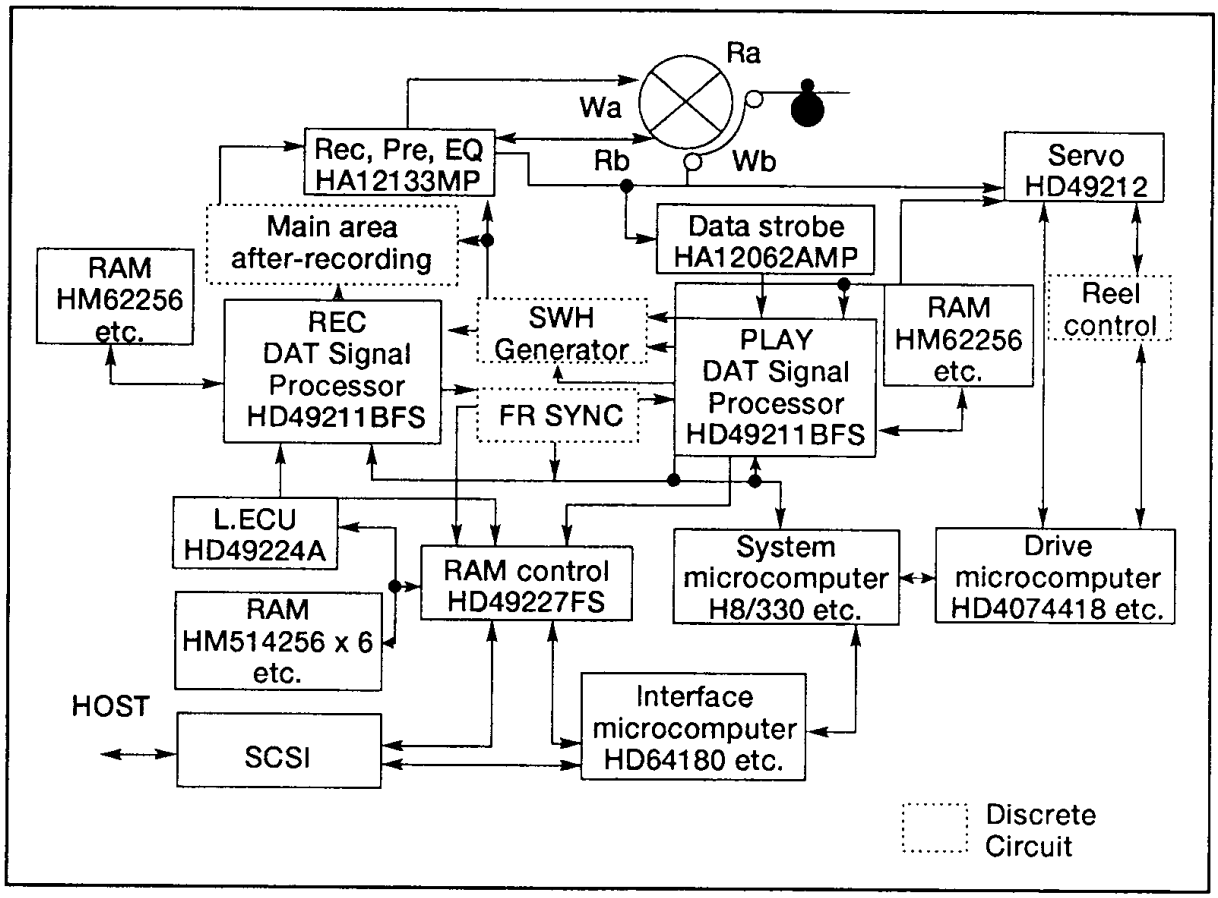


Figure 13 Register Read

DATA/DAT System Configuration



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