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# HD74AC165/HD74ACT165

## Parallel-Load 8-bit Shift Register

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### Description

This 8-bit serial shift register shifts data from  $Q_A$  to  $Q_H$  when clocked, Parallel inputs to each stage are enabled by a low level at the Shift/Load Input. Also included is a gated clock input and a complementary output from the eighth bit.

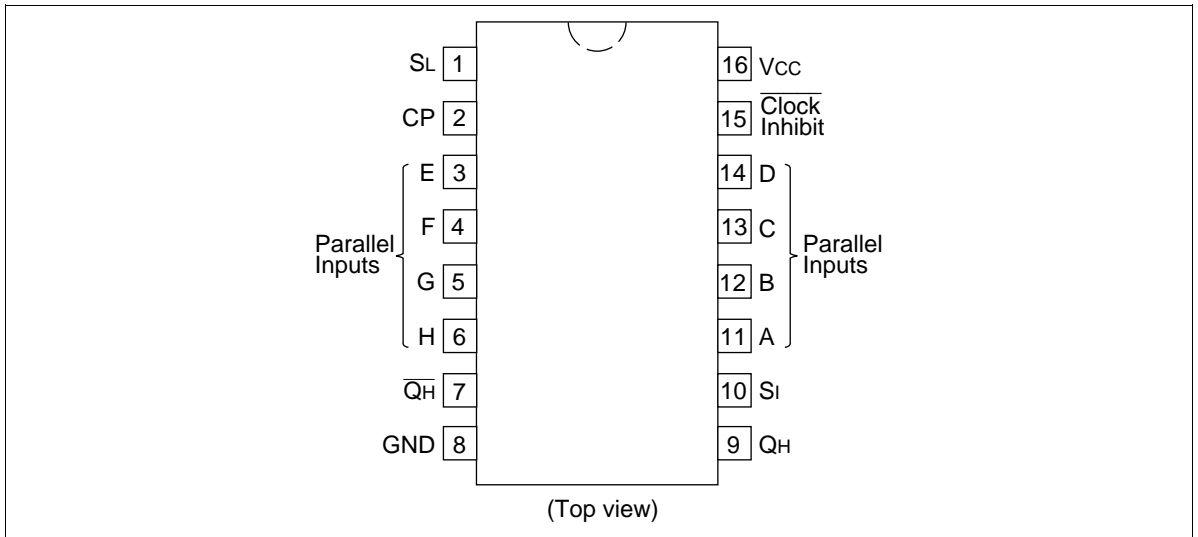
Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

### Features

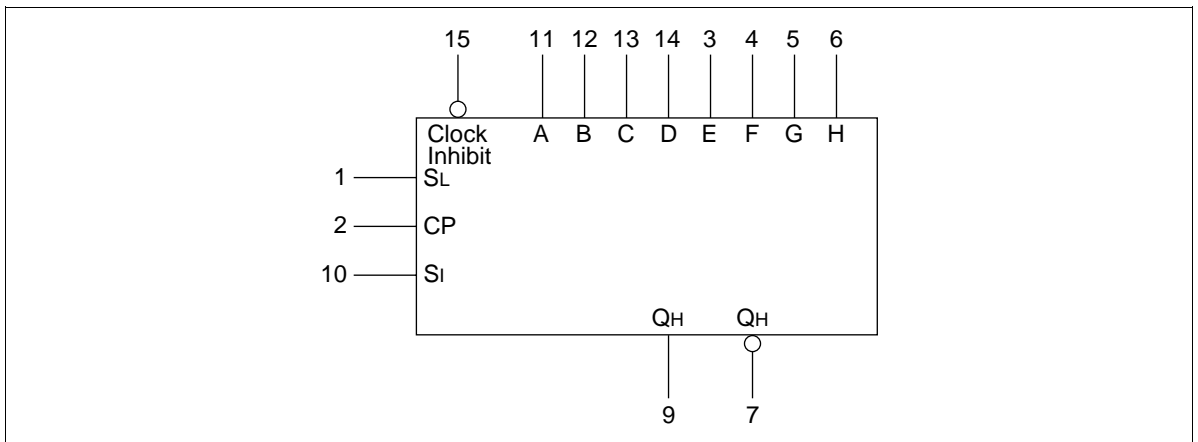
- Outputs Source/Sink 24 mA
- HD74ACT165 has TTL-Compatible Inputs

# HD74AC165/HD74ACT165

## Pin Arrangement



## Logic Symbol





## Pin Names

A to H	Parallel Inputs
$S_i$	Serial Input
CP	Clock Input
$S_L$	Shift Load
$\overline{\text{Clock Inhibit}}$	Clock Inhibit
$Q_H, \overline{Q}_H$	Outputs

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**Truth Table**


**Inputs**

$S_L$	$\overline{\text{Clock}}$		$S_I$	Parallel	Internal Outputs		Outputs
	Inhibit	CP		A ..... H	$Q_A$	$Q_B$	$Q_H$
L	X	X	X	a ..... h	a	b	h
H	L	L	X	X	$Q_{A\overline{D}}$	$Q_{B\overline{O}}$	$Q_{H\overline{O}}$
H	L		H	X	H	$Q_{An}$	$Q_{Gn}$
H	L		L	X	L	$Q_{An}$	$Q_{Cn}$
H	H	X	X	X	$Q_{A\overline{D}}$	$Q_{B\overline{O}}$	$Q_{H\overline{O}}$

H : High Voltage Level

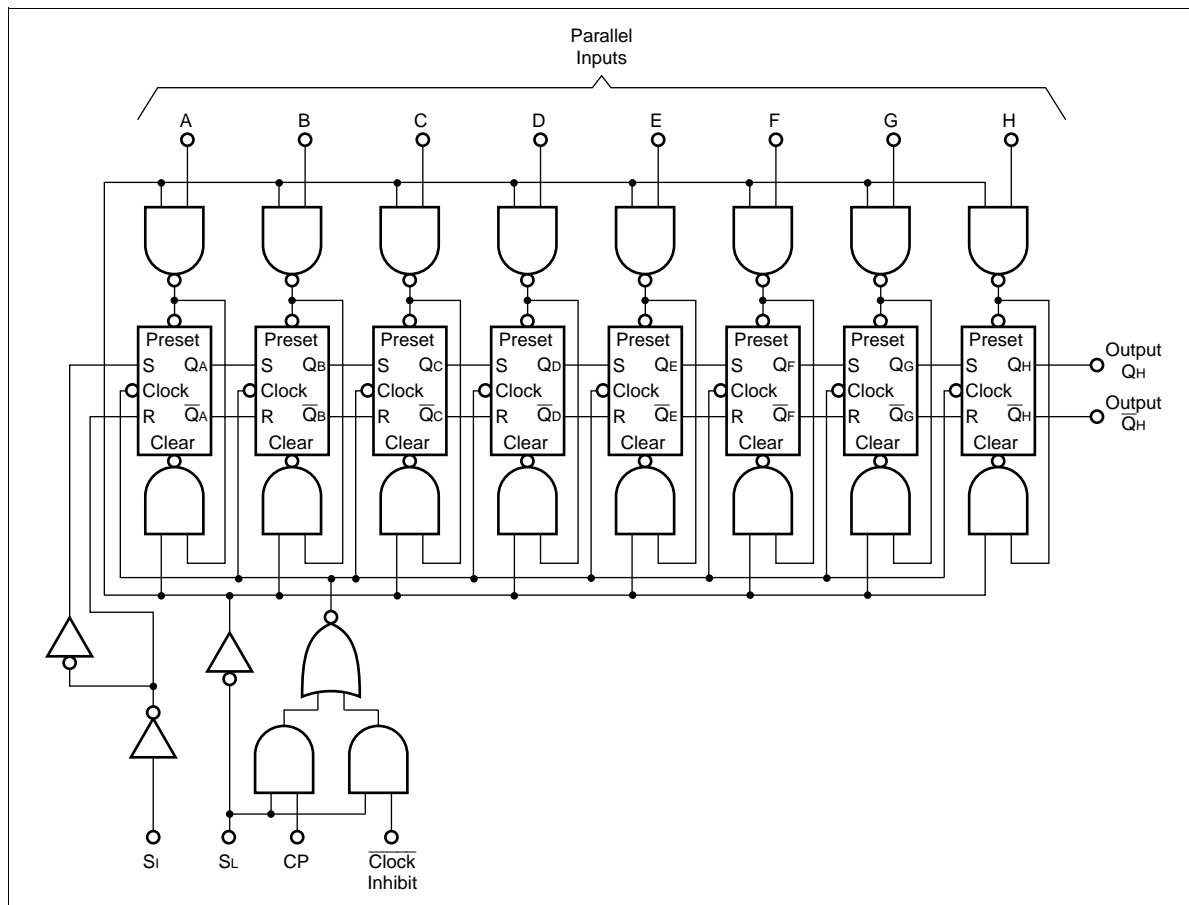
L : Low Voltage Level

X : Immaterial

 : Low-to-High Clock Transition

# HD74AC165/HD74ACT165

## Logic Diagram



## DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	$I_{CC}$	80	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$
Maximum quiescent supply current	$I_{CC}$	8.0	$\mu A$	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$ , $T_a = 25^\circ C$
Maximum additional $I_{CC}/\text{input}$ (HD74ACT165)	$I_{CCT}$	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ , $V_{CC} = 5.5 V$ , $T_a = \text{Worst case}$

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AC Characteristics: HD74AC165

Item	Symbol	V <sub>CC</sub> (V) <sup>*1</sup>	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f <sub>max</sub>	3.3	85	—	—	70	—	MHz
		5.0	100	—	—	90	—	
Propagation delay CP to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	3.3	1.0	11.0	17.5	1.0	20.5	ns
		5.0	1.0	8.0	11.5	1.0	13.5	
Propagation delay CP to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	3.3	1.0	12.0	18.0	1.0	21.5	ns
		5.0	1.0	8.5	12.5	1.0	14.5	
Propagation delay H to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	3.3	1.0	13.5	19.5	1.0	22.5	ns
		5.0	1.0	9.5	13.5	1.0	15.5	
Propagation delay H to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	3.3	1.0	9.0	14.0	1.0	16.5	ns
		5.0	1.0	6.5	9.5	1.0	11.0	
Propagation delay S <sub>L</sub> to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	3.3	1.0	11.5	20.5	1.0	23.5	ns
		5.0	1.0	8.5	14.0	1.0	16.0	
Propagation delay S <sub>L</sub> to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	3.3	1.0	10.0	16.5	1.0	19.5	ns
		5.0	1.0	7.5	11.0	1.0	12.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

# HD74AC165/HD74ACT165

## AC Operating Requirements: HD74AC165

Item	Symbol	V <sub>CC</sub> (V)*1	Ta = +25°C	Ta = -40°C		Unit
			C <sub>L</sub> = 50 pF	to +85°C	C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW	t <sub>su</sub>	3.3	3.5	5.0	6.0	ns
H to S <sub>L</sub>		5.0	2.5	4.0	4.5	
Hold time, HIGH or LOW	t <sub>h</sub>	3.3	-1.0	0.5	0.5	ns
H to S <sub>L</sub>		5.0	-0.5	0.5	0.5	
Setup time, HIGH or LOW	t <sub>su</sub>	3.3	1.0	3.5	4.0	ns
S <sub>in</sub> to CP		5.0	0.5	3.0	3.5	
Hold time, HIGH or LOW	t <sub>h</sub>	3.3	1.5	2.0	2.0	ns
S <sub>in</sub> to CP		5.0	1.0	2.0	2.0	
Setup time, HIGH or LOW	t <sub>su</sub>	3.3	3.0	5.0	6.0	ns
S <sub>L</sub> to CP		5.0	2.0	4.0	4.5	
Hold time, HIGH or LOW	t <sub>h</sub>	3.3	-2.0	0.0	0.0	ns
S <sub>L</sub> to CP		5.0	-1.0	0.0	0.0	
Recovery time clock inhibit	t <sub>rec</sub>	3.3	2.5	3.5	3.5	ns
to CP		5.0	2.0	3.0	3.0	
Clock pulse width	t <sub>w</sub>	3.3	3.0	5.5	7.0	ns
		5.0	3.0	4.5	5.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

**AC Characteristics: HD74ACT165**

Item	Symbol	V <sub>cc</sub> (V)*1	Ta = +25°C C <sub>L</sub> = 50 pF			Ta = -40°C to +85°C C <sub>L</sub> = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f <sub>max</sub>	5.0	7.0	—	—	60	—	MHz
Propagation delay CP to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	5.0	1.0	8.5	13.5	1.0	15.5	ns
Propagation delay CP to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	5.0	1.0	9.5	14.0	1.0	16.5	ns
Propagation delay H to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	5.0	1.0	10.5	13.5	1.0	15.5	ns
Propagation delay H to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	5.0	1.0	7.5	11.0	1.0	12.5	ns
Propagation delay S <sub>L</sub> to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PLH</sub>	5.0	1.0	9.5	15.0	1.0	18.0	ns
Propagation delay S <sub>L</sub> to Q <sub>H</sub> or $\overline{Q}_H$	t <sub>PHL</sub>	5.0	1.0	8.5	13.0	1.0	15.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

# HD74AC165/HD74ACT165

## AC Operating Requirements: HD74ACT165

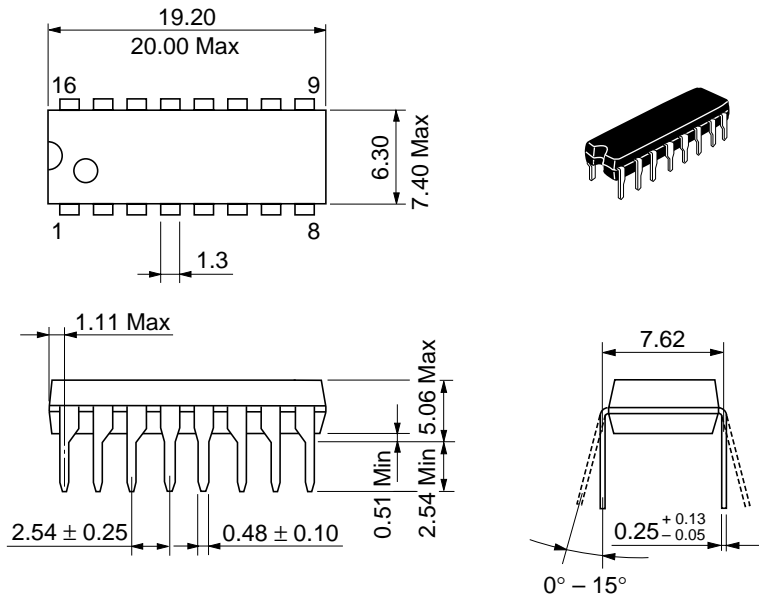
Item	Symbol	$V_{CC}$ (V)*1	Ta = +25°C	Ta = -40°C		Unit
			C <sub>L</sub> = 50 pF	to +85°C	C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW H to S <sub>L</sub>	t <sub>su</sub>	5.0	3.0	4.0	4.5	ns
Hold time, HIGH or LOW H to S <sub>L</sub>	t <sub>h</sub>	5.0	-1.0	0.0	0.0	ns
Setup time, HIGH or LOW S <sub>in</sub> to CP	t <sub>su</sub>	5.0	0.5	3.0	3.5	ns
Hold time, HIGH or LOW S <sub>in</sub> to CP	t <sub>h</sub>	5.0	0.5	2.0	2.0	ns
Setup time, HIGH or LOW S <sub>L</sub> to CP	t <sub>su</sub>	5.0	2.0	4.0	4.5	ns
Hold time, HIGH or LOW S <sub>L</sub> to CP	t <sub>h</sub>	5.0	-1.5	0.0	0.0	ns
Recovery time clock inhibit to CP	t <sub>rec</sub>	5.0	2.0	3.0	3.0	ns
Clock pulse width	t <sub>w</sub>	5.0	3.5	7.0	8.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

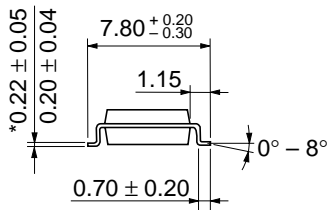
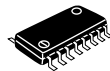
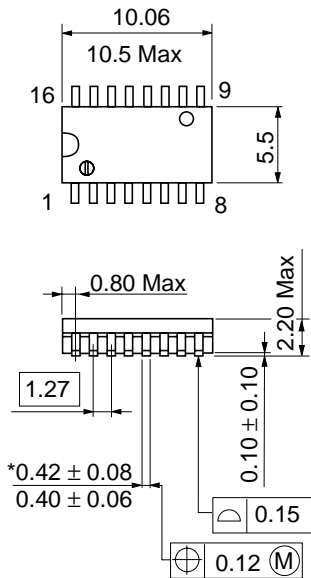
## Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C <sub>IN</sub>	4.5	pF	V <sub>CC</sub> = 5.5 V
Power dissipation capacitance	C <sub>PD</sub>	5.0	pF	V <sub>CC</sub> = 5.0 V



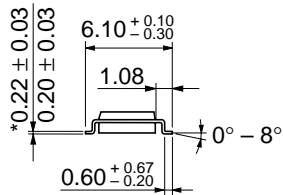
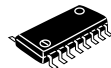
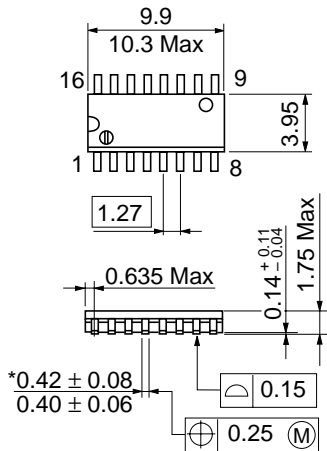


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



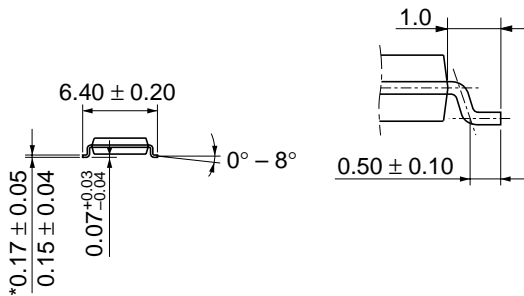
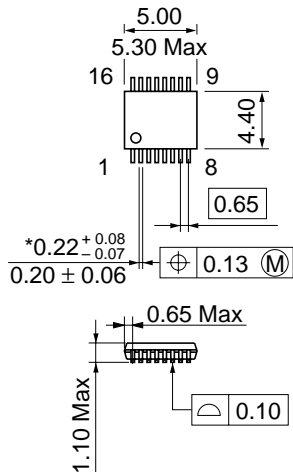
\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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