
HD74AC373/HD74ACT373

Octal Transparent Latch with 3-State Output

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Description Diagram

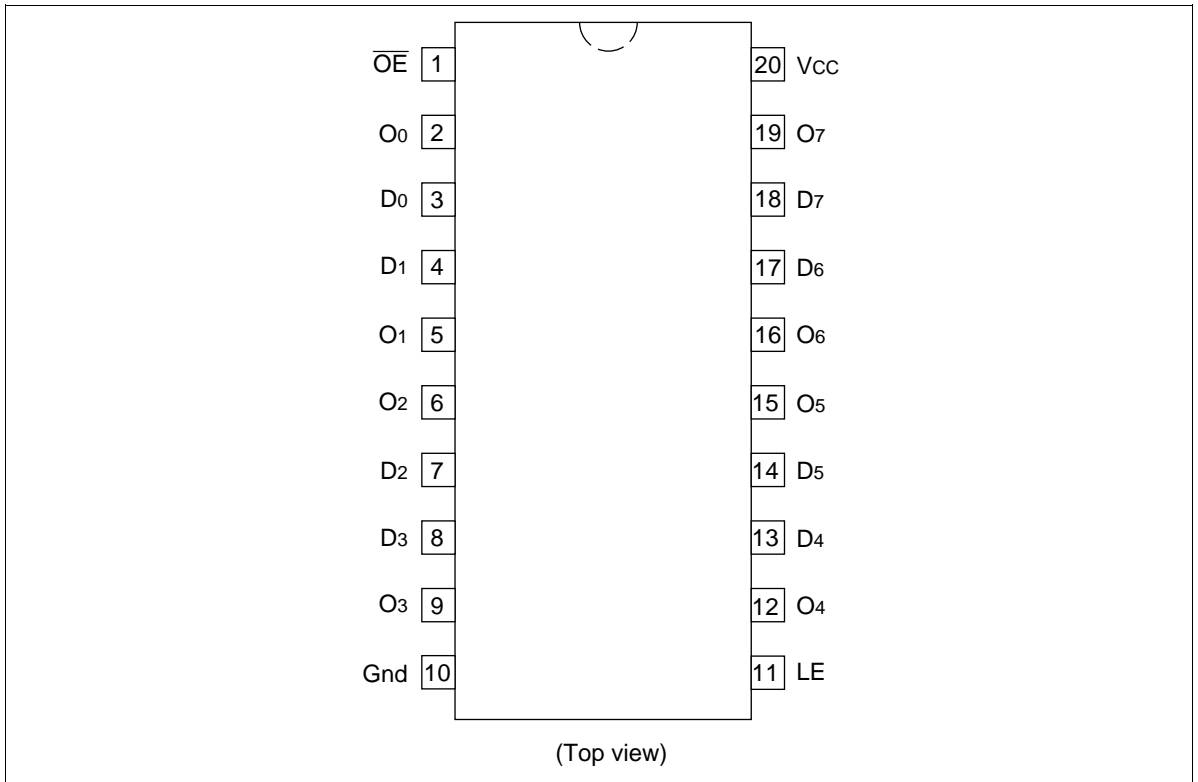
The HD74AC373/HD74ACT373 consists of eight latches with 3-state outputs from bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is High. When LE is Low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is Low. When \overline{OE} is High, the bus output is in the high impedance state.

Features

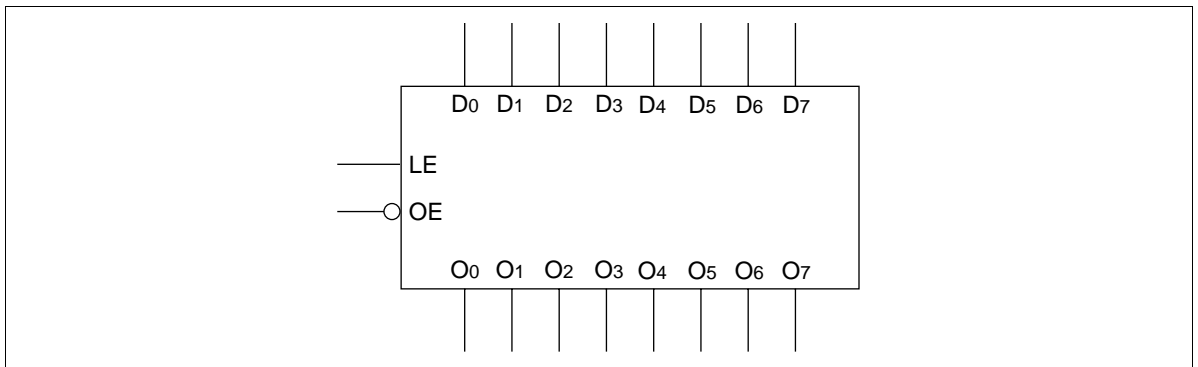
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- HD74AC373 has TTL-Compatible Inputs

HD74AC373/HD74ACT373

Pin Arrangement



Logic Symbol



Pin Names

- D₀ – D₇ Data Inputs
- LE Latch Enable Input
- \overline{OE} Output Enable Input
- O₀ – O₇ 3-State Latch Outputs

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Truth Table

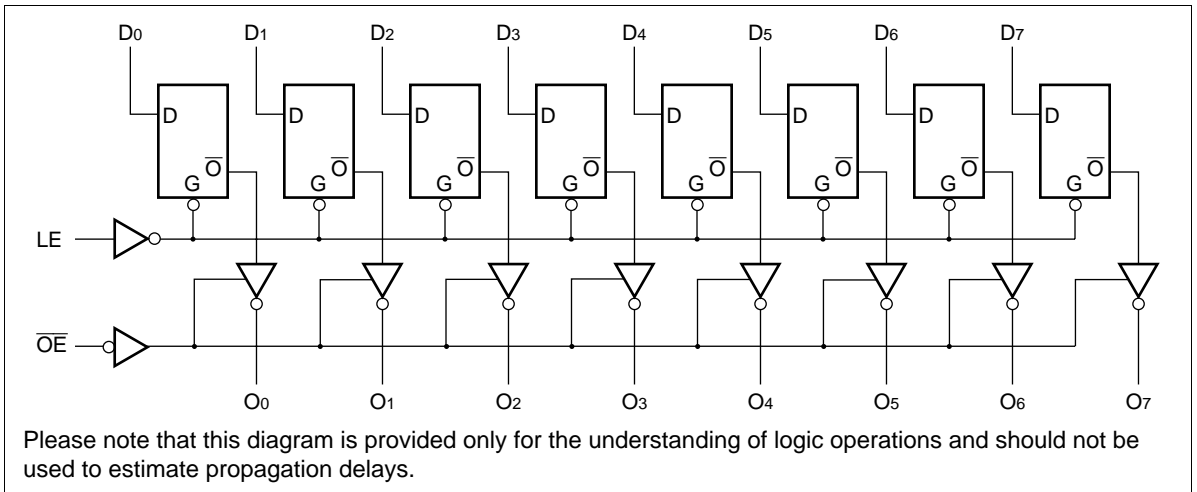
Inputs			Outputs
\overline{OE}	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

- H : High Voltage Level
- L : Low Voltage Level
- Z : High Impedance
- X : Immaterial
- O_0 : Previous O_0 before Low-to-High Transition of Clock

Functional Description

The HD74AC373/HD74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is High, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is Low, the latches store the information that was present on the D inputs setup time preceding the High-to-Low transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is Low, the standard outputs are in the 2-state mode. When \overline{OE} is High, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



HD74AC373/HD74ACT373

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = 25^\circ\text{C}$
Maximum I_{CC}/input (HD74ACT373)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1\text{ V}$, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$

AC Characteristics: HD74AC373

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
D_n to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	9.5	13.0	1.0	14.5	ns
D_n to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
LE to O_n		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	9.5	12.5	1.0	14.0	ns
LE to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Output enable time	t_{PZH}	3.3	1.0	9.0	11.5	1.0	13.5	ns
		5.0	1.0	7.0	8.5	1.0	9.5	
Output enable time	t_{PZL}	3.3	1.0	8.5	11.5	1.0	13.0	ns
		5.0	1.0	6.5	8.5	1.0	9.5	
Output disable time	t_{PHZ}	3.3	1.0	10.0	12.5	1.0	14.5	ns
		5.0	1.0	8.0	11.0	1.0	12.5	
Output disable time	t_{PLZ}	3.3	1.0	8.0	11.5	1.0	12.5	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is $3.3\text{ V} \pm 0.3\text{ V}$
Voltage Range 5.0 is $5.0\text{ V} \pm 0.5\text{ V}$

AC Characteristics: HD74AC373

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay D _n to O _n	t _{PLH}	5.0	1.0	8.5	10.0	1.0	11.5	ns
Propagation delay D _n to O _n	t _{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Propagation delay LE to O _n	t _{PLH}	5.0	1.0	8.5	11.0	1.0	11.5	ns
Propagation delay LE to O _n	t _{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Output enable time	t _{PZH}	5.0	1.0	8.0	9.5	1.0	10.5	ns
Output enable time	t _{PZL}	5.0	1.0	7.5	9.0	1.0	10.5	ns
Output disable time	t _{PHZ}	5.0	1.0	9.0	11.0	1.0	12.5	ns
Output disable time	t _{PLZ}	5.0	1.0	7.5	8.5	1.0	10.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC373

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF		Unit
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
Setup time, HIGH or LOW	t _{su}	3.3	3.5	5.5	6.0	ns	
D _n to LE		5.0	2.0	4.0	4.5		
Hold time, HIGH or LOW	t _h	3.3	-3.0	0.0	0.0	ns	
D _n to LE		5.0	-1.5	0.0	0.0		
LE pulse width, HIGH	t _w	3.3	4.0	5.5	6.0	ns	
		5.0	2.0	4.0	4.5		

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

HD74AC373/HD74ACT373

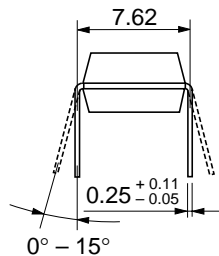
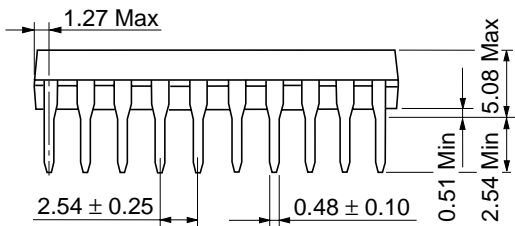
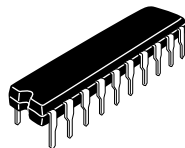
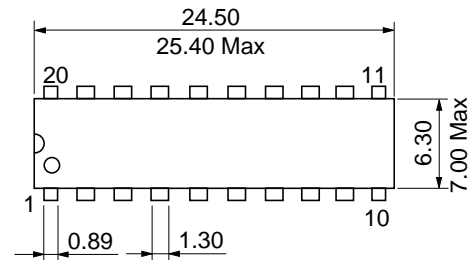
AC Operating Requirements: HD74ACT373

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF		Ta = -40°C to +85°C CL = 50 pF	
			Typ	Guaranteed Minimum	Guaranteed Minimum	Unit
Setup time, HIGH or LOW D _n to LE	t _{su}	5.0	3.0	7.0	8.0	ns
Hold time, HIGH or LOW D _n to LE	t _h	5.0	0.0	0.0	1.0	ns
LE pulse width, HIGH	t _w	5.0	2.0	7.0	8.0	ns

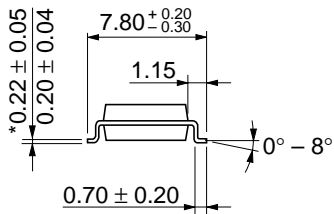
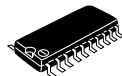
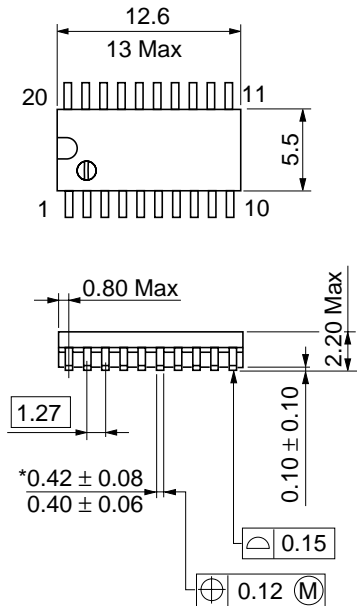
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	40.0	pF	V _{CC} = 5.0 V

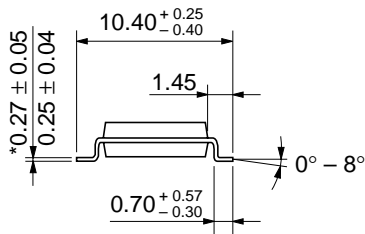
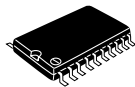
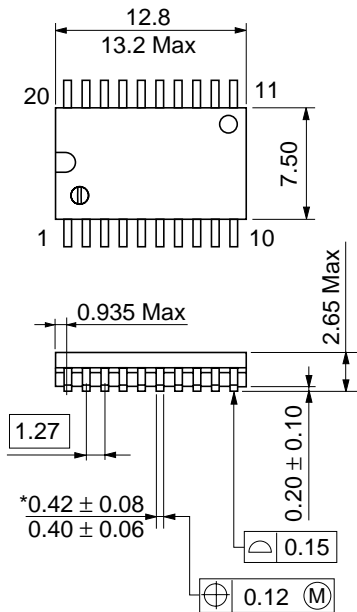


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



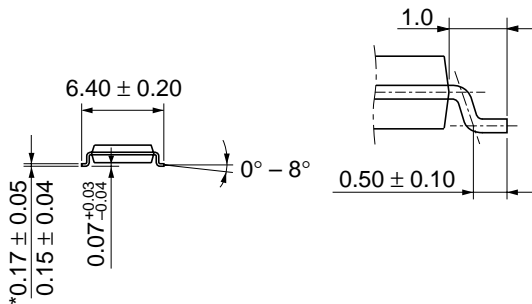
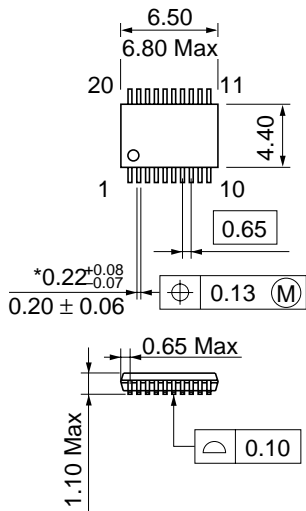
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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