

HD74AC74

Dual D-Type Positive Edge-Triggered Flip-Flop

REJ03D0277-0200Z
 (Previous ADE-205-361 (Z))
 Rev.2.00
 Jul.16.2004

Description

The HD74AC74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Features

Asynchronous Inputs:

- Low input to \bar{S}_D (Set) sets Q to High level
- Low input to \bar{C}_D (Clear) sets Q to Low level
- Clear and Set are independent of clock
- Simultaneous Low on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} High

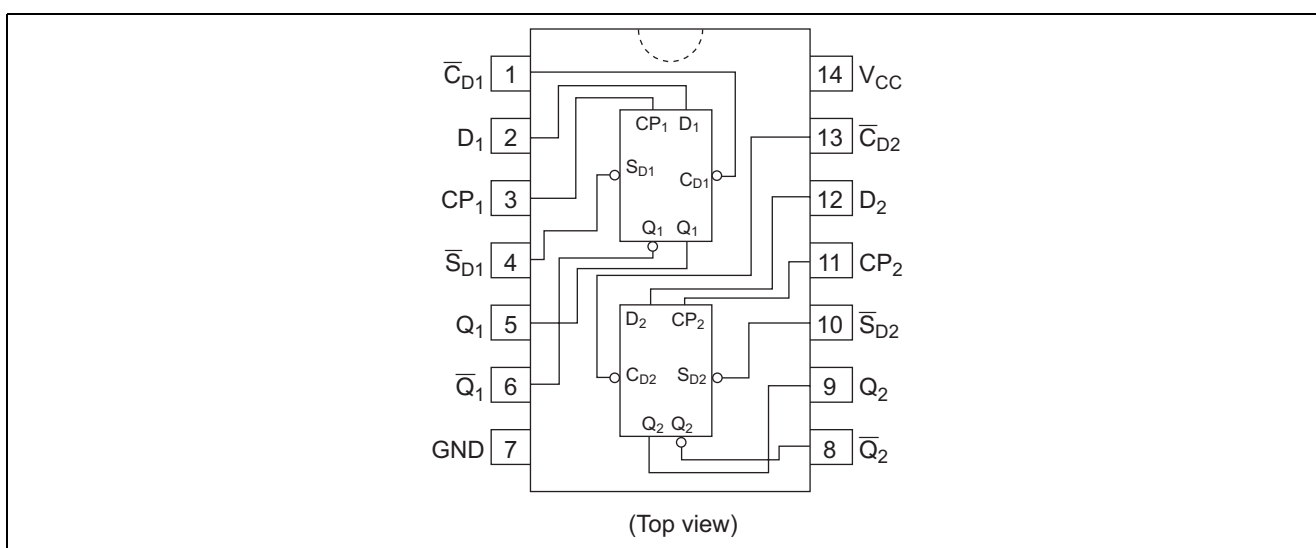
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC74P	DIP-14 pin	DP-14, -14AV	P	—
HD74AC74FPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74AC74RPEL	SOP-14 pin (JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)
HD74AC74TELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

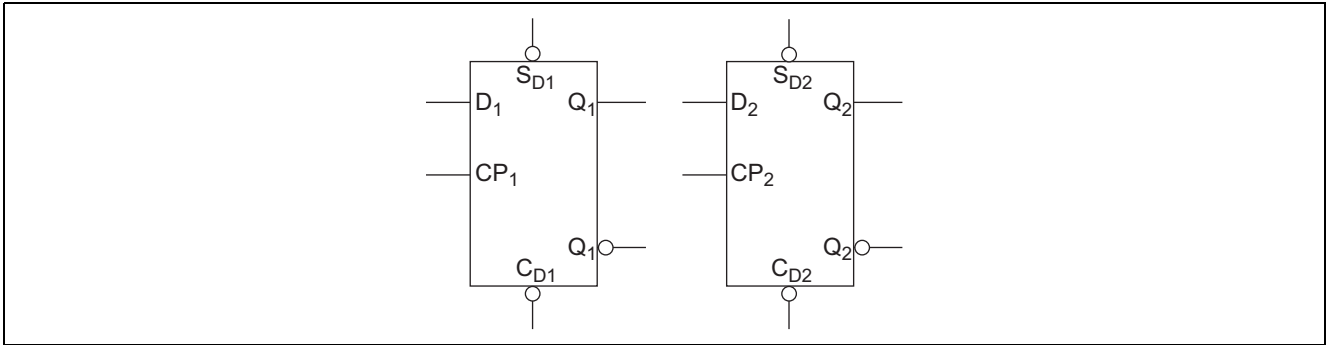
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

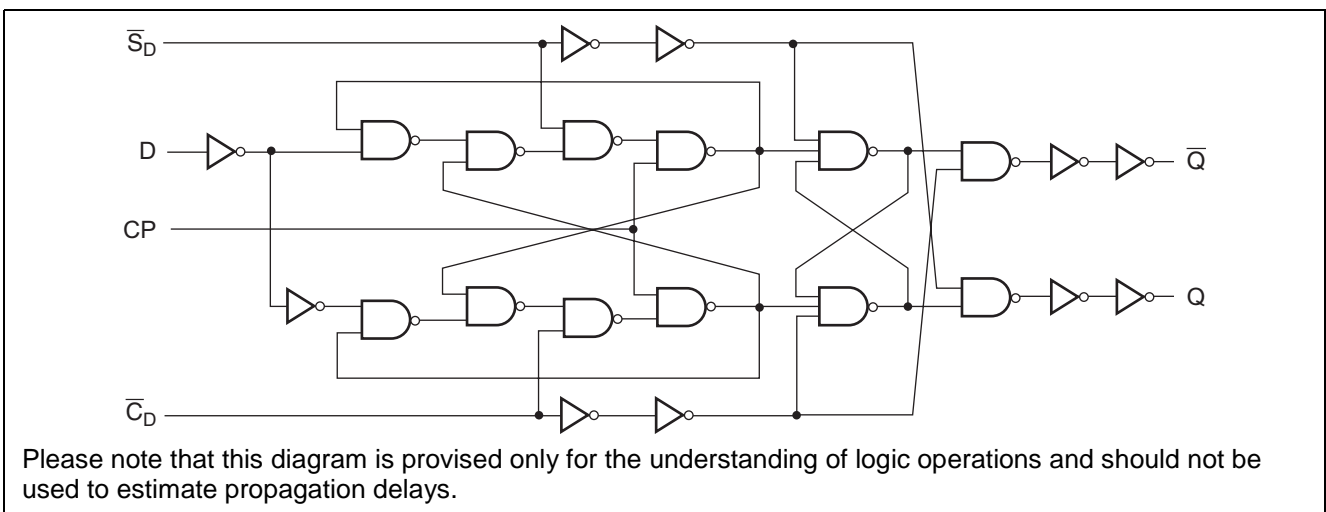
- D_1, D_2 Data Inputs
- CP_1, CP_2 Clock Pulse Inputs
- $\overline{C}_{D1}, \overline{C}_{D2}$ Direct Clear Inputs
- $\overline{S}_{D1}, \overline{S}_{D2}$ Direct Set Inputs
- $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$ Outputs

Truth Table (Each Half)

Inputs				Outputs	
\overline{S}_D	\overline{C}_D	CP	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H		H	H	L
H	H		L	L	H
H	H	L	X	Q_0	\overline{Q}_0

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial
- : Low-to-High Clock Transition
- $Q_0 (\overline{Q}_0)$: Previous Q (\overline{Q}) before Low-to-High Transition of Clock

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5V$
				$V_{CC} = 5.5V$

DC Characteristics

Item	Sym- bol	Vcc (V)	$T_a = 25^\circ C$			$T_a = -40$ to $+85^\circ C$		Unit	Condition			
			min.	typ.	max.	min.	max.					
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$			
		4.5	3.15	2.25	—	3.15	—					
		5.5	3.85	2.75	—	3.85	—					
	V_{IL}	3.0	—	1.50	0.9	—	0.9		$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$			
		4.5	—	2.25	1.35	—	1.35					
		5.5	—	2.75	1.65	—	1.65					
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -50 \mu A$			
		4.5	4.4	4.49	—	4.4	—					
		5.5	5.4	5.49	—	5.4	—					
		3.0	2.58	—	—	2.48	—				$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	
		4.5	3.94	—	—	3.80	—					
		5.5	4.94	—	—	4.80	—					
	V_{OL}	3.0	—	0.002	0.1	—	0.1		$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = 50 \mu A$			
		4.5	—	0.001	0.1	—	0.1					
		5.5	—	0.001	0.1	—	0.1					
		3.0	—	—	0.32	—	0.37		$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$			
		4.5	—	—	0.32	—	0.37					
		5.5	—	—	0.32	—	0.37					
Input leakage current	I_{IN}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{IN} = V_{CC}$ or GND			
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	$V_{OLD} = 1.1V$			
	I_{OHD}	5.5	—	—	—	-75	—	mA	$V_{OHD} = 3.85V$			
Quiescent supply current	I_{CC}	5.5	—	—	4.0	—	40	μA	$V_{IN} = V_{CC}$ or ground			

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	100	125	—	95	—	MHz
		5.0	140	160	—	125	—	
Propagation delay C _{Dn} or S _{Dn} to Q _n or Q _n	t _{PLH}	3.3	1.0	8.0	12.0	1.0	13.0	ns
		5.0	1.0	6.0	9.0	1.0	10.0	
Propagation delay C _{Dn} or S _{Dn} to Q _n or Q _n	t _{PHL}	3.3	1.0	10.5	12.0	1.0	13.5	ns
		5.0	1.0	8.0	9.5	1.0	10.5	
Propagation delay CP _n to Q _n or Q _n	t _{PLH}	3.3	1.0	8.0	13.5	1.0	16.0	ns
		5.0	1.0	6.0	10.0	1.0	10.5	
Propagation delay CP _n to Q _n or Q _n	t _{PHL}	3.3	1.0	8.0	14.0	1.0	14.5	ns
		5.0	1.0	6.0	10.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW D _n to CP _n	t _{su}	3.3	1.5	4.0	4.5	ns
		5.0	1.0	3.0	3.0	
Hold time, HIGH or LOW D _n to CP _n	t _h	3.3	-2.0	0	0	ns
		5.0	-1.5	0	0	
CP _n or C _{Dn} or S _{Dn} Pulse width	t _w	3.3	3.0	5.5	7.0	ns
		5.0	2.5	4.5	5.0	
Recovery time C _{Dn} or S _{Dn} to CP	t _{rec}	3.3	-2.5	0	0	ns
		5.0	-2.0	0	0	

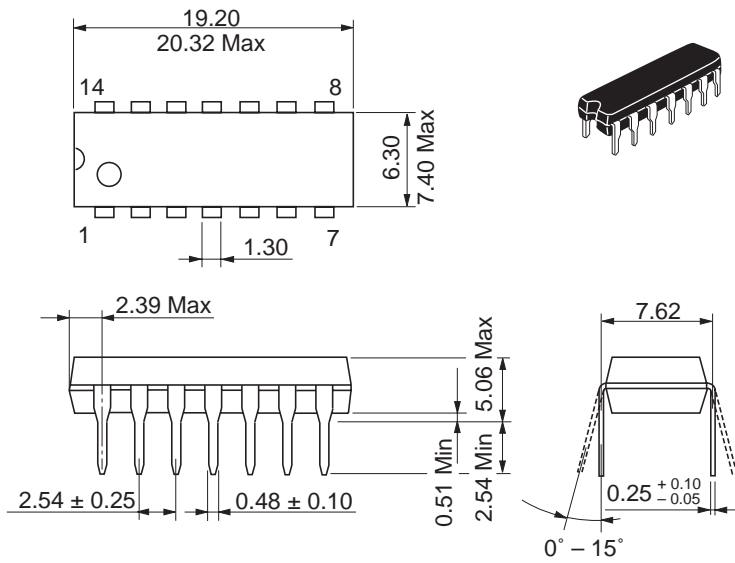
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	35.0	pF	V _{CC} = 5.0 V

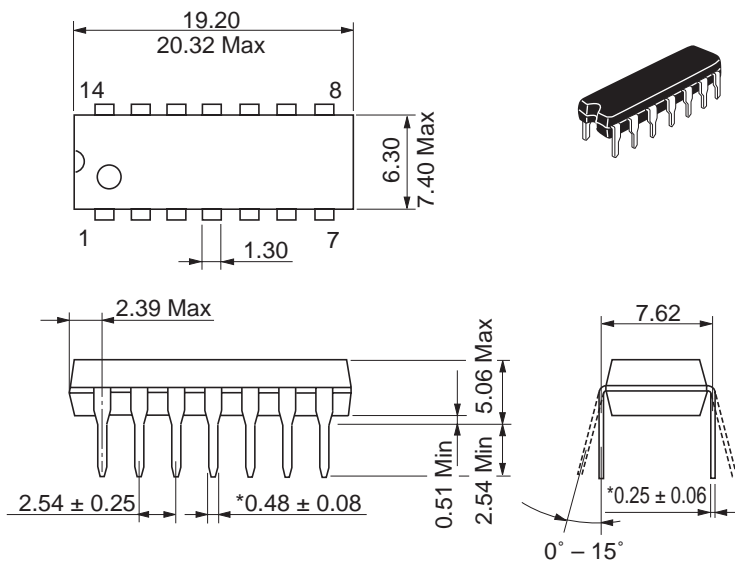
Package Dimensions

As of January, 2003
Unit: mm



Package Code	DP-14
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.97 g

Unit: mm

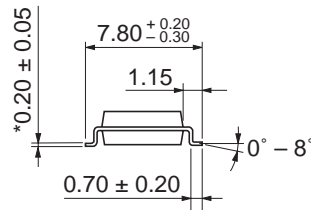
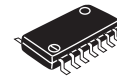
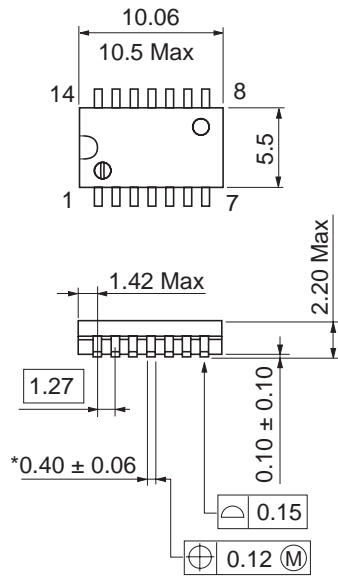


*Ni/Pd/AU Plating

Package Code	DP-14AV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.97 g

As of January, 2003

Unit: mm

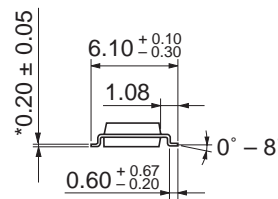
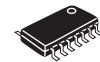
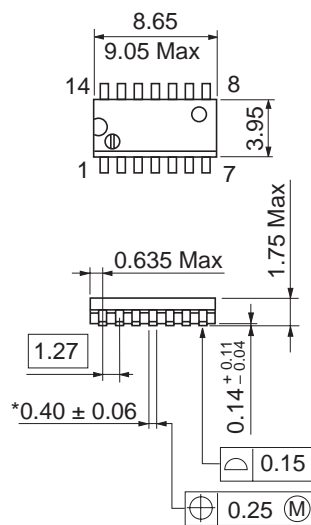


*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003

Unit: mm

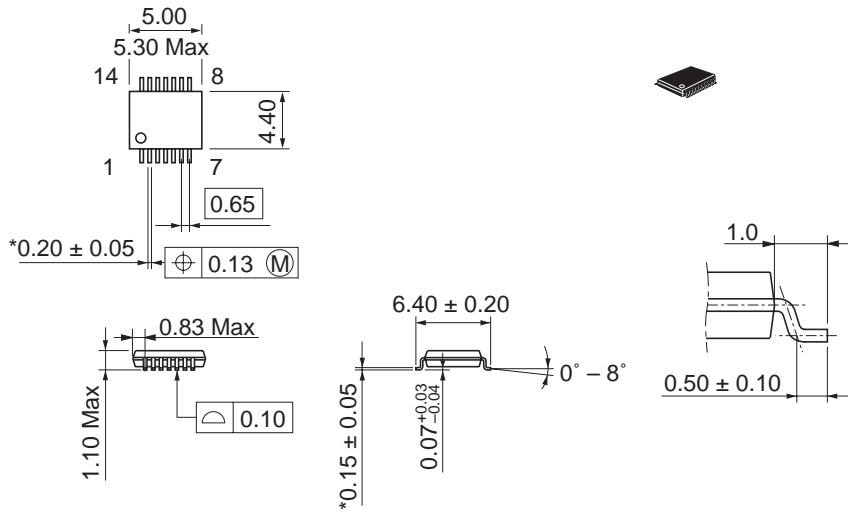


*Ni/Pd/Au plating

Package Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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