

HD74BC245A

Octal Bus Transceivers With 3 State Outputs

REJ03D0282-0400Z (Previous ADE-205-008B (Z)) Rev.4.00 Jul.16.2004

Description

The HD74BC245A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has ten buffers with three state outputs in a 20 pin package. Each device has an active low enable input \overline{G} and a direction control input DiR. When DiR is high, data flows from the A inputs to the B outputs. When DiR is low, data flows from the B inputs to the A outputs. When G is high, disables both A and B ports by placing then in a high impedance.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range

 $Ta = -40 \text{ to} + 85^{\circ}\text{C}$

• Ordering Information

Part Name	Package Type	Package Code	Package	Taping Abbreviation
			Abbreviation	(Quantity)
HD74BC245AP	DILP-20 pin	DP-20N, -20NEV	Р	_
HD74BC245AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74BC245ATELL	TSSOP-20 pin	TTP-20DAV	Т	ELL (2,000 pcs/reel)

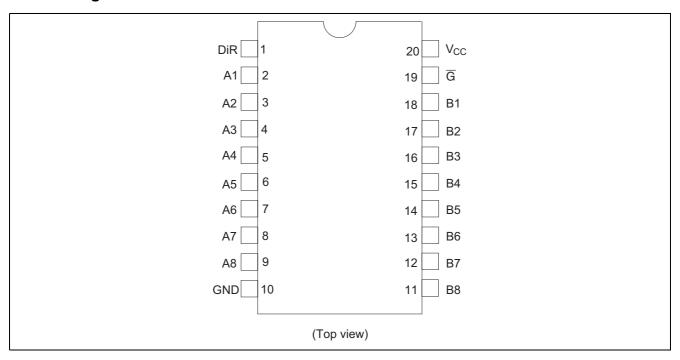
Note: Please consults the sales office for the above package availability.

Function Table

Contro	ol Inputs	
G DiR		Operation
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Z

H : High levelL : Low levelZ : High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{cc}	-0.5 to +7.0	V
Input diode current	I _{IK}	±30	mA
Input voltage	V _{IN}	-0.5 to +7.5	V
Output voltage	V_{OUT}	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	Tstg	-65 to +150	°C

Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

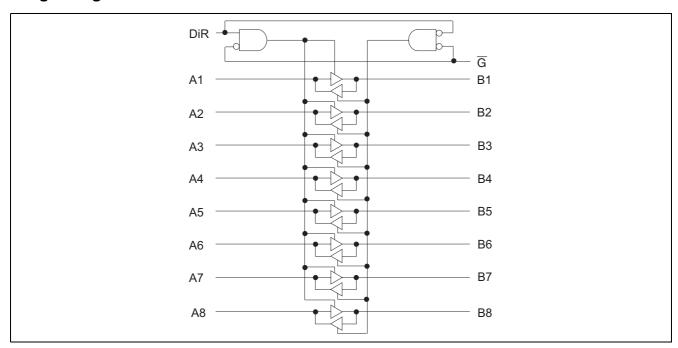
Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	V _{cc}	4.5	5.0	5.5	V
Input voltage	V _{IN}	0	_	V _{cc}	V
Output voltage	V _{OUT}	0	_	V _{cc}	V
Operating temperature	Topr	-40	_	85	°C
Input rise/fall time*1	t _r , t _f	0	_	8	ns/V

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Note: 1. This item guarantees maximum limit when one input switches. Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics (Ta = -40°C to +85°C)

Item	Symbol	V _{cc} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}		2.0	_	V	
	V _{IL}		_	0.8	V	
Output voltage	V _{OH}	4.5	2.4	_	V	$I_{OH} = -3 \text{ mA}$
		4.5	2.0	_	V	$I_{OH} = -15 \text{ mA}$
	V _{OL}	4.5	_	0.5	V	I _{OL} = 48 mA
		4.5	_	0.55	V	I _{OL} = 64 mA
Input diode voltage	V _{IK}	4.5	_	-1.2	V	$I_{IN} = -18 \text{ mA}$
Input current	I ₁	5.5	_	-250	μΑ	$V_{IN} = 0 V$
		5.5	_	100	μΑ	An or Bn, V _{IN} = 5.5 V
		5.5	_	1.0	μΑ	DiR or \overline{G} , $V_{IN} = 5.5 \text{ V}$
		5.5	_	100	μΑ	DiR or \overline{G} , $V_{IN} = 7.0 \text{ V}$
Short circuit output current*1	I _{os}	5.5	-100	-225	mA	$V_{O} = 0 \text{ V}, V_{IN} = 5.5 \text{ V}$
Off state output current	I _{ozh}	5.5	_	-100	μΑ	V _O = 2.7 V
	I _{OZL}	5.5	_	-250	μΑ	V _o = 0.5 V
Supply current	I _{CCL}	5.5	_	31.5	mA	V _{IN} = 0 or 5.5 V
						All outputs is "L"
	I _{CCH}	5.5	_	0.5	mA	$V_{IN} = 0 \text{ or } 5.5 \text{ V}$
						All outputs is "H"
	I _{CCZ}	5.5	_	4.5	mA	$V_{IN} = 0 \text{ or } 5.5 \text{ V}$
						All outputs is "Z"
	I _{CCT} *2	5.5	_	1.5	mA	$V_{IN} = 3.4 \text{ or } 0.5 \text{ V}$

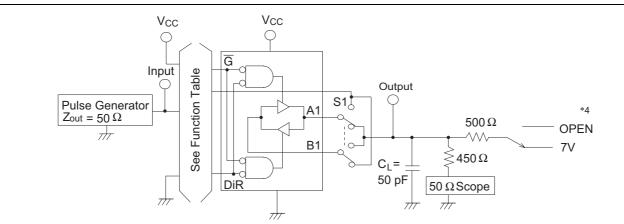
Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Test Method ($C_L = 50 \text{ pF}$)

			Ta = 25°C				
Item Symi		Min	Max	Min	Max	Unit	Test Conditions
Propagation delay time	t _{PLH}	3.0	6.0	3.0	7.0	ns	An to Bn
	t _{PHL}	3.0	6.0	3.0	7.0		
	t _{PLH}	3.0	6.0	3.0	7.0	ns	Bn to An
	t _{PHL}	3.0	6.0	3.0	7.0		
Output enable time	t_{ZH}	3.0	9.0	3.0	11.0	ns	G to Bn
	t_{ZL}	3.0	9.0	3.0	11.0		
	t_{ZH}	3.0	9.0	3.0	11.0	ns	G to An
	t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time	t_{HZ}	3.0	8.0	3.0	10.0	ns	G to Bn
	t _{LZ}	3.0	8.0	3.0	10.0		
	t _{HZ}	3.0	8.0	3.0	10.0	ns	G to An
	t _{LZ}	3.0	8.0	3.0	10.0		
Input capacitanse	C _{IN}	3.0(Typ)				pF	V _{IN} = V _{CC} or GND
Input/output capacitance	C _{I/O}	15.0(Typ))	_		pF	$V_{I/O} = V_{CC}$ or GND

^{2.} When input by the TTL level, it shows $\rm I_{\rm CC}$ increase at per one input pin.

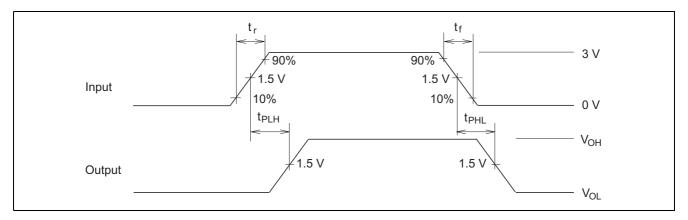
Test Circuit



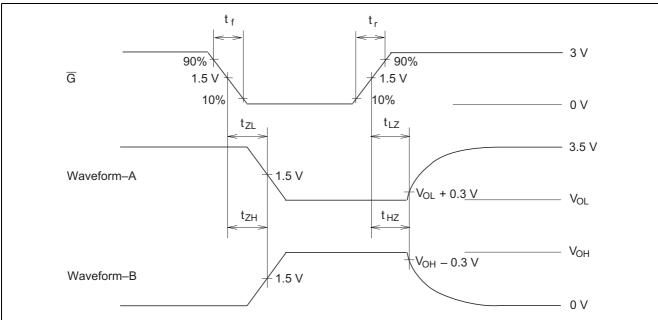
Notes:

- 1. C_L includes probe and jig capacitance.
- 2. A2-B2, A3-B3, A4-B4, A5-B5, A6-B6, A7-B7, A8-B8 are identical to above load circuit.
- 3. S1: Input-Output change switch.
- 4. Open: t_{PLH} , t_{PHL} , t_{ZH} , t_{HZ}
 - $7 \text{ V: } t_{ZL}\text{, } t_{LZ}$

Waveforms-1



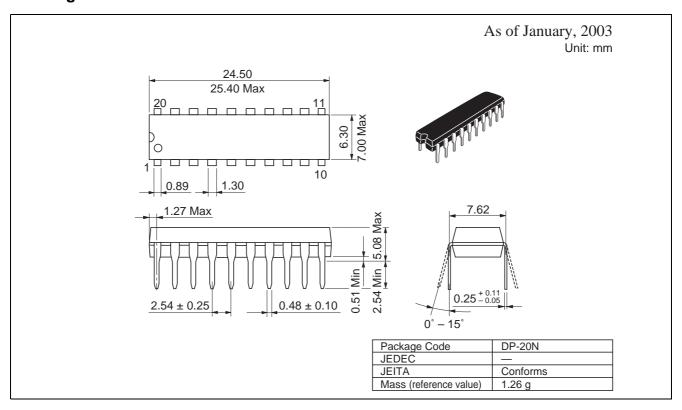
Waveforms-2

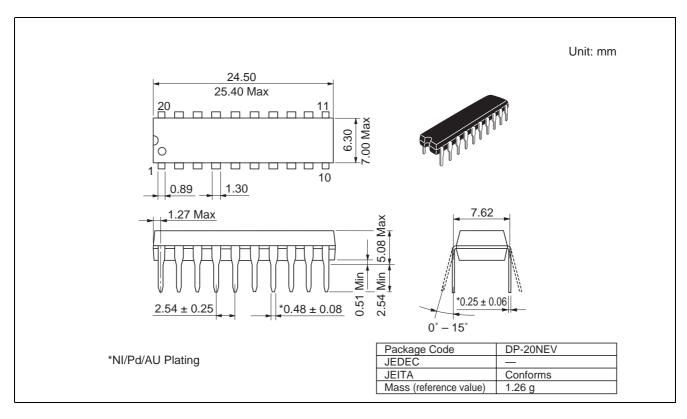


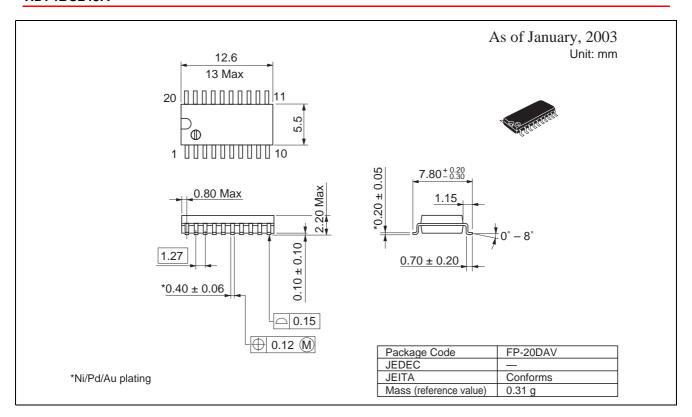
Notes:

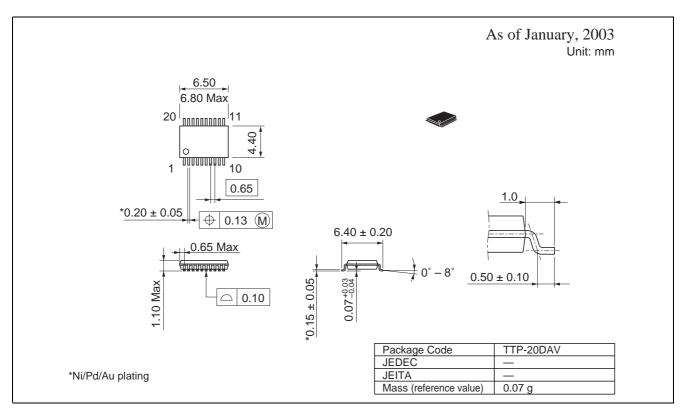
- 1. $t_r = 2.5 \text{ ns}, t_f = 2.5 \text{ ns}$
- 2. Input waveform: PRR = 1 MHz, duty cycle 50%
- 3. Waveform-A shows input conditions such that the output is "L" level when enable by the output control.
- 4. Waveform-B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions









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