HD74HC195

4-bit Parallel-Access Shift Register

HITACHI

Description

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; shift from Q_A towards Q_D.

Paralle loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or toggle flip-flop as shown in the function table.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 13 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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Function Table

Inputs									Outputs				
	Shift/		Serial		Parallel								
Clear	Load	Clock	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Q_D
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	⎍	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	⎍	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	⎍	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	⎍	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	⎍	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H : high level (steady state)

L : low level (steady state)

X : don't care

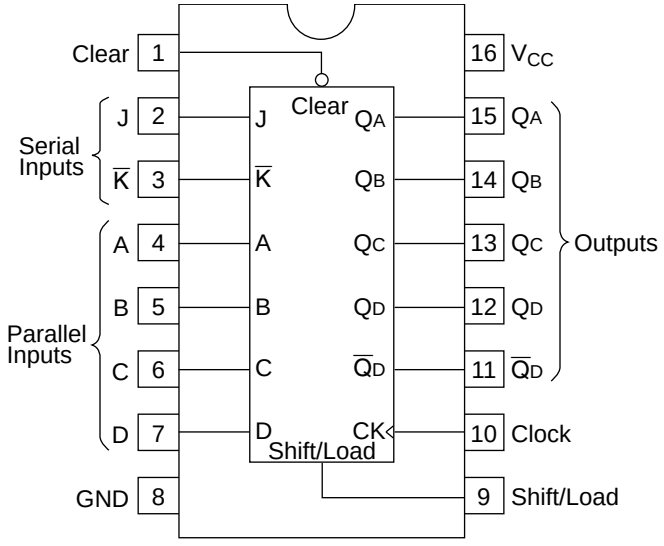
⎍ : transition from low to high level.

a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} : the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady-state input conditions were established.

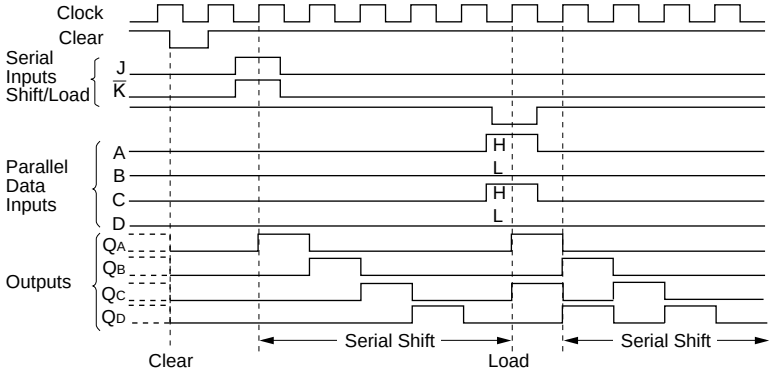
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} : the level of Q_A, Q_B, Q_C or Q_D respectively before the most recent ⎍ transition of the clock.

Pin Arrangement

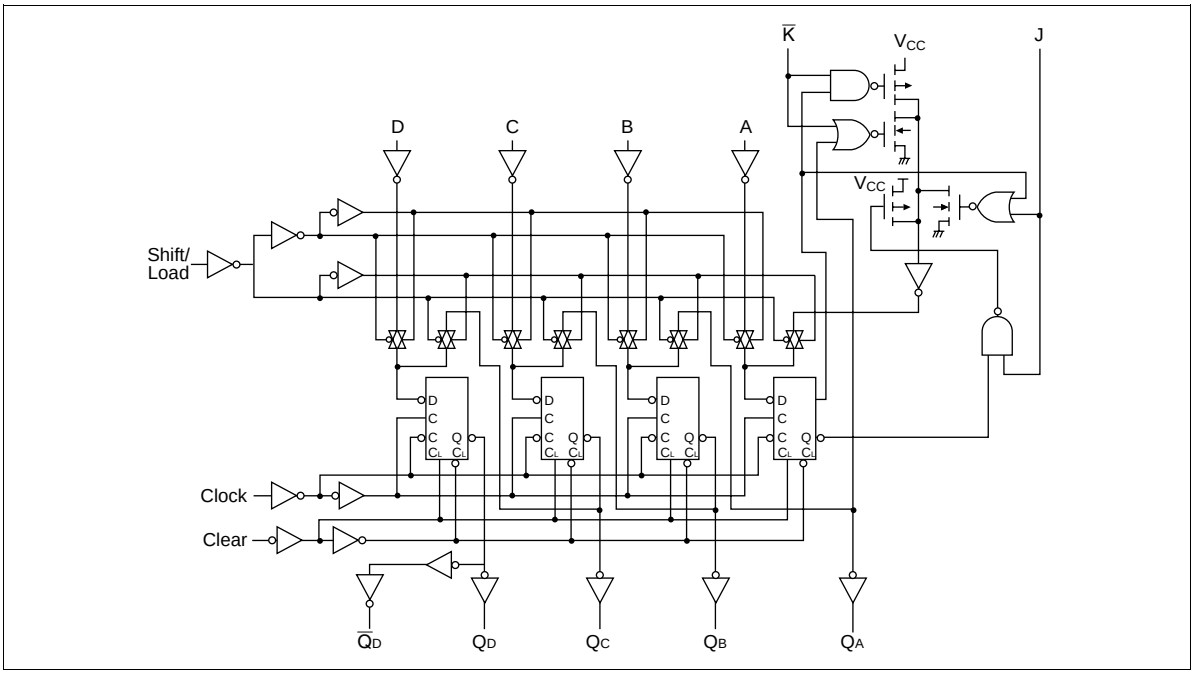


(Top view)

Timing Diagram



Logic Diagram



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

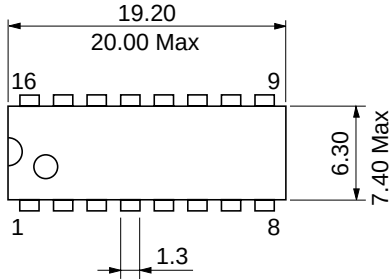
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

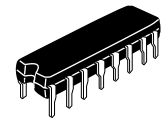
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MH_Z	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PHL}	2.0	—	—	140	—	175	ns	Clock to Q
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t_{PLH}	2.0	—	—	140	—	175	ns	
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock to Clear
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	A, B, C, D, J, $\overline{K}$ to Clock
		4.5	20	6	—	25	—		
		6.0	17	—	—	21	—		
		2.0	100	—	—	125	—	ns	Shift/Load to Clock
		4.5	20	13	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	Any input except Shift/Load
		4.5	0	–3	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t_{rem}	2.0	75	—	—	95	—	ns	Shift/Load to Clock
		4.5	15	8	—	19	—		
		6.0	13	—	—	16	—		
		2.0	25	—	—	31	—	ns	Clear inactive to Clock
		4.5	5	0	—	6	—		
		6.0	4	—	—	5	—		

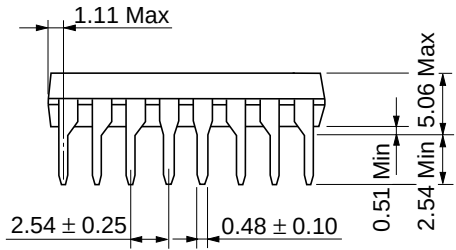
AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

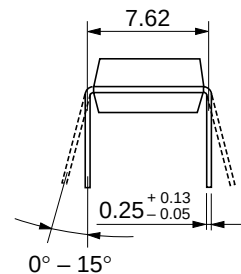
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm









Hitachi Code	DP-16
JEDEC	Conforms
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Weight (reference value)	1.07 g

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