HD74HC668/HD74HC669

Synchronous UP/Down Decade Counter
Synchronous Up/Down 4-bit binary Counter

HITACHI

Description

This synchronous presettable decade counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters.

A buffered clock input triggers the four master-slave flip-flops on the rising (positive going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. when the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, Enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

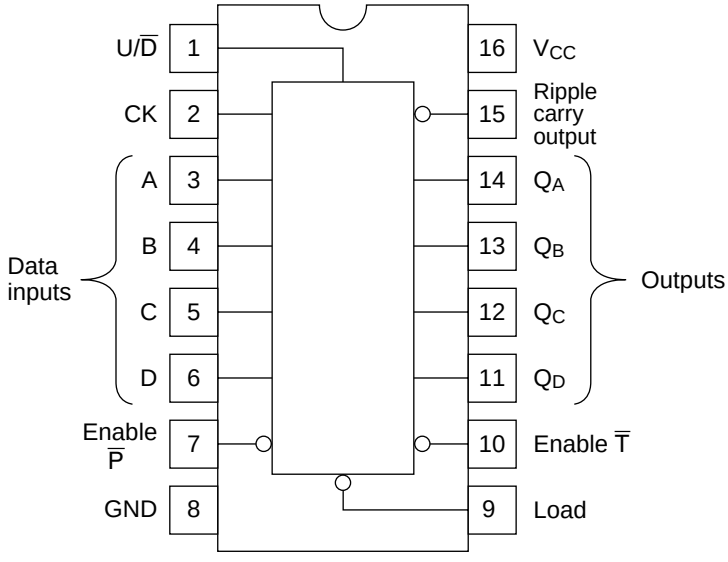
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max

Hitachi semiconductor

- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

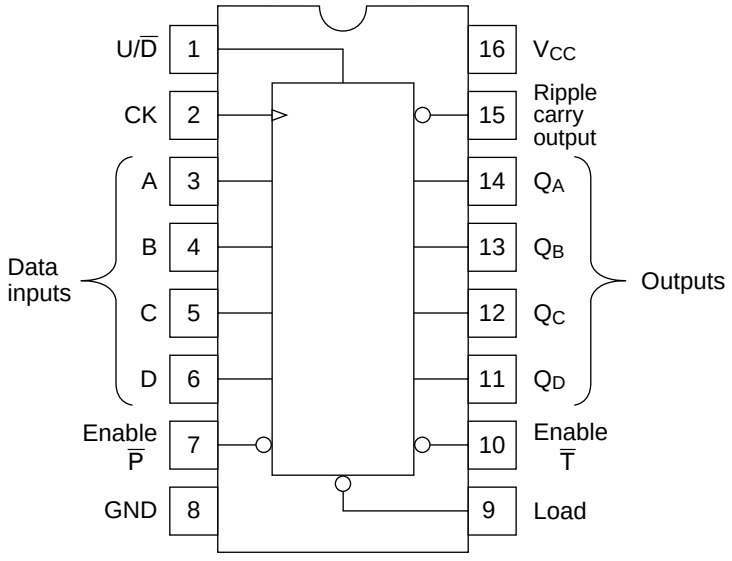
Pin Arrangement

HD74HC668



(Top view)

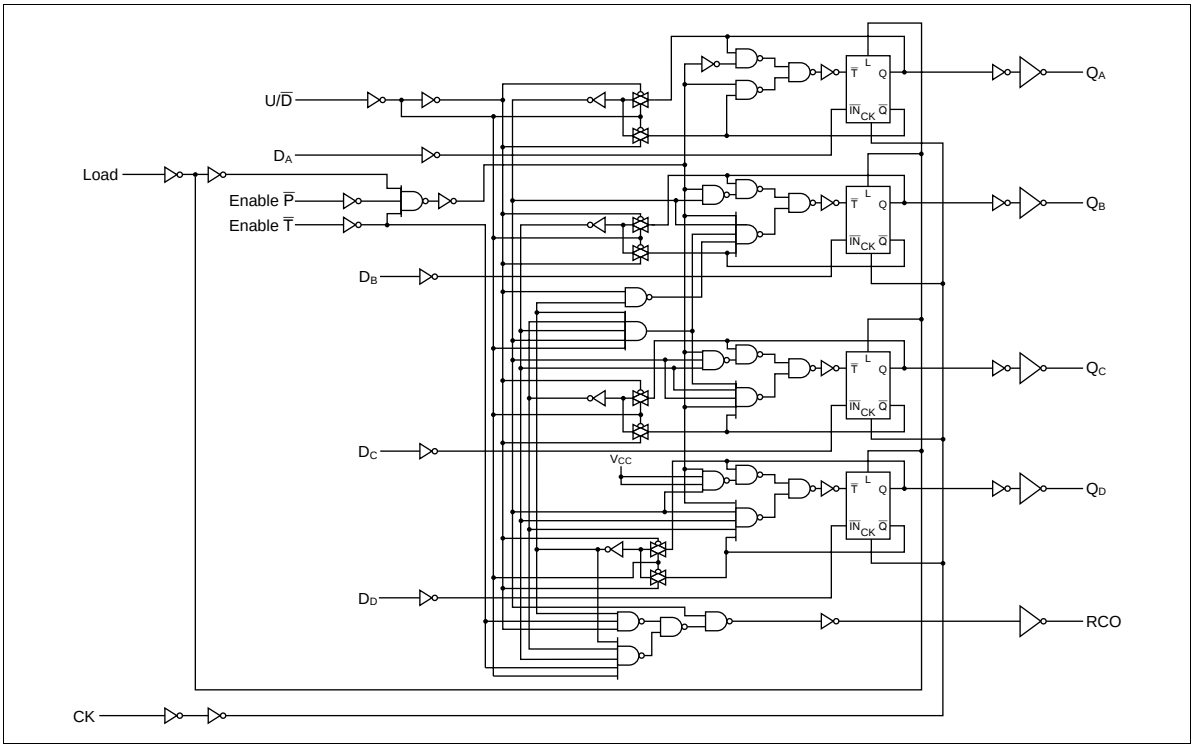
HD74HC669



(Top view)

Logic Diagram

HD74HC668



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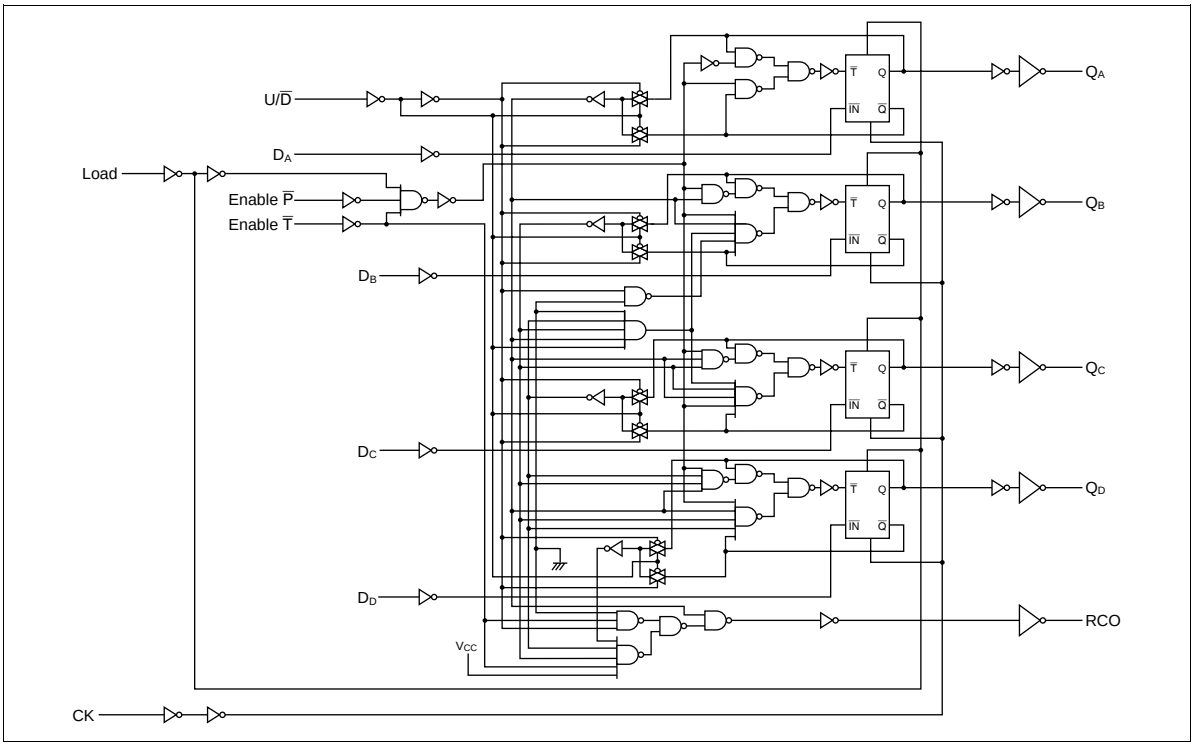
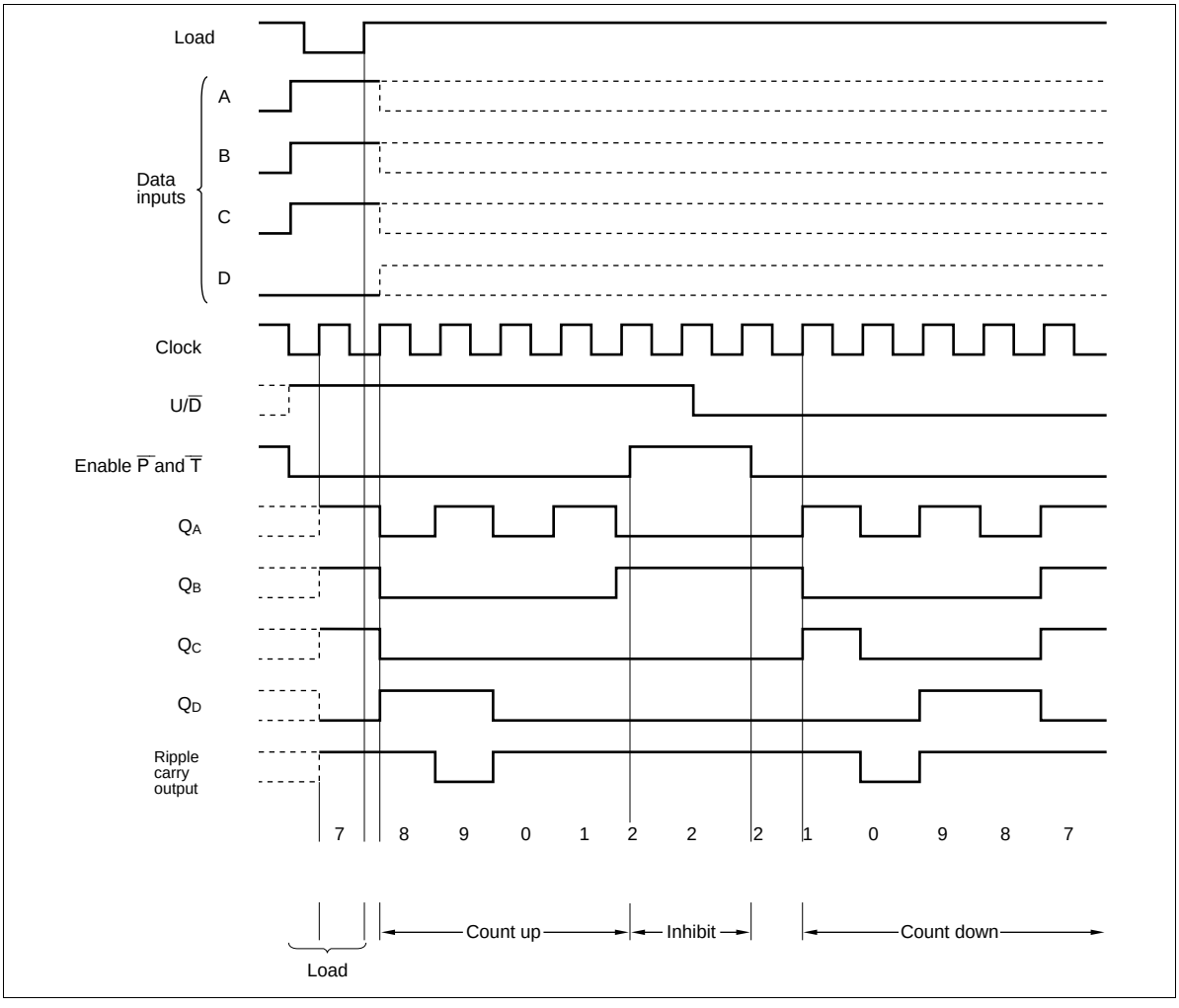

U/$\overline{D}$
D_A
Load
Enable $\overline{P}$
Enable $\overline{T}$
D_B
D_C
D_D
V_{CC}
CK
$\overline{T}$
Q
$\overline{IN}$
$\overline{Q}$
Q_A
Q_B
Q_C
Q_D
RCO

Timing Chart

HD74HC668



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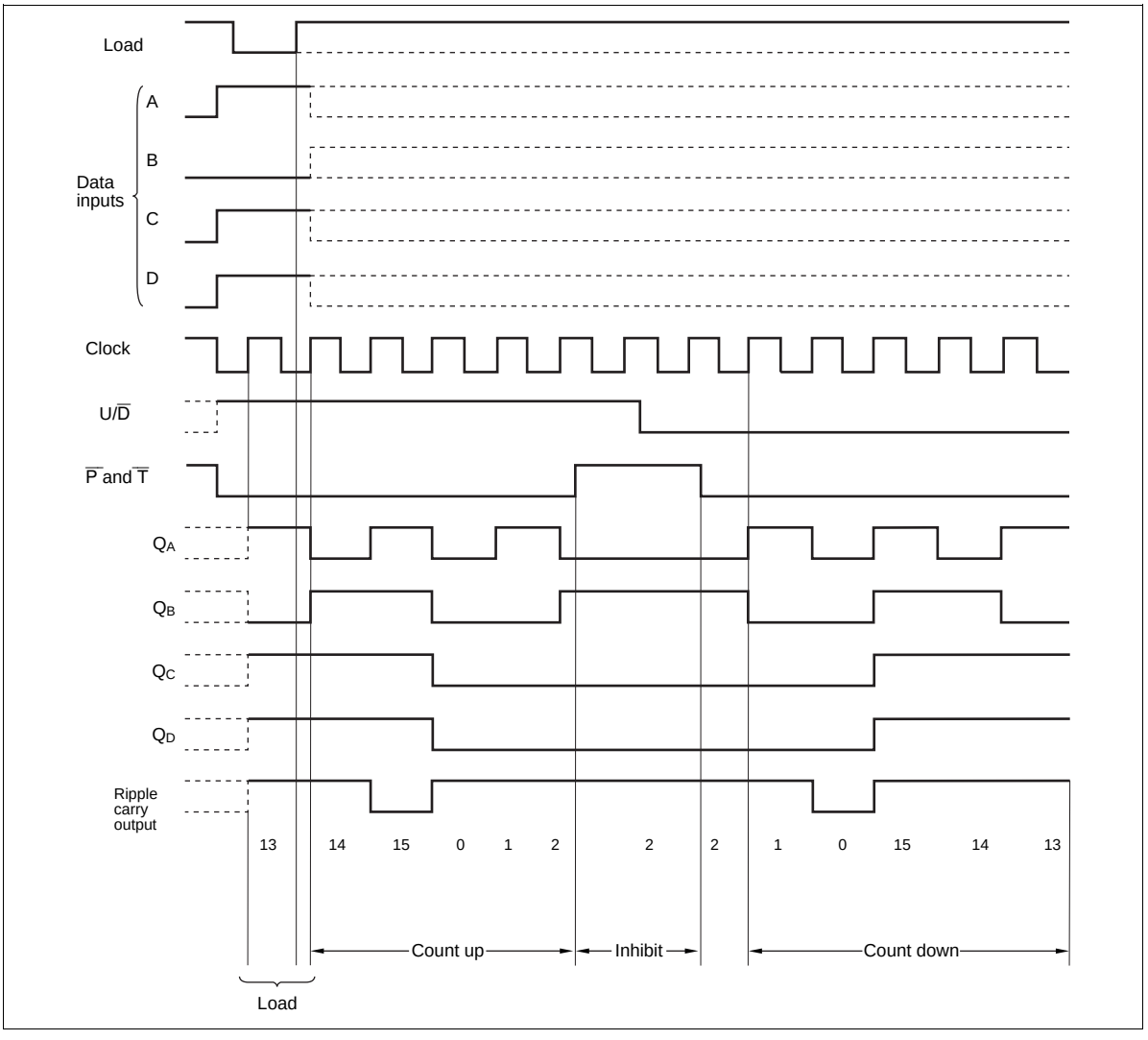

Load
A
B
Data inputs
C
D
Clock
U/$\overline{D}$
$\overline{P}$ and $\overline{T}$
Q_A
Q_B
Q_C
Q_D
Ripple carry output
13
14
15
0
1
2
2
2
1
0
15
14
13
Count up
Inhibit
Count down
Load

DC Characteristics

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

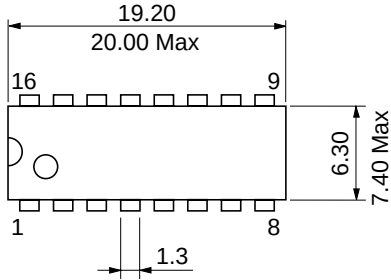
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

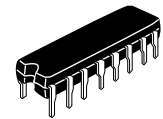
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock Frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	Clock to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	225	—	280	ns	Clock to Q
		4.5	—	—	45	—	56		
		6.0	—	—	38	—	48		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	190	ns	Enable $\overline{T}$ to Ripple carry out
		4.5	—	—	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	U/$\overline{D}$ to Ripple carry out
		4.5	—	—	40	—	50		
		6.0	—	—	34	—	43		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	150	—	—	190	—	ns	Enable $\overline{P}$, $\overline{T}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	t_{su}	2.0	150	—	—	190	—	ns	Loadk to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		
	t_{su}	2.0	150	—	—	190	—	ns	U/$\overline{D}$ to Clock
		4.5	30	—	—	38	—		
		6.0	26	—	—	33	—		

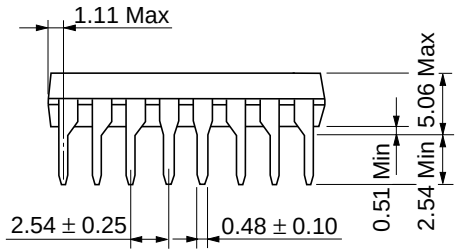
AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

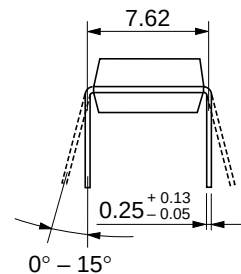
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm



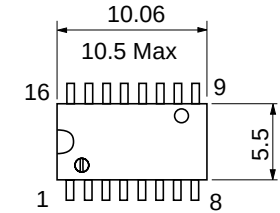


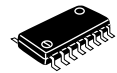


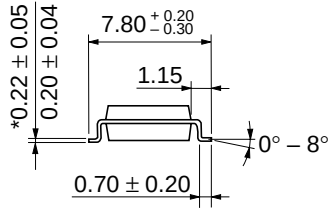


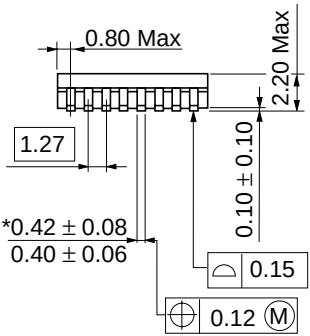
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm





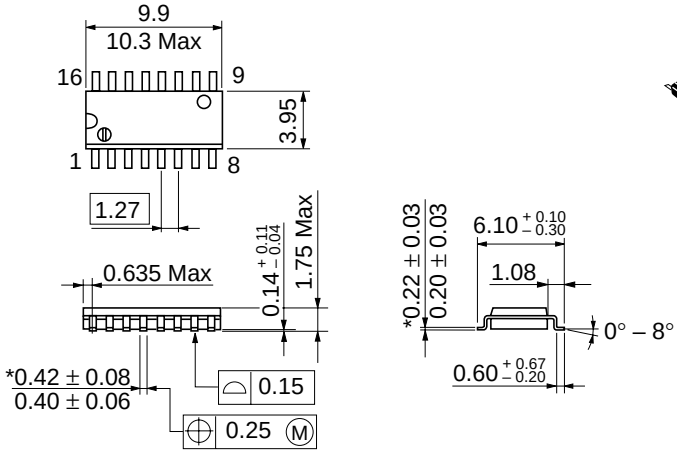


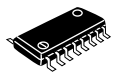


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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