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# **HD74HC74**

# Dual D-type Flip-Flops (with Preset and Clear)

REJ03D0549-0300 Rev.3.00 Oct 27, 2008

### **Description**

The flip-flop has independent data, preset, clear, and clock inputs and Q and  $\overline{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive going transition to the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

#### **Features**

• High Speed Operation:  $t_{pd}$  (Clock to Q or  $\overline{Q}$ ) = 14 ns typ ( $C_L = 50 \text{ pF}$ )

• High Output Current: Fanout of 10 LSTTL Loads

• Wide Operating Voltage:  $V_{CC} = 2 \text{ to } 6 \text{ V}$ 

• Low Input Current: 1 μA max

• Low Quiescent Supply Current:  $I_{CC}$  (static) = 2  $\mu$ A max (Ta = 25°C)

Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC74P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	Р	_
HD74HC74FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74HC74RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)
HD74HC74TELL	TSSOP-14 pin	PTSP0014JA-B (TTP-14DV)	Т	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

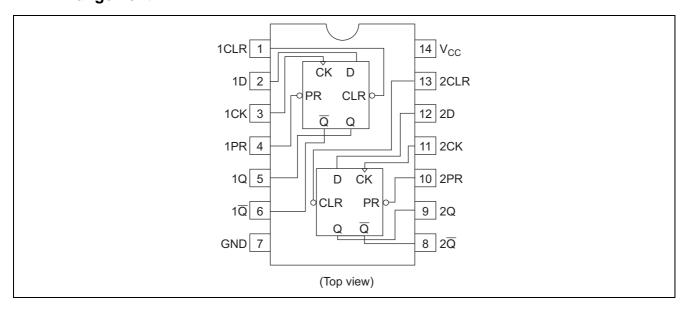
#### **Function Table**

	Inp	Out	puts		
Preset	Clear	Clock	Data	Q	Q
L	Н	Х	Х	Н	L
Н	L	Х	Х	L	Н
L	L	Х	Х	H <sup>*1</sup>	H <sup>*1</sup>
Н	Н		Н	Н	L
Н	Н		L	L	Н
Н	Н	L	Х	No c	hange
Н	Н	Н	Х	No c	hange
Н	Н	_	X	No c	hange

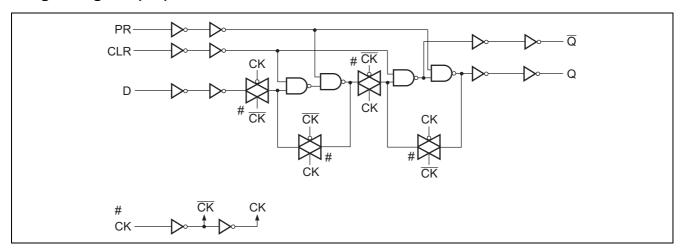
H: High levelL: Low levelX: Irrelevant

Note: 1. Q and  $\overline{Q}$  will remain High as long as Preset and Clear are Low, but Q and  $\overline{Q}$  are unpredictable, if Preset and Clear go High simultaneously.

## **Pin Arrangement**



# Logic Diagram (1/2)



# **Absolute Maximum Ratings**

ltem	Symbol	Ratings	Unit
Supply voltage range	Vcc	-0.5 to 7.0	V
Input / Output voltage	Vin, Vout	-0.5 to V <sub>CC</sub> +0.5	V
Input / Output diode current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
Output current	I <sub>0</sub>	±25	mA
V <sub>CC</sub> , GND current	I <sub>CC</sub> or I <sub>GND</sub>	±50	mA
Power dissipation	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

# **Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to V <sub>CC</sub>	V	
Operating temperature	Та	-40 to 85	°C	
		0 to 1000		V <sub>CC</sub> = 2.0 V
Input rise / fall time <sup>*1</sup>	t <sub>r</sub> , t <sub>f</sub>	0 to 500	ns	$V_{CC} = 4.5 \text{ V}$
		0 to 400		$V_{CC} = 6.0 \text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

## **Electrical Characteristics**

Item	Symbol	V <sub>cc</sub> (V)	Т	a = 25°	С	Ta = -40	to+85°C	Unit	Test Conditions	
	Syllibol	• (0 (•)	Min	Тур	Max	Min	Max	5		
		2.0	1.5	_	_	1.5	_			
	$V_{IH}$	4.5	3.15	1	_	3.15	_	V		
Input voltage		6.0	4.2	1	_	4.2	_			
input voitage		2.0	1	_	0.5	_	0.5			
	$V_{IL}$	4.5	1	_	1.35	_	1.35	V		
		6.0	1	_	1.8	_	1.8			
	V <sub>OH</sub>	2.0	1.9	2.0	_	1.9	_			
		4.5	4.4	4.5	_	4.4	_			$I_{OH} = -20 \mu A$
		6.0	5.9	6.0	_	5.9	_	V	$Vin = V_{IH} \text{ or } V_{IL}$ $I_{OH} =$	
		4.5	4.18	1	_	4.13	_			$I_{OH} = -4 \text{ mA}$
Output voltage		6.0	5.68	1	_	5.63	_			$I_{OH} = -5.2 \text{ mA}$
Output voltage	V <sub>OL</sub>	2.0	I	0.0	0.1		0.1			
		4.5	I	0.0	0.1		0.1			$I_{OL} = 20 \mu A$
		6.0	I	0.0	0.1		0.1	V	$Vin = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$	
		4.5	I	1	0.26		0.33			$I_{OL} = 4 \text{ mA}$
		6.0	I	1	0.26		0.33			$I_{OL} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1		±1.0	μΑ	$Vin = V_{CC} \text{ or } GN$	ID
Quiescent supply current	I <sub>CC</sub>	6.0	_	_	2.0	_	20	μΑ	Vin = V <sub>CC</sub> or GN	ID, lout = $0 \mu A$

# **Switching Characteristics**

 $(C_L = 50 \text{ pF, Input } t_r = t_f = 6 \text{ ns})$ 

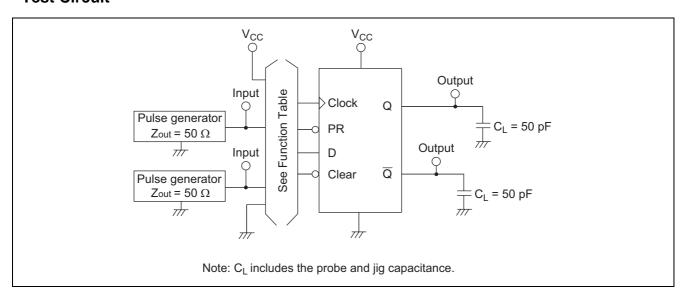
Item	Symbol	Symbol	V <sub>cc</sub> (V)	Т	a = 25°	С	Ta = -40	to +85°C	Unit	Unit	Unit	Test Conditions
iteiii	Syllibol	VCC (V)	Min	Тур	Max	Min	Max	Offic	rest conditions			
Maximum clock		2.0	_		5		4					
frequency	f <sub>max</sub>	4.5	_	35	25		20	MHz				
печасноу		6.0	_		29		24					
	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0	_		160		200		Clock to Q or Q			
		4.5	_	14	32		40	ns				
Propagation delay		6.0	_		27		34					
time		2.0	_		160		200		Preset or Clear to Q or Q			
		4.5	_	13	32		40	ns				
		6.0	_		27		34					
Setup time	t <sub>su</sub>	2.0	100		1	125						
		4.5	20	1	_	25	_	ns	Data to Clock			
		6.0	17		_	21	_					

# **Switching Characteristics**

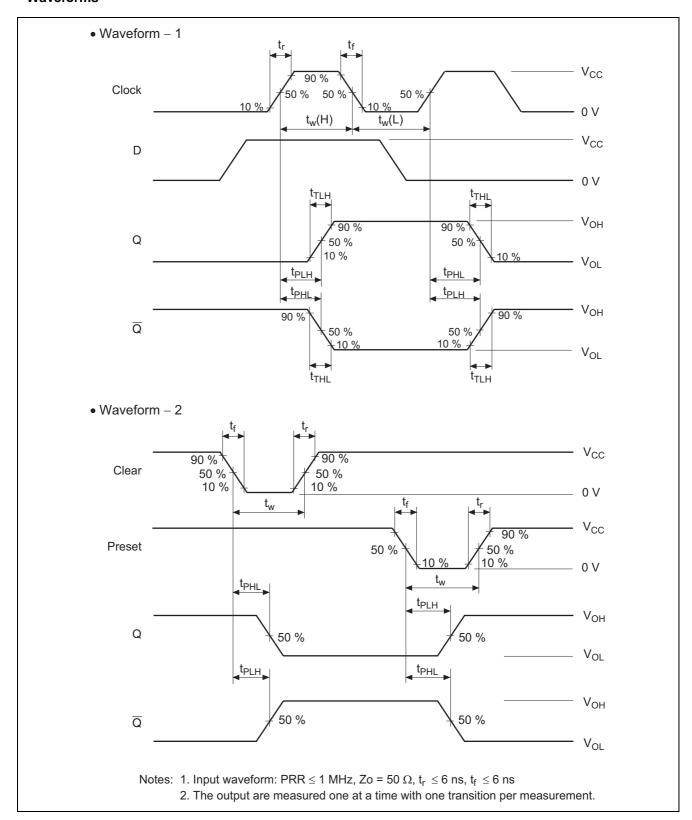
 $(C_L = 50 \text{ pF, Input } t_r = t_f = 6 \text{ ns})$ 

Item	Cymbol	Symbol	V (\( \)	Т	a = 25°	С	Ta = -40	to +85°C	Unit	Test Conditions
item	Symbol	V <sub>CC</sub> (V)	Min	Тур	Max	Min	Max	Onit	rest Conditions	
		2.0	5	_	_	5	_			
Hold time	t <sub>h</sub>	4.5	5	0	_	5	_	ns	Clock to Data	
		6.0	5	<b>-</b> 5	_	5	_			
		2.0	25	1	_	31	_		Preset, Clear to Clock	
Removal time	t <sub>rem</sub>	4.5	5	1	_	6	_	ns		
		6.0	4	1	_	5	_			
	t <sub>w</sub>	2.0	80	1	_	100	_		Clock, Preset, Clear	
Pulse width		4.5	16	8	_	20	_	ns		
		6.0	14	_	_	17	_			
Output rise/fall time	t <sub>TLH</sub> , t <sub>THL</sub>	2.0	_	_	75	_	95			
		4.5	_	5	15	_	19	ns		
		6.0		_	13		16			
Input capacitance	Cin	_		5	10	_	10	pF		

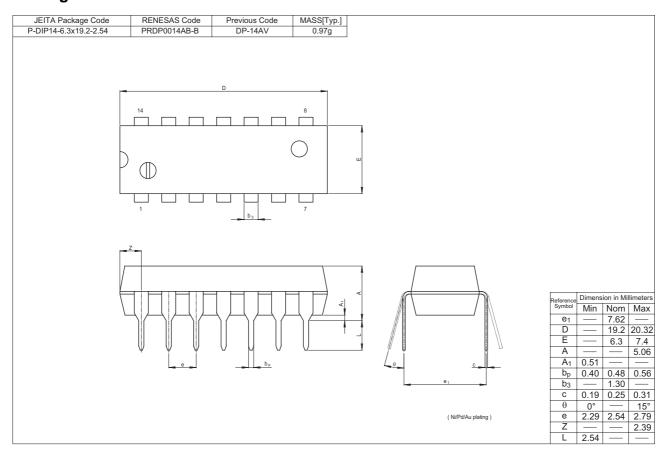
## **Test Circuit**

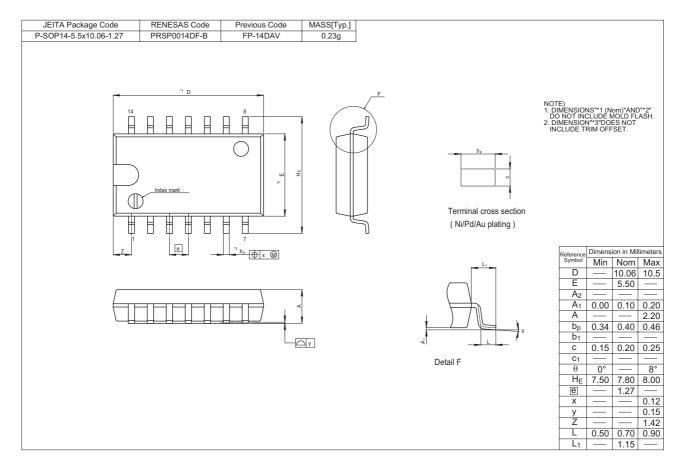


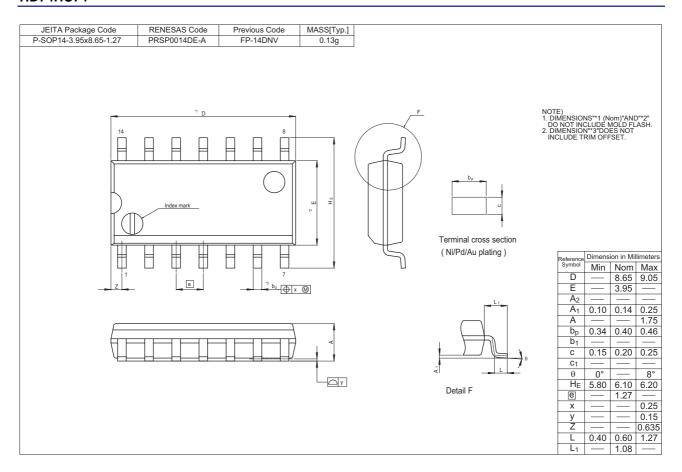
#### **Waveforms**

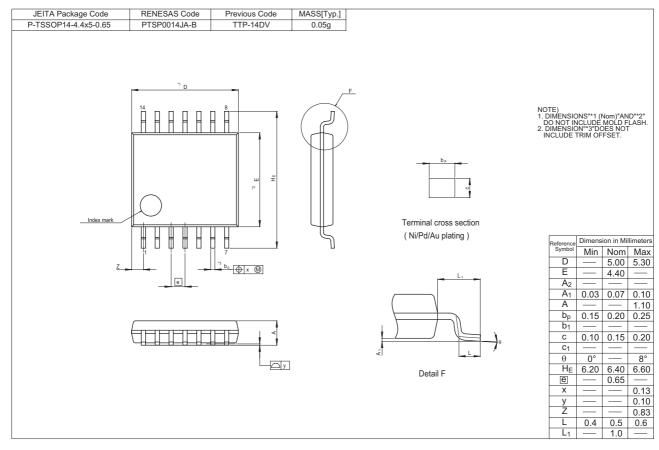


### **Package Dimensions**









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