

HD74LS109A • Dual J-K Positive-edge-triggered Flip-Flops (with Preset and Clear)

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Pulse width	Clock High	25	—	—	ns
	Preset Clear Low	25	—	—	
Setup time	"H" Data	20↑	—	—	ns
	"L" Data	20↑	—	—	
Hold time	t_h	5↑	—	—	ns

Note) ↑; The arrow indicates the rising edge.

FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	\bar{Q}_0

Notes) H; high level, L; low level, X; irrelevant

↑; transition from low to high level

Q_0 ; level of Q before the indicated steady-state conditions were established.

\bar{Q}_0 ; complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established.

*; This configuration is nonstable, that is, it will not persist where preset and clear inputs return to their inactive (high) level.

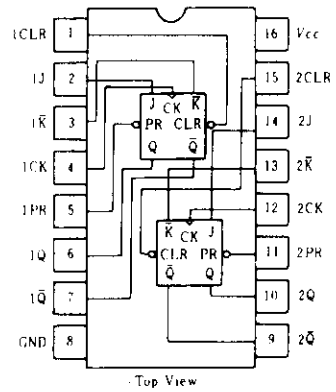
ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	—	—	V	
	V_{OL}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$, $V_{IL} = 0.8\text{V}$	—	—	0.5	V	
		$I_{OL} = 8\text{mA}$	—	—	0.4		
Input current	J, \bar{K} , CK CLR, PR	I_{IH}	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$	—	—	20	μA
	J, \bar{K} , CK CLR, PR	I_{IL}	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$	—	—	0.4	
	J, \bar{K} , CK CLR, PR	I_i	$V_{CC} = 5.25\text{V}$, $V_I = 7\text{V}$	—	—	0.1	mA
	J, \bar{K} , CK CLR, PR	I_i	$V_{CC} = 5.25\text{V}$, $V_I = 7\text{V}$	—	—	0.2	
	Short-circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA
Supply current **	I_{CC}	$V_{CC} = 5.25\text{V}$	—	4	8	mA	
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}$, $I_{IN} = -18\text{mA}$	—	—	-1.5	V	

* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

PIN ARRANGEMENT



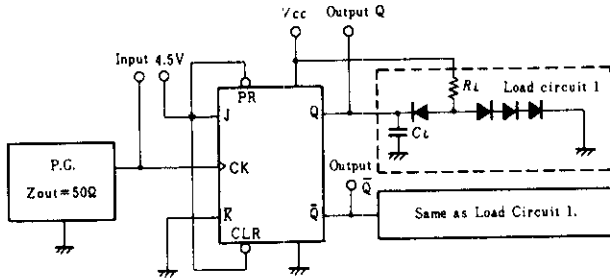
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	25	33	—	MHz
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, \bar{Q}		—	13	25	ns
	t_{PHL}				—	25	40	ns

TESTING METHOD

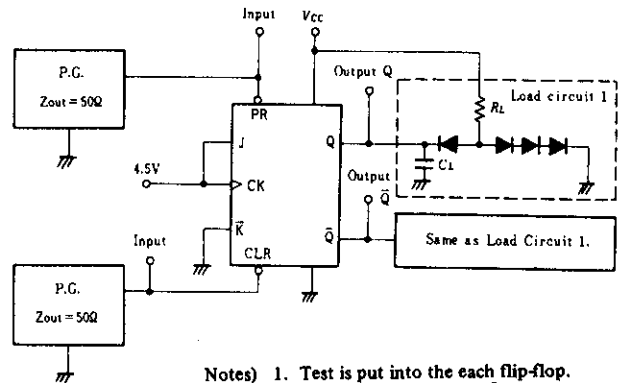
1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \bar{Q})



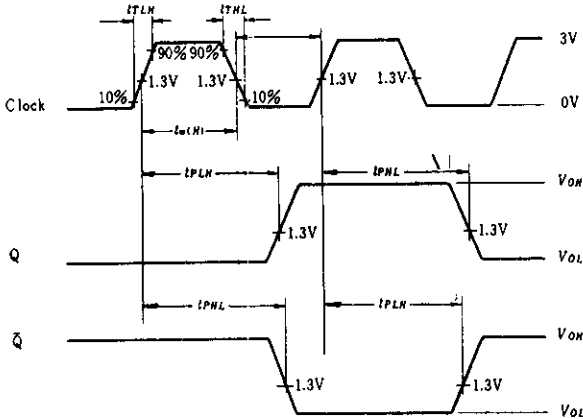
- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

1.2) t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})

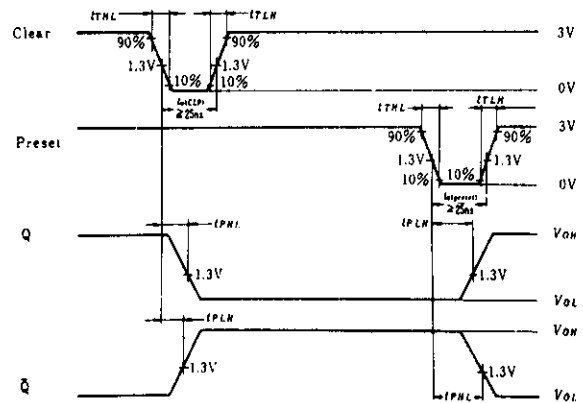


- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

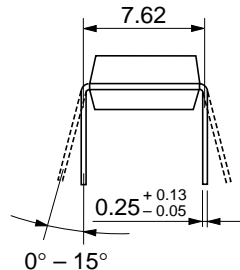
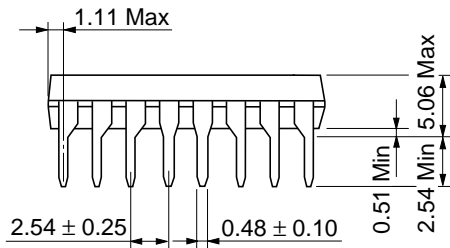
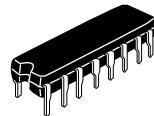
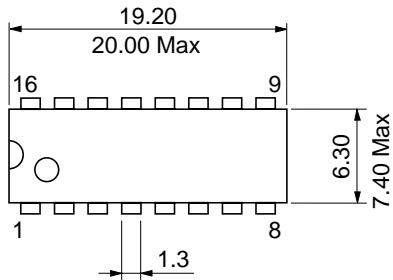
Waveform



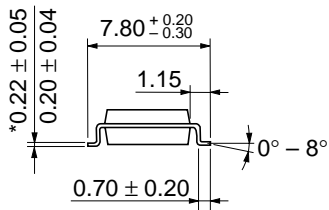
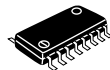
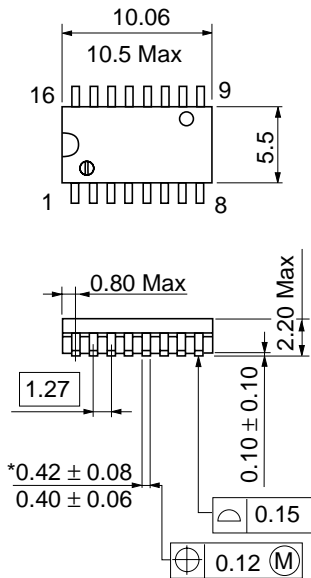
Note) Clock input pulse: $t_{TLH} \leq 15ns$, $t_{TLN} \leq 6ns$, $PRR=1MHz$, duty cycle=50% and: for f_{max} , $t_{TLH} = t_{TLN} \leq 2.5ns$.



Note) Clear and preset input pulse: $t_{TLH} \leq 15ns$, $t_{TLN} \leq 6ns$, $PRR=1MHz$.

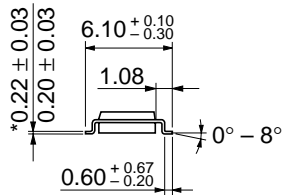
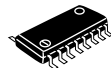
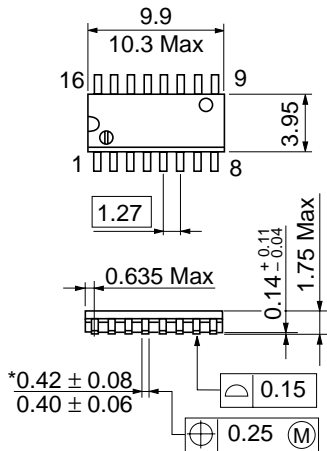


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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