

HD74LS161A

Synchronous 4-bit Binary Counter (direct clear)

REJ03D0445-0200

Rev.2.00

Feb.18.2005

This synchronous 4-bit binary counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

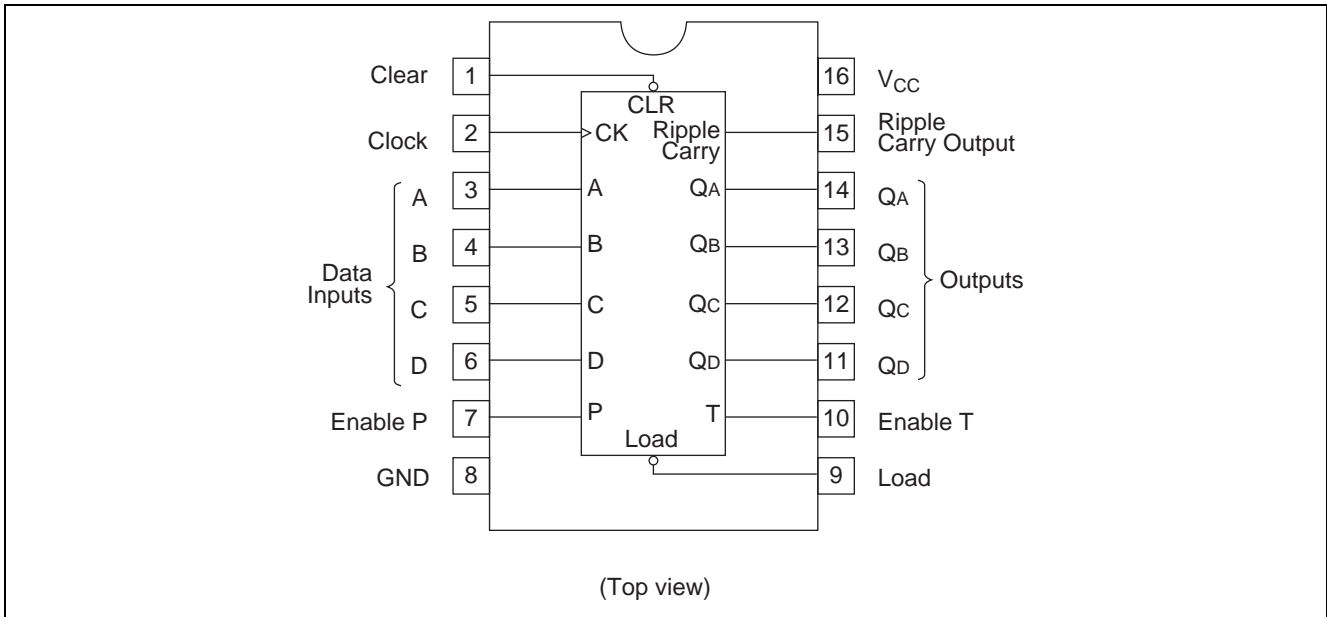
Features

- Ordering Information

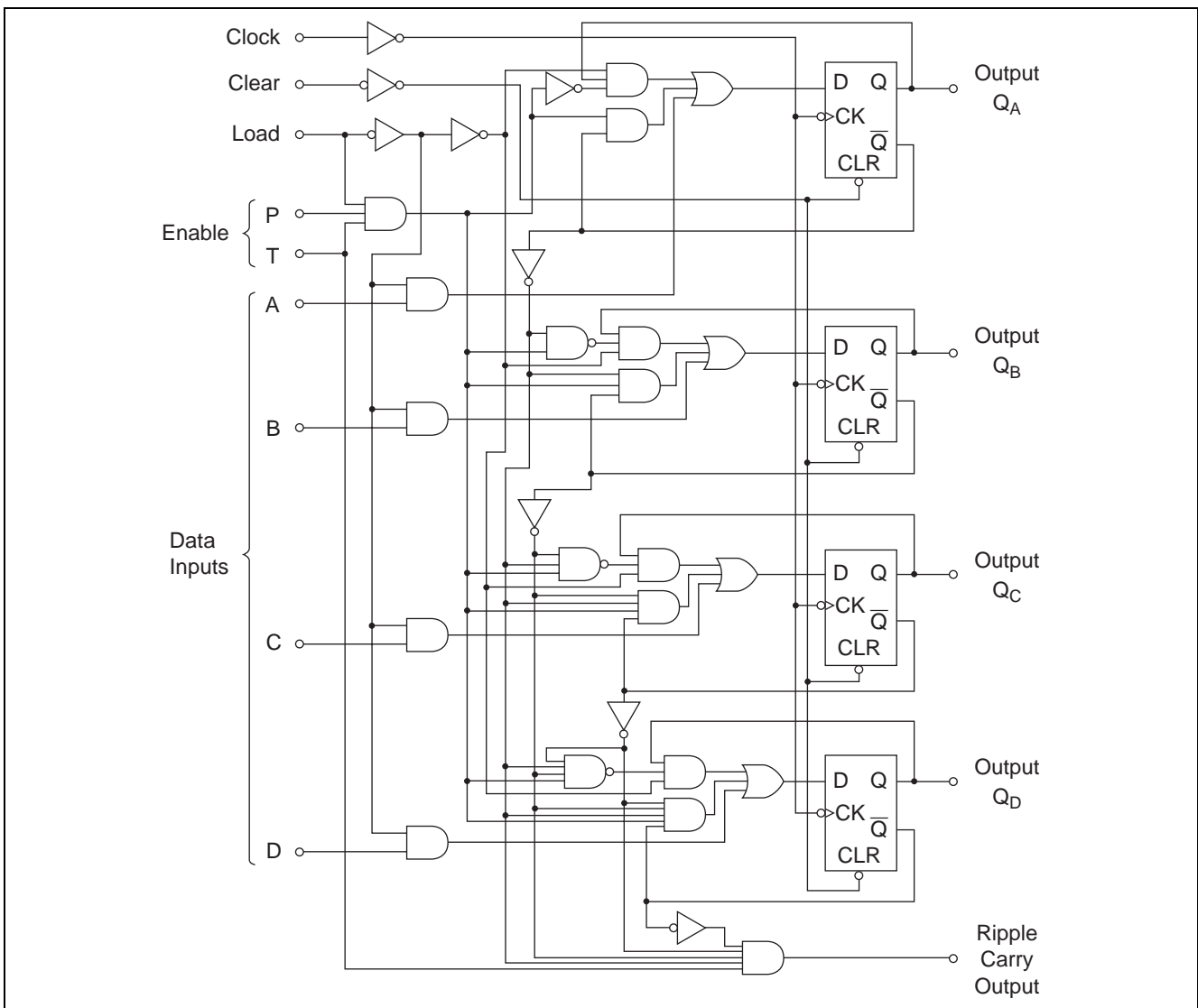
| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|----------------|--------------------|------------------------------|----------------------|--------------------------------|
| HD74LS161AP | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74LS161AFPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |
| HD74LS161ARPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A (FP-16DNV) | RP | EL (2,500 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Block Diagram



Absolute Maximum Ratings

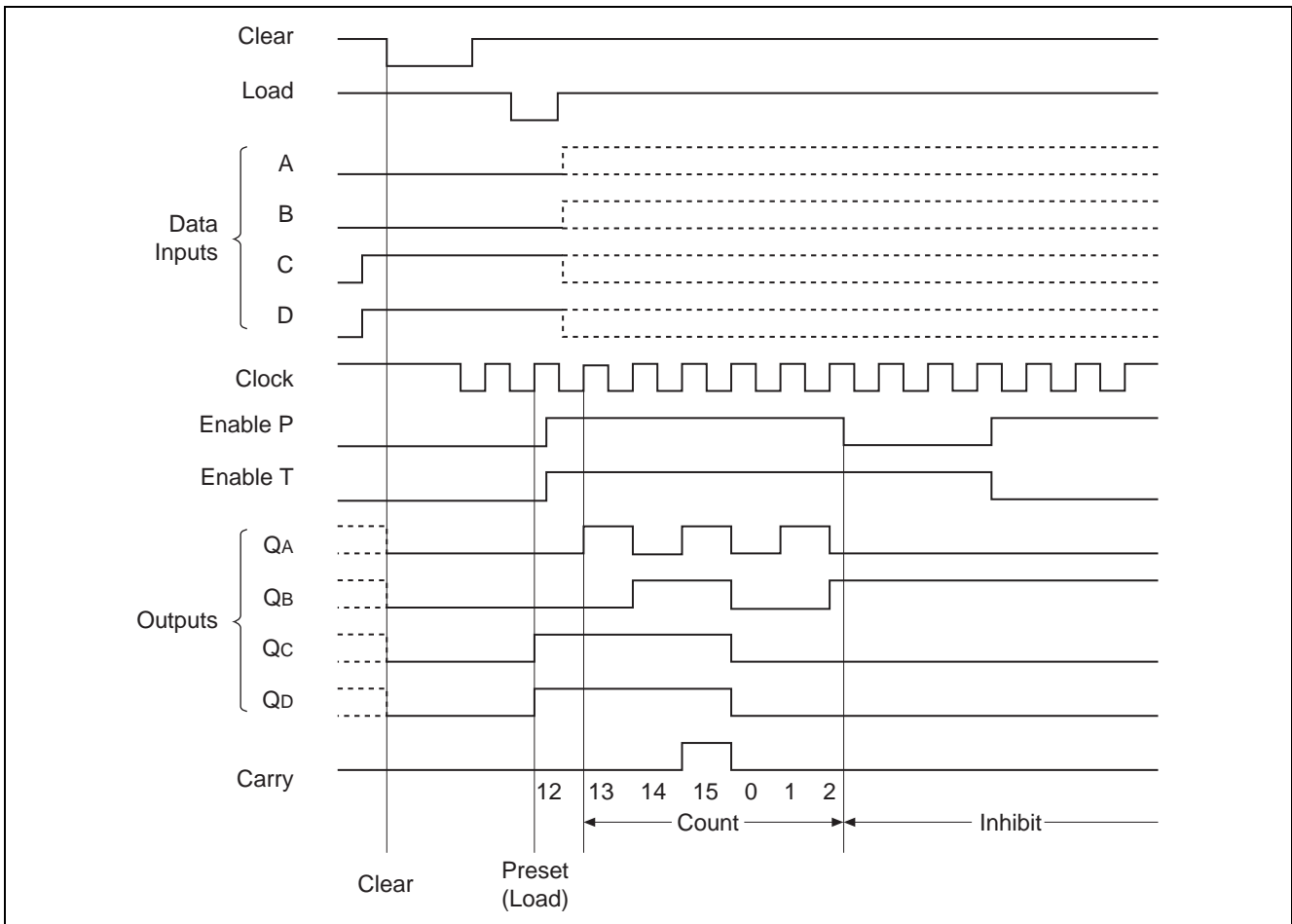
| Item | Symbol | Ratings | Unit |
|---------------------|----------|-------------|------|
| Supply voltage | V_{CC} | 7 | V |
| Input voltage | V_{IN} | 7 | V |
| Power dissipation | P_T | 400 | mW |
| Storage temperature | Tstg | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | |
|-----------------------|---------------|----------|------|------|---------|----|
| Supply voltage | V_{CC} | 4.75 | 5.00 | 5.25 | V | |
| Output current | I_{OH} | — | — | -400 | μA | |
| | I_{OL} | — | — | 8 | mA | |
| Operating temperature | Topr | -20 | 25 | 75 | °C | |
| Clock frequency | f_{clock} | 0 | — | 25 | MHz | |
| Clock pulse width | $t_w (clock)$ | 25 | — | — | ns | |
| Clear pulse width | $t_w (clear)$ | 20 | — | — | ns | |
| Setup time | A, B, C, D | t_{su} | 20 | — | — | ns |
| | Enable P, T | | 20 | — | — | ns |
| | Load | | 20 | — | — | ns |
| Hold time | t_h | 3 | — | — | ns | |

Typical Clear, Preset, and Inhibit Sequence



Electrical Characteristics

(Ta = -20 to +75 °C)

| Item | | Symbol | min. | typ.* | max. | Unit | Condition |
|------------------------------|-----------------------|------------------|------|-------|------|------|---|
| Input voltage | | V _{IH} | 2.0 | — | — | V | |
| | | V _{IL} | — | — | 0.8 | V | |
| Output voltage | | V _{OH} | 2.7 | — | — | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA |
| | | V _{OL} | — | — | 0.4 | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V |
| — | — | | 0.5 | | | | |
| Input current | Data, Enable P | I _{IH} | — | — | 20 | μA | V _{CC} = 5.25 V, V _I = 2.7 V |
| | Load, Clock, Enable T | | — | — | 40 | | |
| | Clear | | — | — | 20 | | |
| | Data, Enable P | I _{IL} | — | — | -0.4 | mA | V _{CC} = 5.25 V, V _I = 0.4 V |
| | Load, Clock, Enable T | | — | — | -0.8 | | |
| | Clear | | — | — | -0.4 | | |
| | Data, Enable P | I _I | — | — | 0.1 | mA | V _{CC} = 5.25 V, V _I = 7 V |
| | Load, Clock, Enable T | | — | — | 0.2 | | |
| | Clear | | — | — | 0.1 | | |
| Short-circuit output current | | I _{OS} | -20 | — | -100 | mA | V _{CC} = 5.25 V |
| Supply current** | | I _{CCH} | — | 18 | 31 | mA | V _{CC} = 5.25 V |
| | | I _{CCL} | — | 19 | 32 | mA | V _{CC} = 5.25 V |
| Input clamp voltage | | V _{IK} | — | — | -1.5 | V | V _{CC} = 4.75 V, I _{IN} = -18 mA |

Notes: * V_{CC} = 5 V, Ta = 25°C

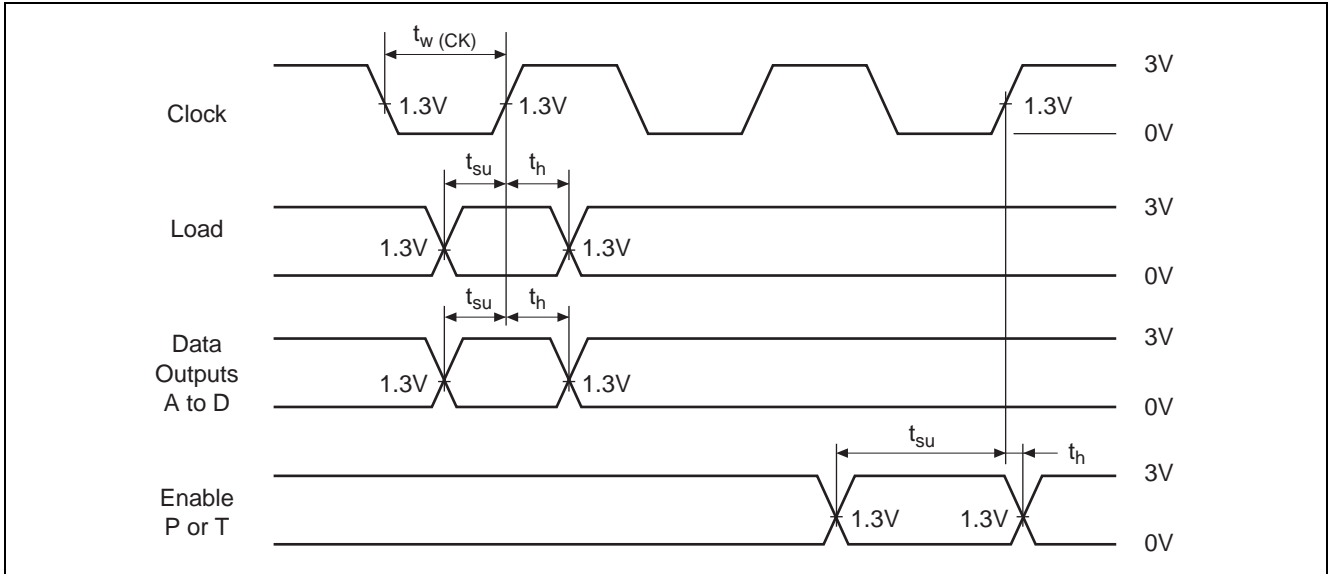
** I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

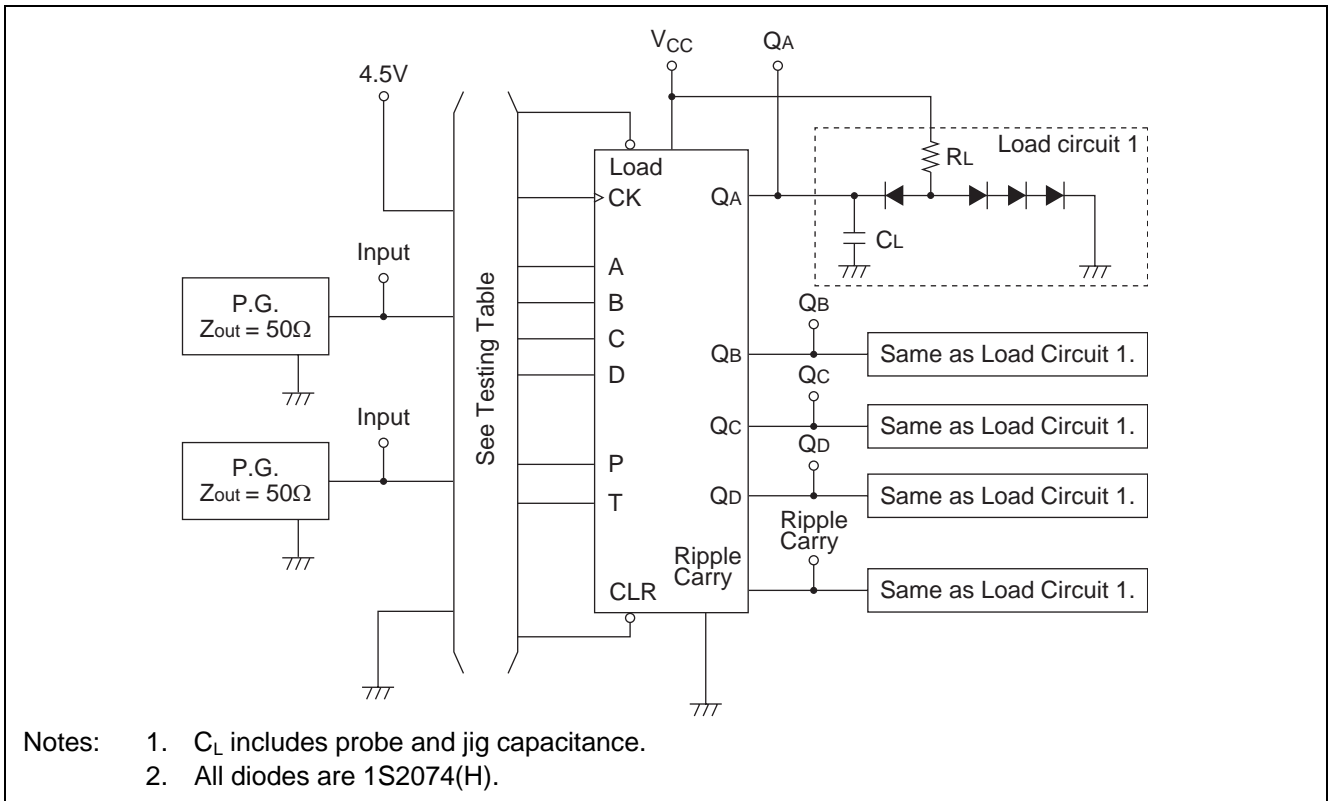
| Item | Symbol | Inputs | Outputs | min. | typ. | max. | Unit | Condition | |
|-------------------------|------------------|----------------------------------|----------------------------------|-------|------|------|------|--|----|
| Maximum clock frequency | f _{max} | Clock | Q _A to Q _D | 25 | 32 | — | MHz | | |
| Propagation delay time | t _{PLH} | Clock | Ripple | — | 20 | 35 | ns | C _L = 15 pF, R _L = 2 kΩ | |
| | t _{PHL} | | | — | 18 | 35 | | | |
| | t _{PLH} | Clock (Load = "H") | Q _A to Q _D | — | 13 | 24 | ns | | |
| | t _{PHL} | | | — | 18 | 27 | | | |
| | t _{PLH} | Clock (Load = "L") | Q _A to Q _D | — | 13 | 24 | ns | | |
| | t _{PHL} | | | — | 18 | 27 | | | |
| | t _{PLH} | Enable T | Ripple | Carry | — | 9 | 14 | | ns |
| | t _{PHL} | | | | — | 9 | 14 | | |
| t _{PHL} | Clear | Q _A to Q _D | — | 20 | 28 | ns | | | |

Timing Method



Testing Method

Test Circuit



Testing Table

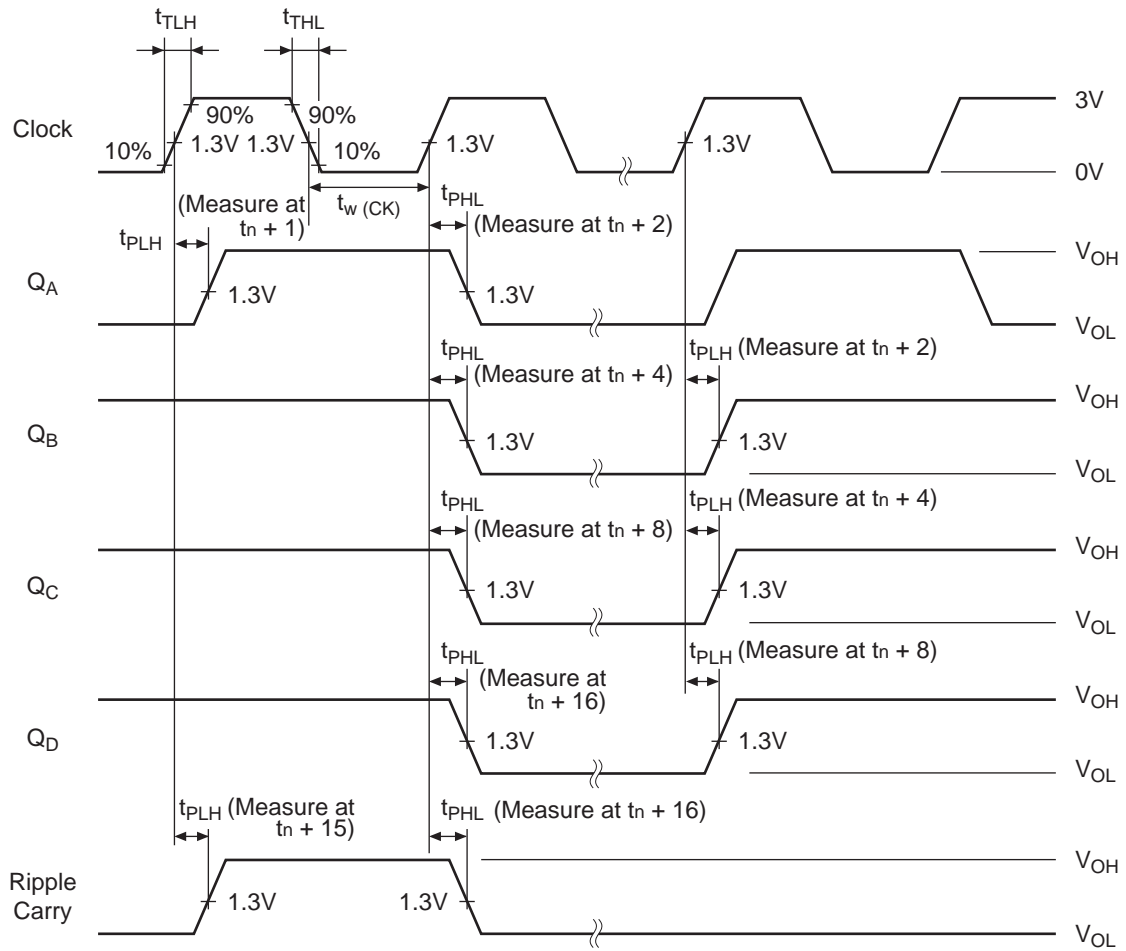
| Item | From input to output | Inputs | | | | | | | | |
|------------------------|----------------------------|--------|------|--------|------|-------|------|------|------|------|
| | | Clear | Load | Enable | | Clock | Data | | | |
| | | | | P | T | | A | B | C | D |
| f_{max} | | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND |
| t_{PLH} t_{PHL} | CK Ripply → Carry | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND |
| | CK → Q | 4.5V | 4.5V | 4.5V | 4.5V | IN | GND | GND | GND | GND |
| | CK → Q | 4.5V | GND | GND | GND | IN | IN* | IN* | IN* | IN* |
| | Enable T → Ripple Carry | 4.5V | GND | 4.5V | IN | IN* | 4.5V | 4.5V | 4.5V | 4.5V |
| | CLR → Q | IN | GND | GND | GND | IN* | 4.5V | 4.5V | 4.5V | 4.5V |

Notes: *. For initialized

| Item | From input to output | Outputs | | | | |
|------------------------|-----------------------|----------------|----------------|----------------|----------------|--------------|
| | | Q _A | Q _B | Q _C | Q _D | Ripple Carry |
| f_{max} | | OUT | OUT | OUT | OUT | OUT |
| t_{PLH} t_{PHL} | CK→Ripple Carry | — | — | — | — | OUT |
| | CK→Q | OUT | OUT | OUT | OUT | — |
| | CK→Q | OUT | OUT | OUT | OUT | — |
| | Enable T→Ripple Carry | — | — | — | — | OUT |
| | CLR→Q | OUT | OUT | OUT | OUT | — |

Waveforms 1

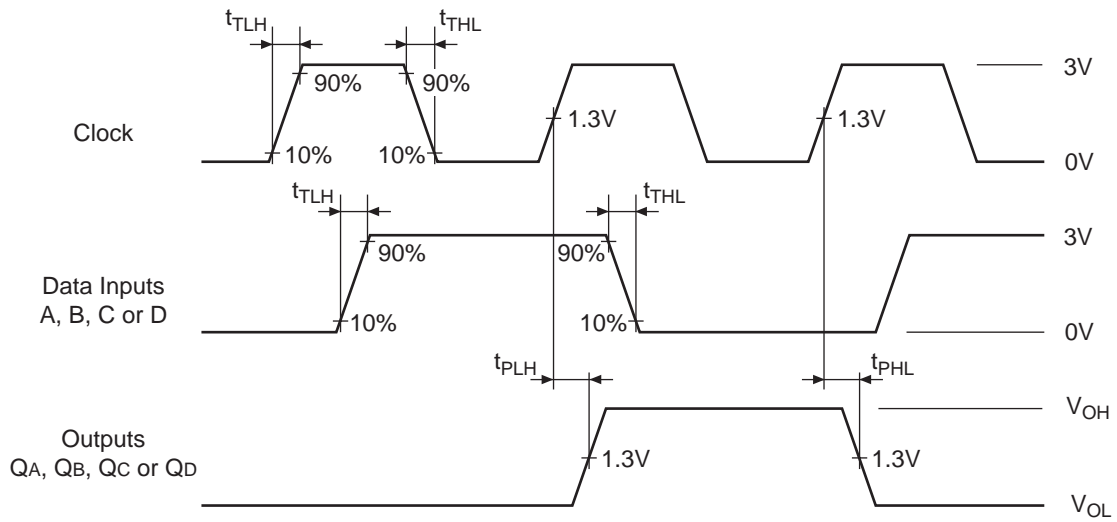
f_{max} , t_{PLH} , t_{PHL} , (Clock→Q, Ripple Carry)



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
 and : $f_{max} t_{TLH} = t_{THL} \leq 2.5$ ns.
 t_n is reference bit time when all outputs are low.

Waveforms 2

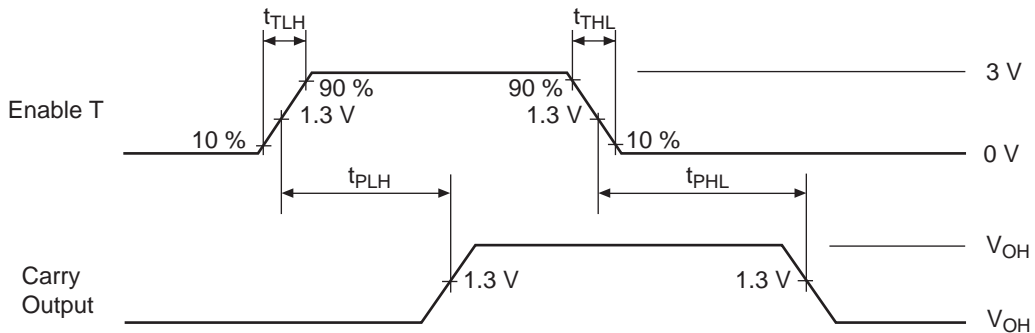
t_{PLH} , t_{PHL} , (Clock→Q)



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, Clock input: PRR = 1 MHz, duty cycle 50%, Data input: PRR = 500 kHz, duty cycle 50%

Waveforms 3

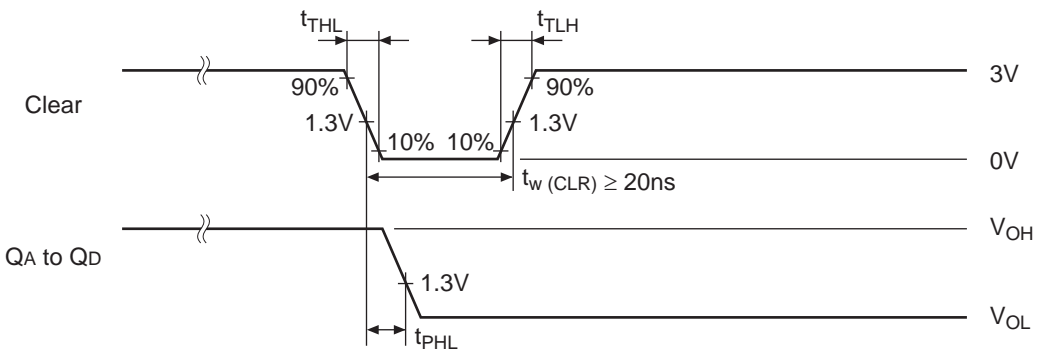
t_{PLH} , t_{PHL} , (Enable T→Ripple Carry)



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

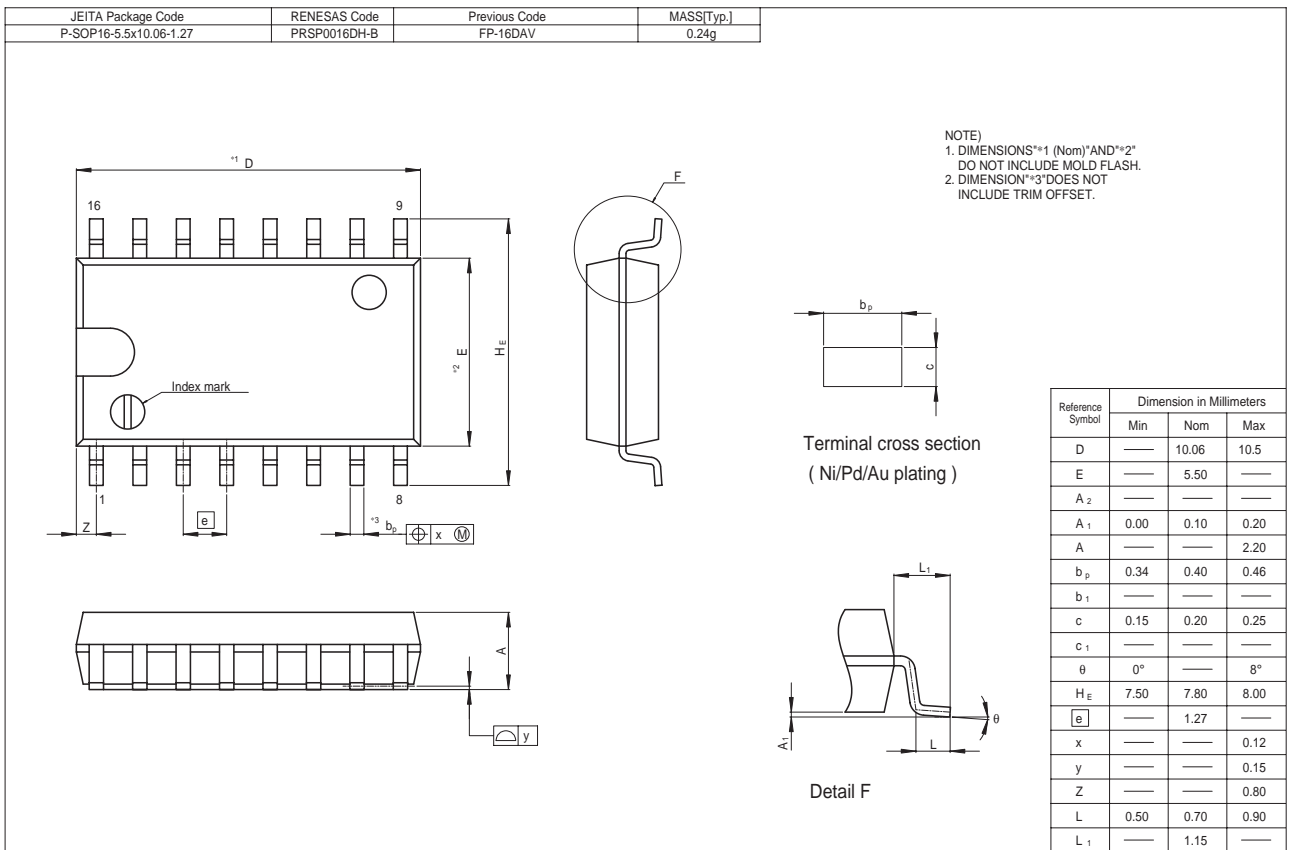
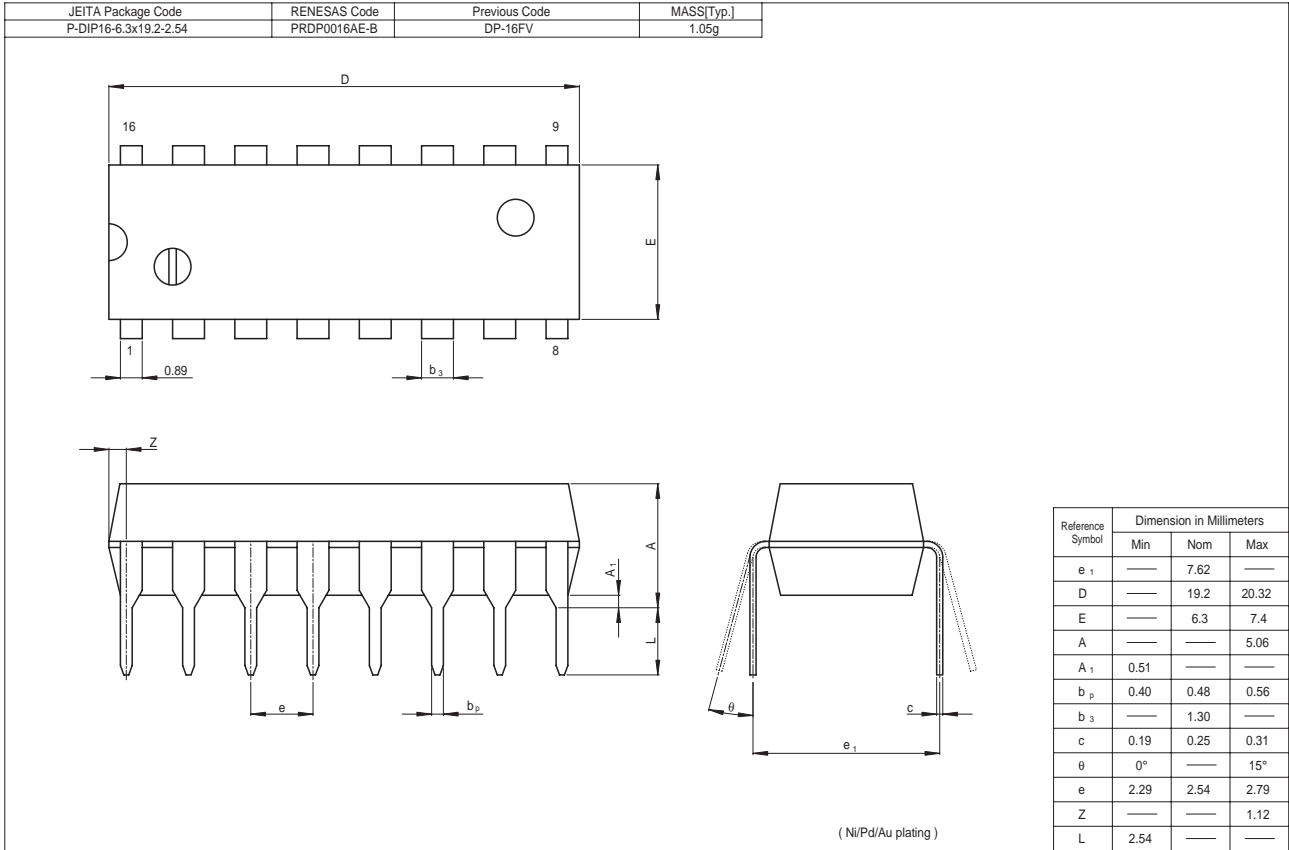
Waveforms 4

t_{PHL} , (Clear→Q)



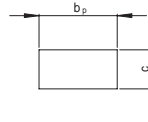
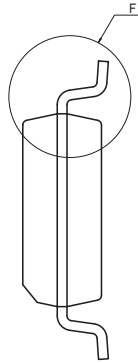
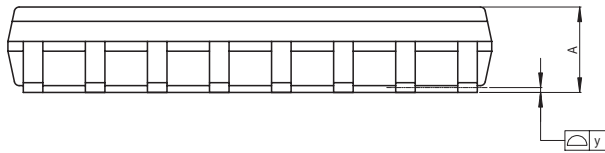
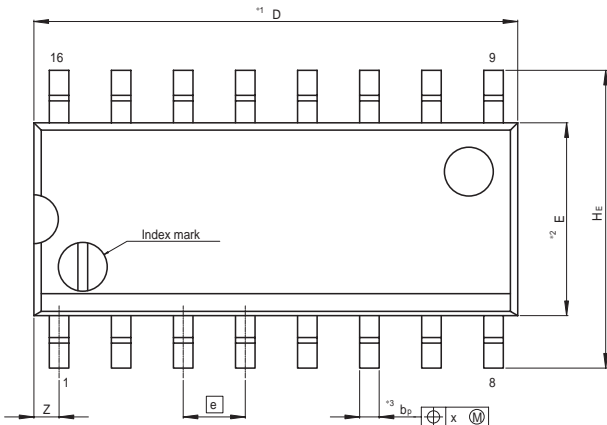
Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns

Package Dimensions

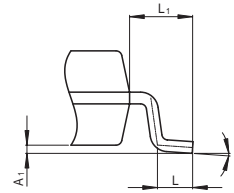


HD74LS161A

| | | | |
|---|------------------------------|---------------------------|---------------------|
| JEITA Package Code P-SOP16-3.95x9.9-1.27 | RENESAS Code PRSP0016DG-A | Previous Code FP-16DNV | MASS[Typ.] 0.15g |
|---|------------------------------|---------------------------|---------------------|



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS *1 (Nom) *2 AND *3
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3 DOES NOT
INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|-------|
| | Min | Nom | Max |
| D | — | 9.90 | 10.30 |
| E | — | 3.95 | — |
| A ₂ | — | — | — |
| A ₁ | 0.10 | 0.14 | 0.25 |
| A | — | — | 1.75 |
| b _p | 0.34 | 0.40 | 0.46 |
| b ₁ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 5.80 | 6.10 | 6.20 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.15 |
| Z | — | — | 0.635 |
| L | 0.40 | 0.60 | 1.27 |
| L ₁ | — | 1.08 | — |

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