HD74LS166A ●8-bit Shift Registers

The inputs are buffered to lower the drive requirements to one series 74 or 74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design. This parallel-in or serial-in, serial-out shift register has a complexity of 77 equivalent gates on a monolithic chip. This device features gated clock inputs and an overriding clear input.

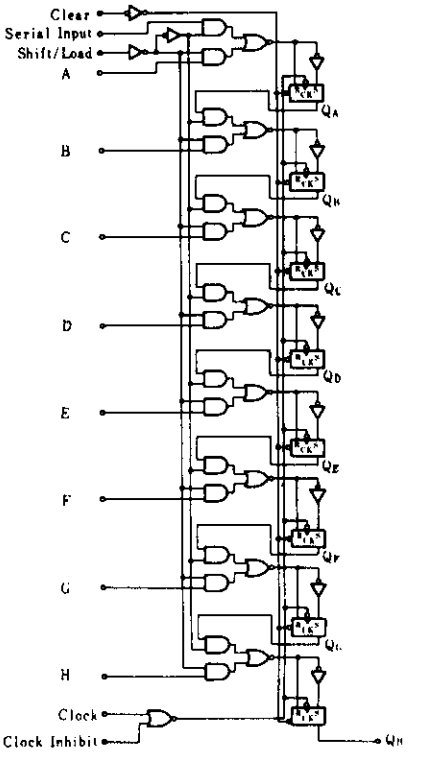
The parallel-in or serial-in modes are established by the shift/load input.

When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

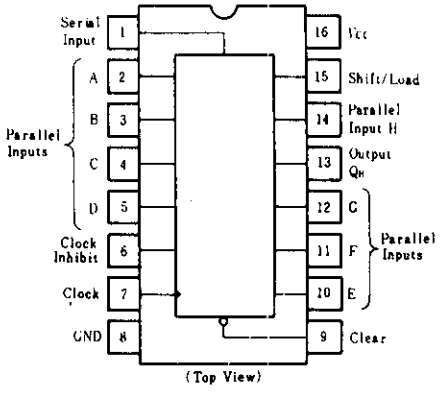
Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input.

This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overides all other inputs, including the clock, and sets all flip-flops to zero.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs						Internal Outputs		Outputs
Clear	Shift Load	Clock Inhibit	Clock	Serial	Parallel A……H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a……h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~h; the level of steady-state input at inputs A to H respectively
5. Q_{A0}~Q_{H0}; the level of Q_A to Q_H, respectively, before the indicated steady-state input conditions were established.
6. Q_{An}~Q_{Hn}; the level of Q_A to Q_H, respectively, before the most recent ↓ transition of the clock.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	nom	max	Unit
High level output current	I_{OH}	–	–	−400	μA
Low level output current	I_{OL}	–	–	8	mA
Clock frequency	f_{clock}	0	–	25	MHz
Clock and clear pulse width	t_w	20	–	–	ns
Mode control seup time	t_{su}	30	–	–	ns
Data setup time	t_{su}	20	–	–	ns
Hold time	t_h	0	–	–	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V_{IH}		2.0	—	—	V
	V_{IL}		—	—	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IH}=0.8V$, $I_{OH}=-400\mu A$	2.7	—	—	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=4mA$	—	—	0.4	V
		$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OL}=8mA$	—	—	0.5	V
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$	—	—	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$	—	—	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$	—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$	−20	—	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$	—	20	32	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$	—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

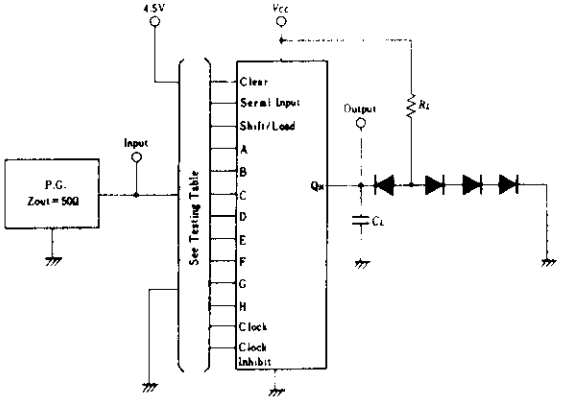
** With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}		$C_L=15pF$, $R_L=2k\Omega$	25	35	—	MHz
Propagation delay time	t_{PHL}	Clear		—	19	30	ns
	t_{PHL}	Clock		7	14	25	ns
	t_{PLH}			5	11	20	ns

■TESTING METHOD

1) Test Circuit

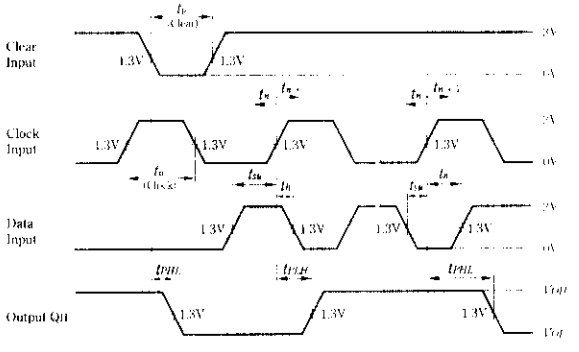


Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

2) Testing Table

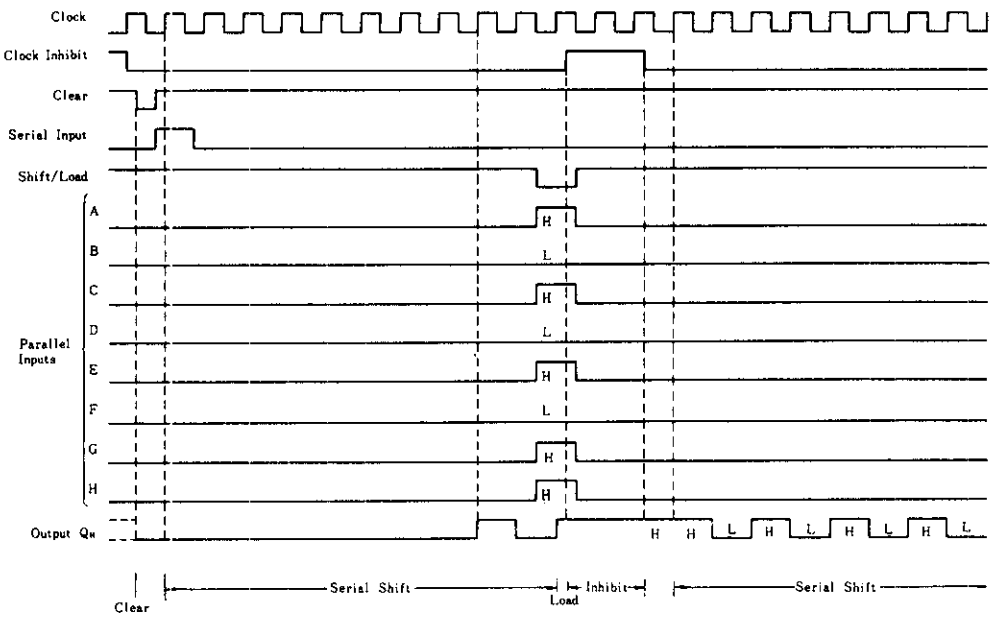
Data inputs	Shift/Load	Output	Bit time
Data H	0V	Q_H	t_{n+1}
Serial-in	4.5V	Q_H	t_{n+8}

Waveform

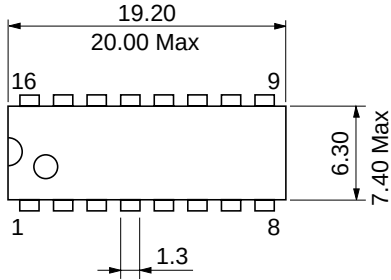


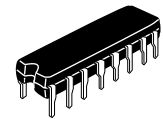
Notes) 1. Input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$, $PRR=1MHz$
duty cycle 50%
Clock input: $t_w \geqq 20ns$
Clear input: $t_w \geqq 20ns$, $t_h=10ns$, when testing f_{max}, vary the clock PRR.
2. Propagation delay time (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
3. t_n; bit time before clocking transition.
t_{n+1}; bit time after one clocking transition.
t_{n+8}; bit time after eight clocking transition.

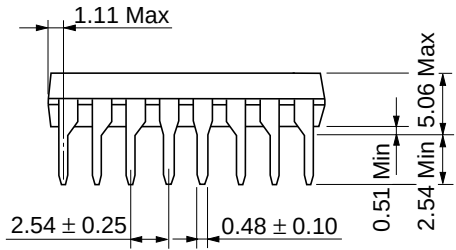
■TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES

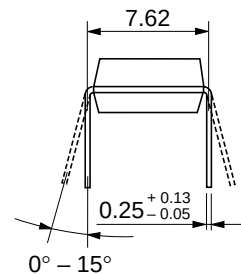


Unit: mm



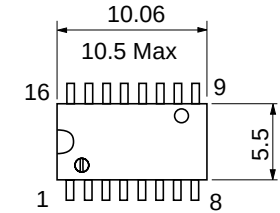


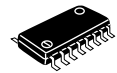


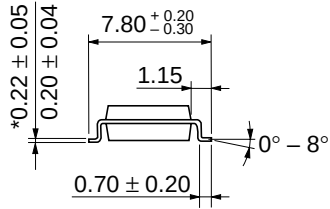


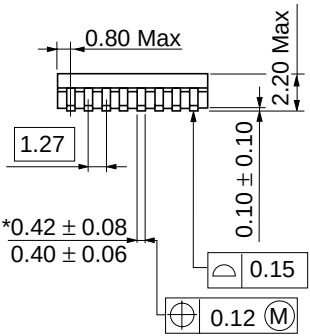
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm









*Dimension including the plating thickness
Base material dimension

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JEDEC	—
EIAJ	Conforms
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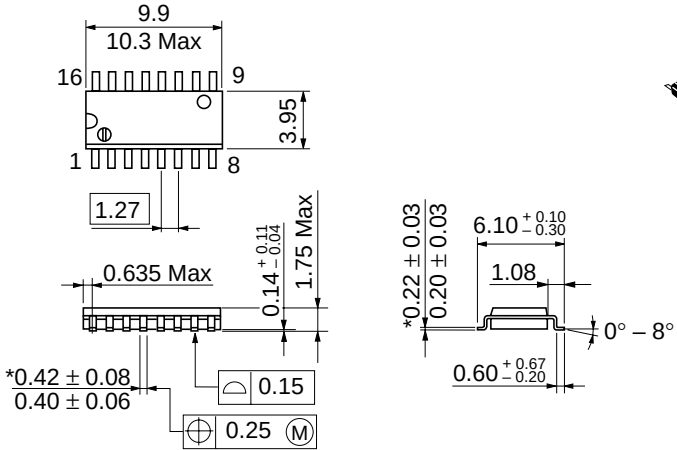
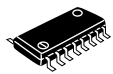
Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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