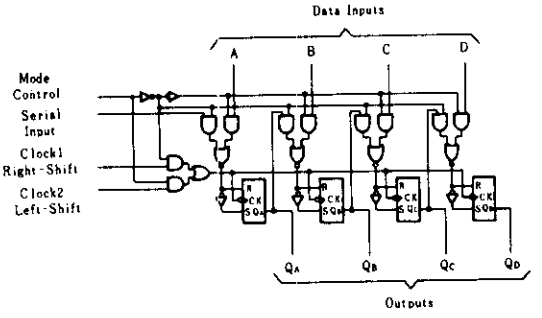
HD74LS95B ●4-bit Parallel Access Shift Registers

This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three mode operation:

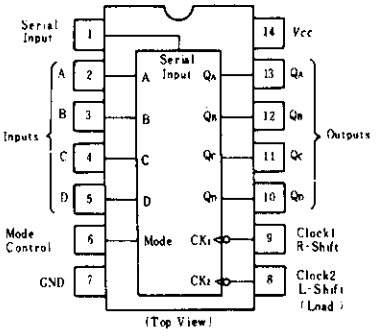
- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited. Shift right is accomplished on the high-to-low transition of clock-1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock-2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock-1 and clock-2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low: however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



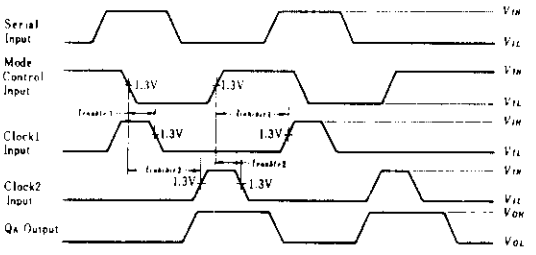
■FUNCTION TABLE

Mode Control	Clocks 2(L)	Clocks 1(↓)	Serial	Parallel A	Parallel B	Parallel C	Parallel D	Outputs Q_A	Outputs Q_B	Outputs Q_C	Outputs Q_D
H	H	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	×	×	a	b	c	d	a	b	c	d
H	↓	×	×	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	×	↓	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	×	↓	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. Q_{A0}~Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
6. Q_{An}~Q_{Dn}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent (↑) transition of the clock.
7. †; Shifting left requirs external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	$t_{w(CK)}$	25	—	—	ns
Setup time	t_{su}	20	—	—	ns
Hold time	t_h	10	—	—	ns
Enable time 1	$t_{enable\ 1}$	20	—	—	ns
Enable time 2	$t_{enable\ 2}$	20	—	—	ns
Inhibit time 1	$t_{inhibit\ 1}$	20	—	—	ns
Inhibit time 2	$t_{inhibit\ 2}$	20	—	—	ns



Clock Enable/Inhibit Times

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	—	—	V
	V_{IL}			—	—	0.8	
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	—	—	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	—	—	0.4	V
			$I_{OL}=8mA$	—	—	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		—	—	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		—	—	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		—	—	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	—	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		—	13	21	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		—	—	−1.5	V

* V_{CC}=5V, Ta=25°C

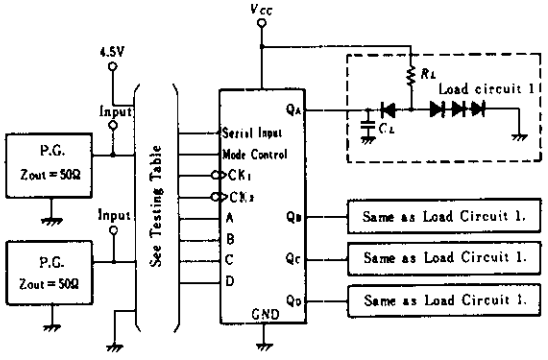
** I_{CC} is measured with all outputs and serial input open; A,B,C, and D inputs grounded; mode control at 4.5V; and momentary 3V, then ground, applied both clock inputs.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	$C_L=15pF$, $R_L=2k\Omega$	25	36	—	MHz
Propagation delay time	t_{PLH}		—	18	27	ns
	t_{PHL}		—	21	32	ns

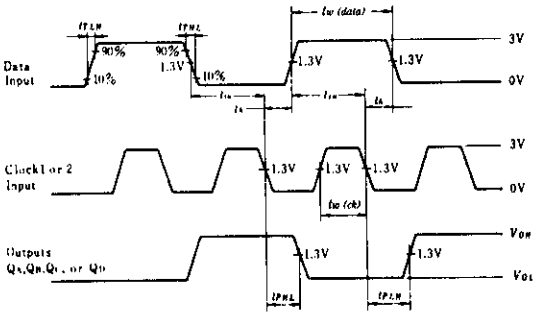
■TESTING METHOD

1) Test Circuit



Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

Waveform

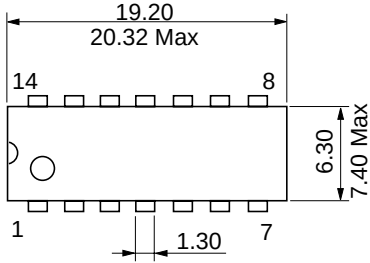


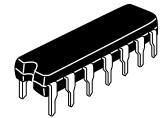
Note) 1. Input pulse: t_{TLH}, $t_{THL} \leqq 10$ns,
Data PRR=500kHz
Clock PRR=1MHz

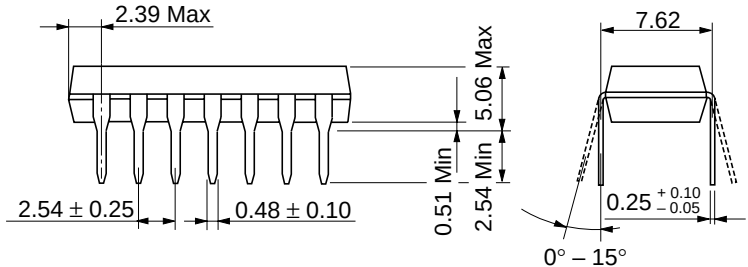
2) Testing Table

Item	From input to output	Inputs								Outputs			
		CK-1	CK-2	Mode Control	Serial Inputs	A	B	C	D	Q_A	Q_B	Q_C	Q_D
f_{max}	CK-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
	CK-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	OUT	OUT	OUT	OUT
t_{PLH}	CK-1→Q	IN	4.5V	0V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
t_{PHL}	CK-2→Q	4.5V	IN	4.5V	4.5V	IN	IN	IN	IN	OUT	OUT	OUT	OUT

Unit: mm

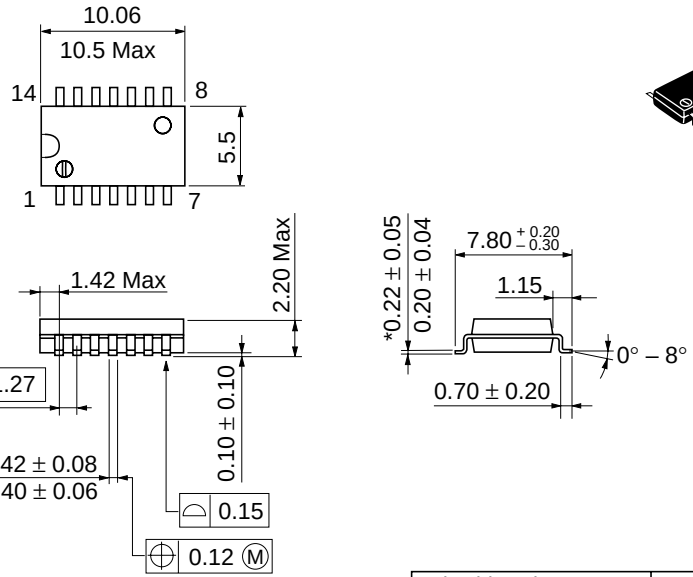


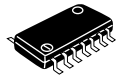




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

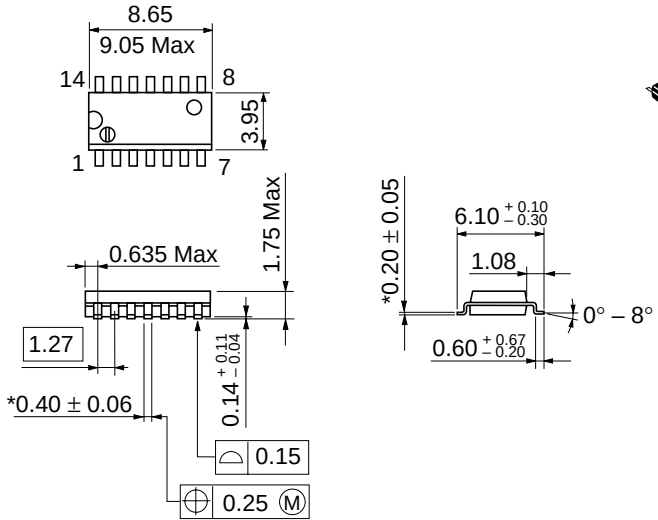




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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