To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LV595A

8-bit Shift Registers with 3-state Outputs

REJ03D0335–0200Z
(Previous ADE-205-281 (Z))
Rev.2.00
Jun. 28, 2004

Description

This device each contains an 8-bit serial-in, parallel-out shift registers that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and the storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- V_{CC} = 2.0 V to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.3 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Output current ±6 mA (@V_{CC} = 3.0 V to 3.6 V), ±12 mA (@V_{CC} = 4.5 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV595AFPEL	SOP–16 pin (JEITA)	FP–16DAV	FP	EL (2,000 pcs/reel)
HD74LV595ARPEL	SOP–16 pin (JEDEC)	FP–16DNV	RP	EL (2,500 pcs/reel)
HD74LV595ATELL	TSSOP–16 pin	TTP–16DAV	T	ELL (2,000 pcs/reel)

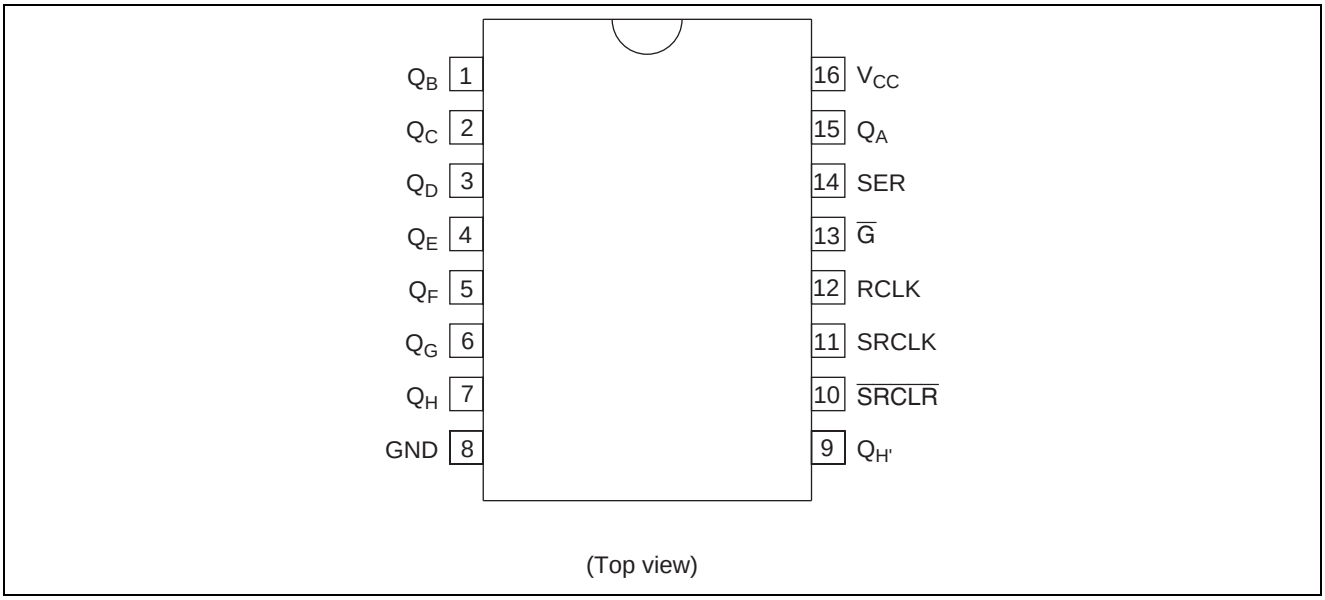
Note: Please consult the sales office for the above package availability.

Function Table

Inputs					
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{G}}$	Function
X	X	X	X	H	Force outputs into high-impedance state
X	X	X	X	L	Enable parallel output
X	X	L	X	X	Reset shift register
L	↑	H	X	X	Shift data into shift register
H	↑	H	X	X	Shift data into shift register
X	↓	H	X	X	Shift register remains unchanged
X	X	X	↑	X	Transfer shift register contents to latch register
X	X	X	↓	X	Latch register remains unchanged

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range*[1]	V_I	–0.5 to 7.0	V	
Output voltage range*[1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output: H or L
		–0.5 to 7.0		Output: Z or V_{CC}: OFF
Input clamp current	I_{IK}	–20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±70	mA	
Maximum power dissipation at Ta = 25°C (in still air)*[3]	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

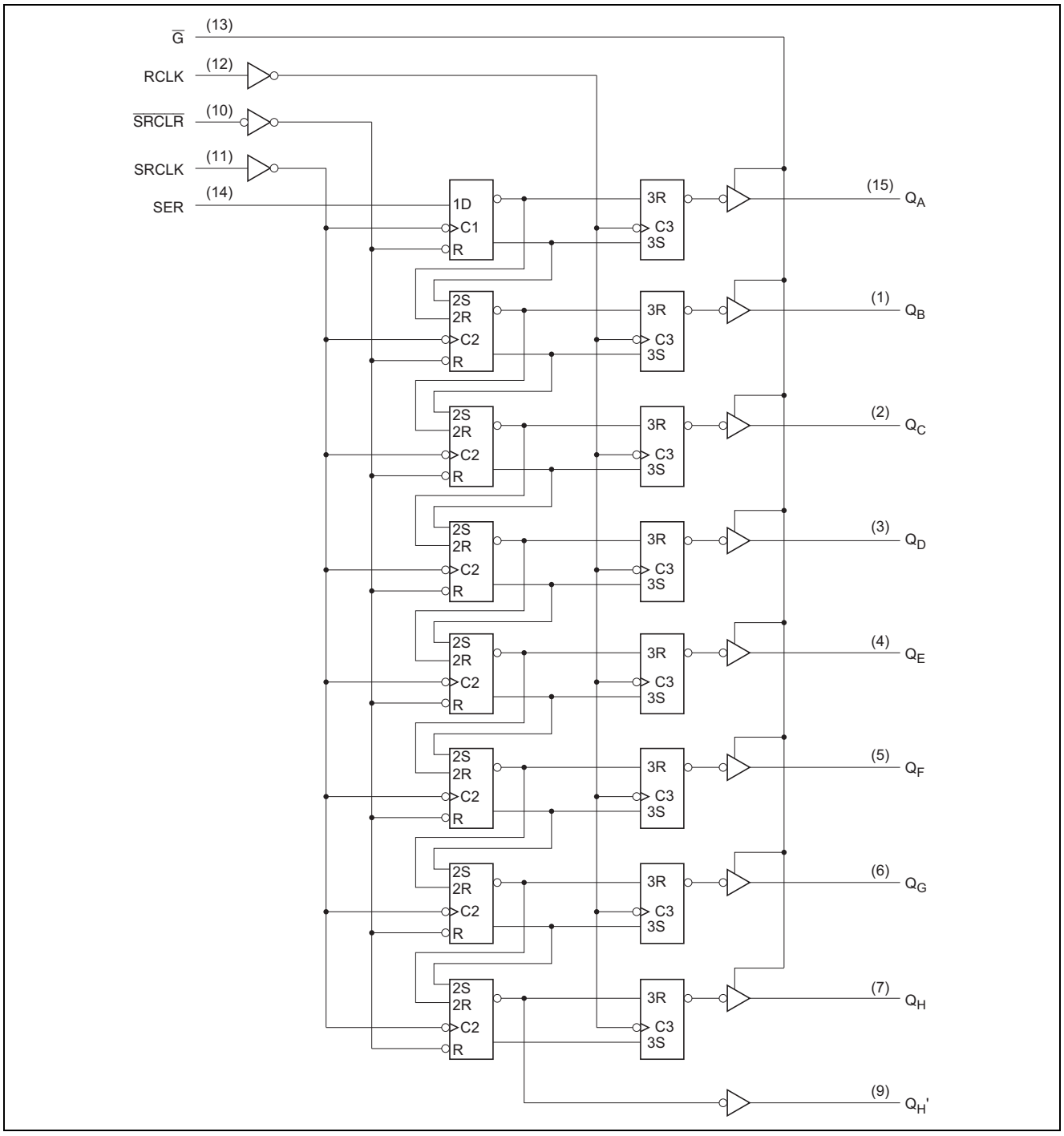
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

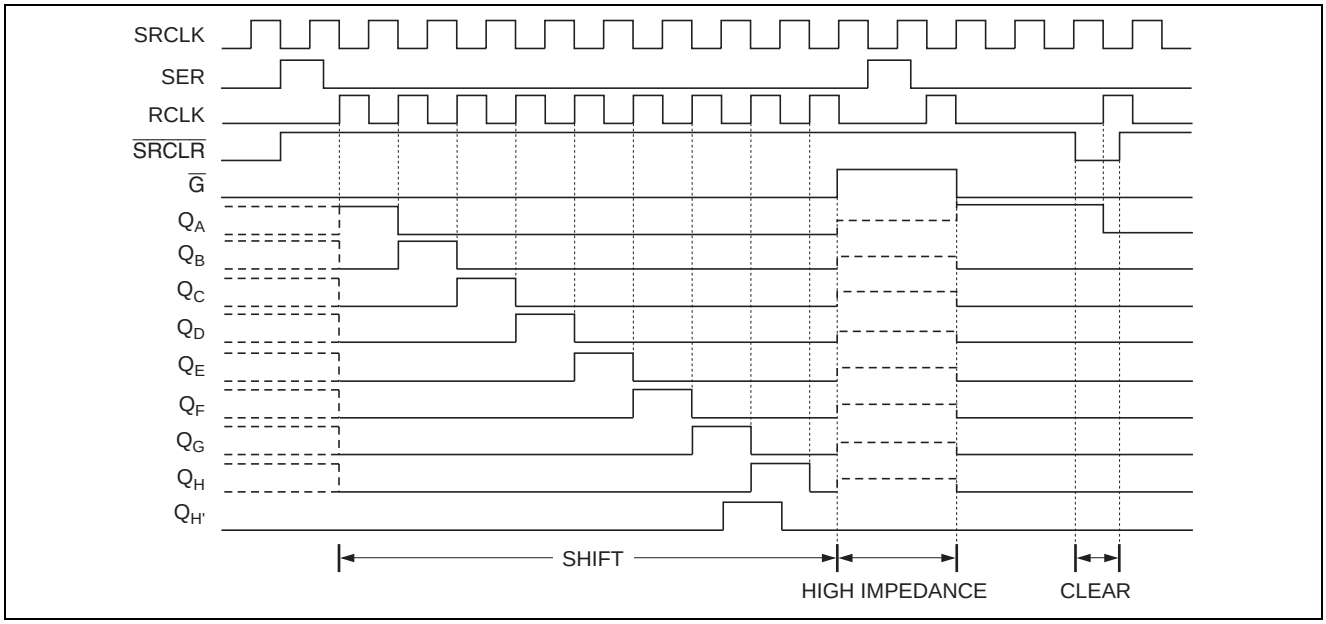
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	–50	μA	V_{CC} = 2.0 V
		—	–2	mA	V_{CC} = 2.3 to 2.7 V
		—	–6		V_{CC} = 3.0 to 3.6 V
		—	–12		V_{CC} = 4.5 to 5.5 V
	I_{OL}	—	50	μA	V_{CC} = 2.0 V
		—	2	mA	V_{CC} = 2.3 to 2.7 V
		—	6		V_{CC} = 3.0 to 3.6 V
		—	12		V_{CC} = 4.5 to 5.5 V
Input transition rise or fall rate	Δt /Δv	0	200	ns/V	V_{CC} = 2.3 to 2.7 V
		0	100		V_{CC} = 3.0 to 3.6 V
		0	20		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

Ta = –40 to 85°C

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	V_{CC} – 0.1	—	—	V	I_{OH} = –50 µA
		2.3	2.0	—	—		I_{OH} = –2 mA
		3.0	2.48	—	—		I_{OH} = –6 mA
		4.5	3.8	—	—		I_{OH} = –12 mA
	V_{OL}	Min to Max	—	—	0.1		I_{OL} = 50 µA
		2.3	—	—	0.4		I_{OL} = 2 mA
		3.0	—	—	0.44		I_{OL} = 6 mA
		4.5	—	—	0.55		I_{OL} = 12 mA
Input current	I_{IN}	0 to 5.5	—	—	±1	µA	V_{IN} = 5.5 V or GND
Off-state output current	I_{OZ}	5.5	—	—	±5	µA	V_O = V_{CC} or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	µA	V_{IN} = V_{CC} or GND, I_O = 0
Output leakage current	I_{OFF}	0	—	—	5	µA	V_I or V_O = 0 to 5.5 V
Input capacitance	C_{IN}	3.3	—	3.5	—	pF	V_I = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 2.5 ± 0.2 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	65	80	—	45	—	MHz	C_L = 15 pF		
		60	70	—	40	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	11.6	16.4	1.0	19.5	ns	C_L = 15 pF	SRCLK	Q_H'
		—	14.8	19.4	1.0	22.5		C_L = 50 pF		
		—	10.5	15.3	1.0	18.0		C_L = 15 pF	RCLK	Q_A – Q_H
		—	13.7	18.3	1.0	21.0		C_L = 50 pF		
	t_{PHL}	—	11.2	16.2	1.0	18.2		C_L = 15 pF	$\overline{SRCLK}$	Q_H'
		—	14.4	19.2	1.0	21.2		C_L = 50 pF		
Enable time	t_{ZH}	—	10.3	14.8	1.0	17.5	ns	C_L = 15 pF	$\overline{G}$	Q_A – Q_H
	t_{ZL}	—	12.2	17.7	1.0	20.5		C_L = 50 pF		
Disable time	t_{HZ}	—	7.6	11.5	1.0	13.5	ns	C_L = 15 pF		
	t_{LZ}	—	14.4	18.2	1.0	19.2		C_L = 50 pF		
Setup time	t_{SU}	5.5	—	—	5.5	—	ns		SER before SRCLK ↑	
		10.0	—	—	10.5	—			SRCLK ↑ before RCLK ↑	
		10.0	—	—	11.0	—			$\overline{SRCLR}$ low before RCLK ↑	
		5.0	—	—	5.0	—			$\overline{SRCLR}$ high (inactive) before SRCLK ↑	
Hold time	t_h	2.0	—	—	2.0	—	ns		SER after SRCLK ↑	
		0.5	—	—	0.5	—			SRCLK ↑ after RCLK ↑	
		0.5	—	—	0.5	—			$\overline{SRCLR}$ low after RCLK ↑	
Pulse width	t_w	7.0	—	—	7.5	—	ns		RCLK high or low	
		7.0	—	—	7.5	—			SRCLK high or low	
		6.0	—	—	6.5	—			$\overline{SRCLR}$ low	

Switching Characteristics (cont)

V_{CC} = 3.3 ± 0.3 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	80	150	—	70	—	MHz	C_L = 15 pF		
		55	130	—	50	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	8.8	13.0	1.0	15.0	ns	C_L = 15 pF	SRCLK	Q_H'
		—	11.3	16.5	1.0	18.5		C_L = 50 pF		
		—	7.7	11.9	1.0	13.5		C_L = 15 pF	RCLK	$Q_A – Q_H$
		—	10.2	15.4	1.0	17.0		C_L = 50 pF		
	t_{PHL}	—	8.4	12.8	1.0	13.7		C_L = 15 pF	$\overline{SRCLK}$	Q_H'
		—	10.9	16.3	1.0	17.2		C_L = 50 pF		
Enable time	t_{ZH}	—	7.5	11.5	1.0	13.5	ns	C_L = 15 pF	$\overline{G}$	$Q_A – Q_H$
	t_{ZL}	—	9.0	15.0	1.0	17.0		C_L = 50 pF		
Disable time	t_{HZ}	—	5.9	11.7	1.0	13.5	ns	C_L = 15 pF		
	t_{LZ}	—	12.1	15.7	1.0	16.2		C_L = 50 pF		
Setup time	t_{SU}	3.5	—	—	3.5	—	ns		SER before SRCLK ↑	
		8.0	—	—	8.5	—			SRCLK ↑ before RCLK ↑	
		8.0	—	—	9.0	—			$\overline{SRCLR}$ low before RCLK ↑	
		3.0	—	—	3.0	—			$\overline{SRCLR}$ high (inactive) before SRCLK ↑	
Hold time	t_h	1.5	—	—	1.5	—	ns		SER after SRCLK ↑	
		0.0	—	—	0.0	—			SRCLK ↑ after RCLK ↑	
		0.0	—	—	0.0	—			$\overline{SRCLR}$ low after RCLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		RCLK high or low	
		5.0	—	—	5.0	—			SRCLK high or low	
		5.0	—	—	5.0	—			$\overline{SRCLR}$ low	

Switching Characteristics (cont)

V_{CC} = 5.0 ± 0.5 V

Item	Symbol	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum lock frequency	f_{max}	135	185	—	115	—	MHz	C_L = 15 pF		
		95	155	—	85	—		C_L = 50 pF		
Propagation delay time	t_{PLH}/t_{PHL}	—	6.2	8.2	1.0	9.4	ns	C_L = 15 pF	SRCLK	Q_H'
		—	7.7	10.2	1.0	11.4		C_L = 50 pF		
		—	5.4	7.4	1.0	8.5		C_L = 15 pF	RCLK	$Q_A – Q_H$
		—	6.9	9.4	1.0	10.5		C_L = 50 pF		
	t_{PHL}	—	5.9	8.0	1.0	9.1		C_L = 15 pF	$\overline{SRCLK}$	Q_H'
		—	7.4	10.0	1.0	11.1		C_L = 50 pF		
Enable time	t_{ZH}	—	4.8	8.6	1.0	10.0	ns	C_L = 15 pF	$\overline{G}$	$Q_A – Q_H$
	t_{ZL}	—	8.3	10.6	1.0	12.0		C_L = 50 pF		
Disable time	t_{HZ}	—	4.8	8.6	1.0	10.0	ns	C_L = 15 pF		
	t_{LZ}	—	7.6	11.0	1.0	11.0		C_L = 50 pF		
Setup time	t_{SU}	3.0	—	—	3.0	—	ns		SER before SRCLK ↑	
		5.0	—	—	5.0	—			SRCLK ↑ before RCLK ↑	
		5.0	—	—	5.0	—			$\overline{SRCLR}$ low before RCLK ↑	
		2.5	—	—	2.5	—			$\overline{SRCLR}$ high (inactive) before SRCLK ↑	
Hold time	t_h	2.0	—	—	2.0	—	ns		SER after SRCLK ↑	
		0.0	—	—	0.0	—			SRCLK ↑ after RCLK ↑	
		0.0	—	—	0.0	—			$\overline{SRCLR}$ low after RCLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		RCLK high or low	
		5.0	—	—	5.0	—			SRCLK high or low	
		5.0	—	—	5.0	—			$\overline{SRCLR}$ low	

Output-skew Characteristics

C_L = 50 pF

Item	Symbol	V_{CC} = (V)	Ta = 25°C		Ta = –40 to 85°C		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk\ (O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

C_L = 50 pF

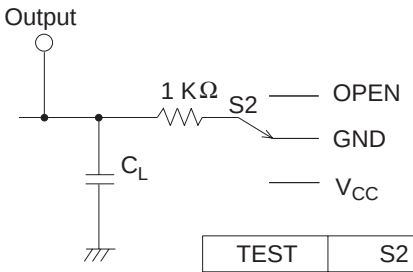
Item	Symbol	V_{CC} = (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Power dissipation capacitance	C_{PD}	3.3	—	32.7	—	pF	f = 10 MHz
		5.0	—	33.1	—		

Noise Characteristics

C_L = 50 pF

Item	Symbol	V_{CC} = (V)	Ta = 25°C Min	Typ	Max	Unit	Test Conditions
Quiet output, maximum dynamic V_{OL}	$V_{OL (P)}$	3.3	—	0.65	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL (V)}$	3.3	—	–0.59	–0.8	V	
Quiet output, minimum dynamic V_{OH}	$V_{OH (V)}$	3.3	—	2.84	—	V	
High-level dynamic input voltage	$V_{IH (D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL (D)}$	3.3	—	—	0.99	V	

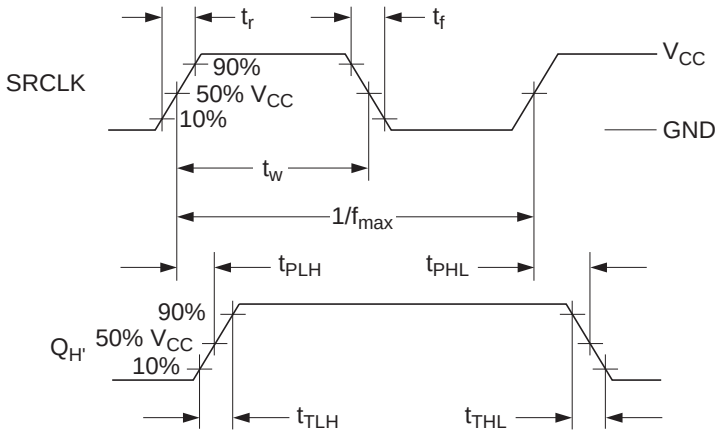
Test Circuit



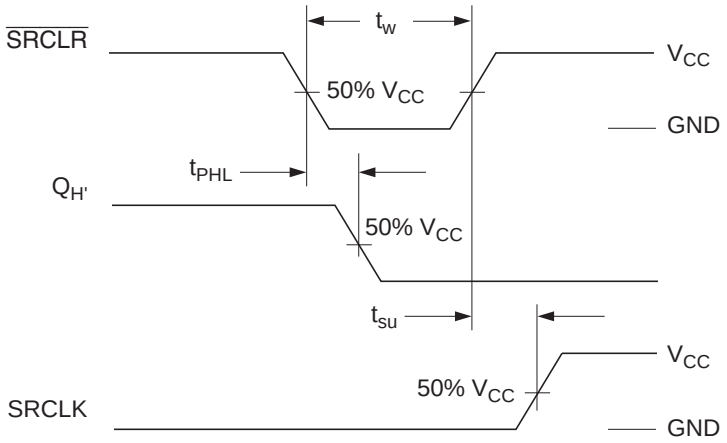
TEST	S2
t_{PLH}/ t_{PHL}	OPEN
t_{ZH}/ t_{HZ}	GND
t_{ZL}/ t_{LZ}	V_{CC}

Note: C_L includes the probe and jig capacitance.

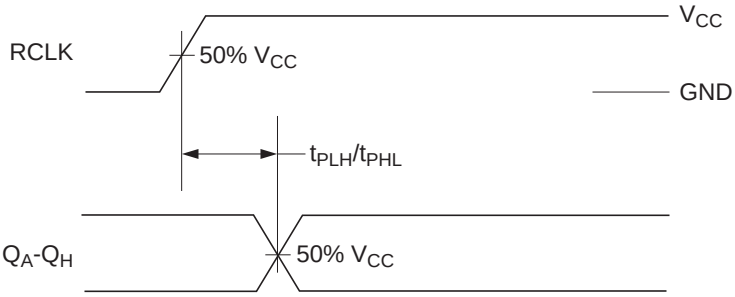
Waveform – 1



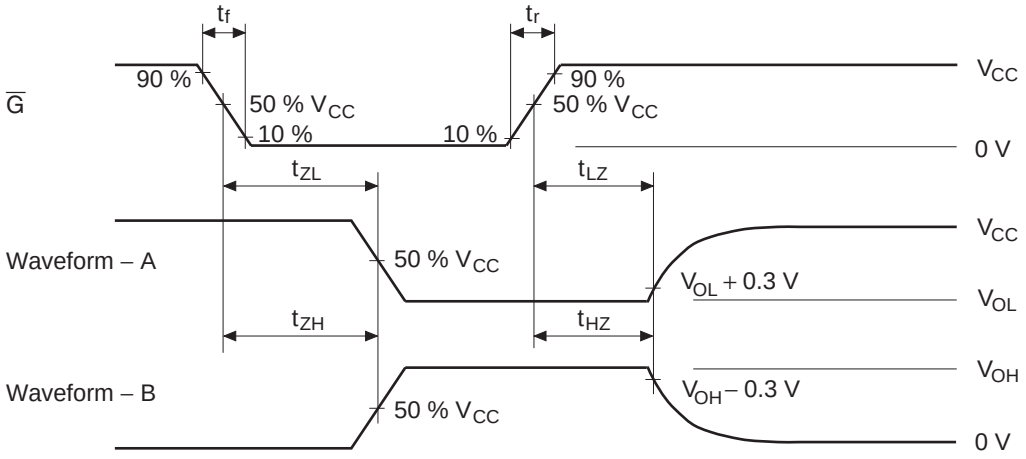
Waveform – 2



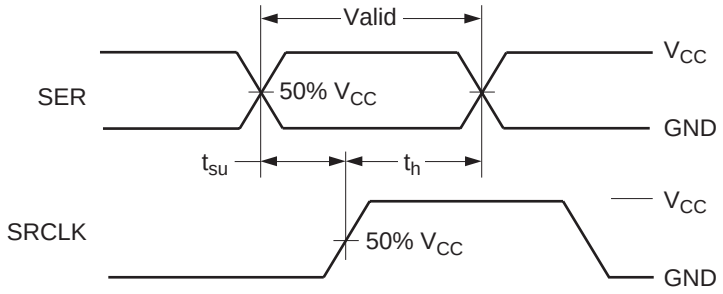
Waveform – 3



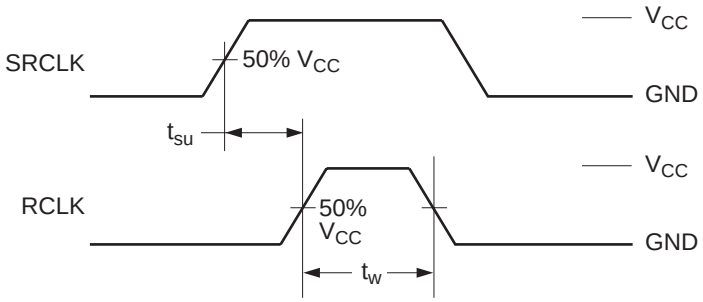
Waveform – 4



Waveform – 5



Waveform – 6

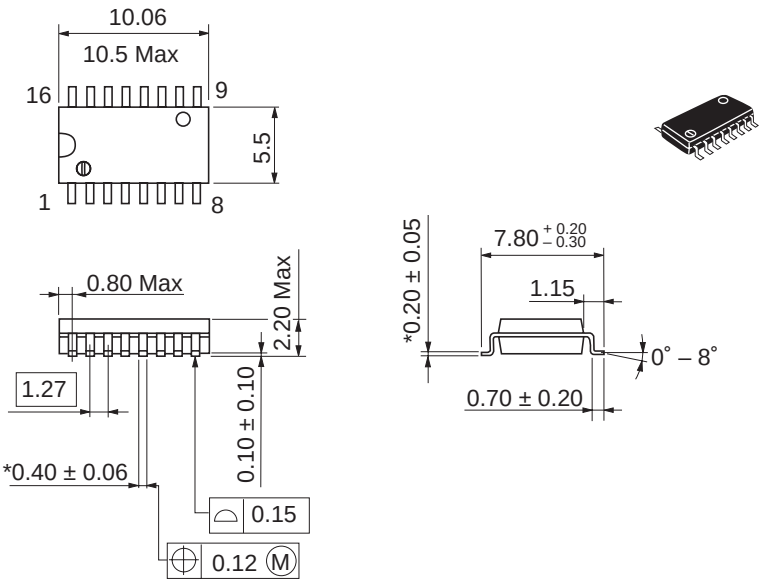


Notes: 1. Input waveform: PRR ≤ 1 MHz, Zo = 50 Ω, t ≤ 3 ns, t ≤ 3 ns
2. Waveform–A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform–B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of January, 2003

Unit: mm

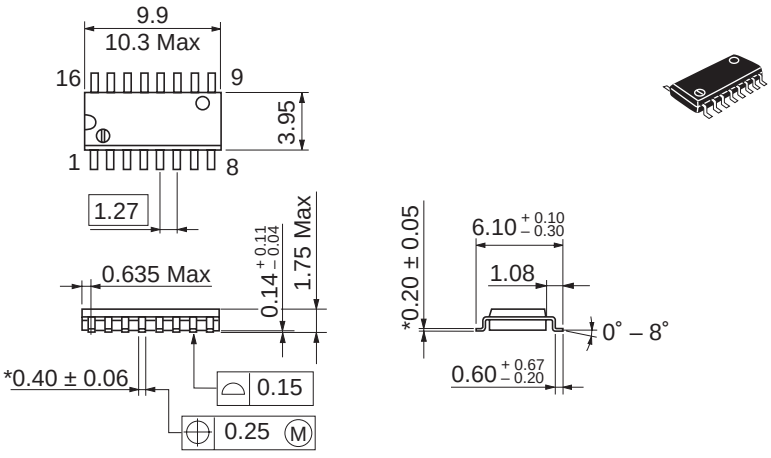


*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003

Unit: mm

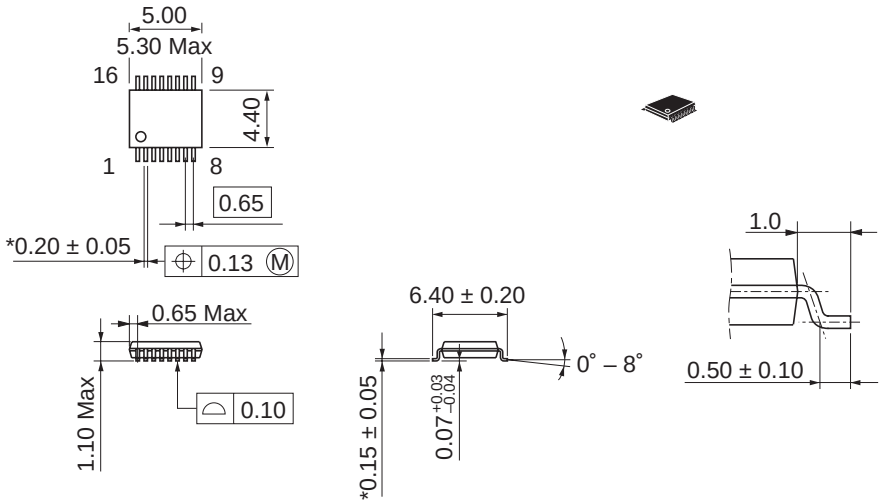


*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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