

# HD74LVC125A

## Quad. Bus Buffer Gates with 3-state Outputs

REJ03D0348-0400Z  
 (Previous ADE-205-108C (Z))  
 Rev.4.00  
 Jul. 23, 2004

### Description

The HD74LVC125A has four bus buffer gates in a 14 pin package. The device require the three state control input C to be taken high to put the output into the high impedance condition, whereas the device requires the control input to be low to put the output into high impedance. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH} (\text{Max.}) = 5.5\text{ V}$  ( $@V_{CC} = 0\text{ V to }5.5\text{ V}$ )
- All outputs  $V_{OUT} (\text{Max.}) = 5.5\text{ V}$  ( $@V_{CC} = 0\text{ V}$  or output off state)
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  ( $@V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V}$  ( $@V_{CC} = 3.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 24\text{ mA}$  ( $@V_{CC} = 3.0\text{ V to }5.5\text{ V}$ )
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC125AFPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74LVC125ATELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

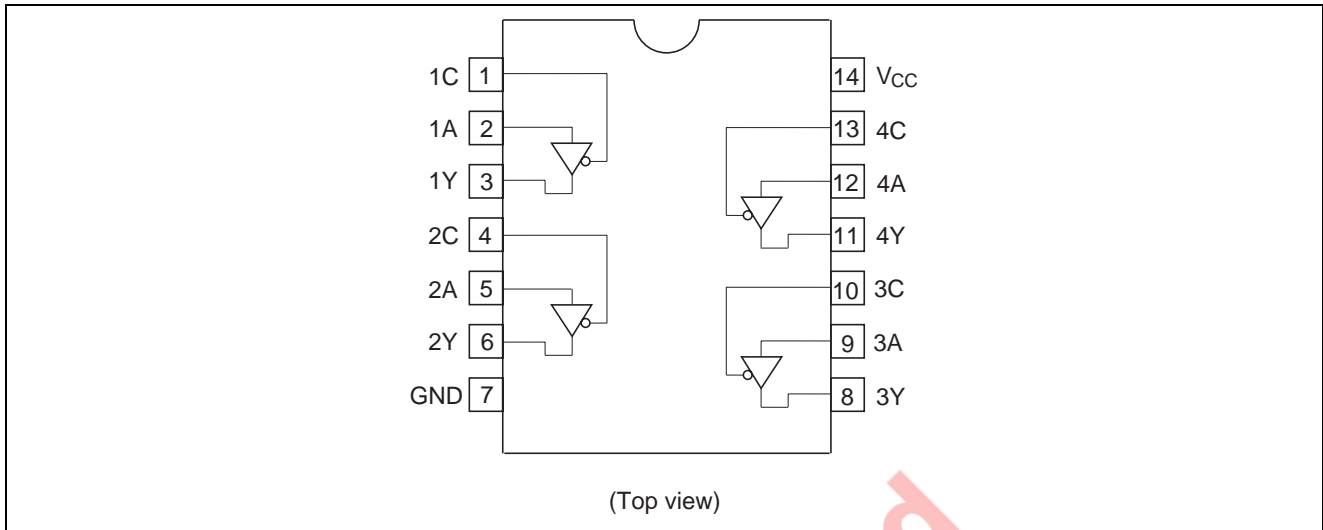
### Function Table

#### Inputs

C	A	Outputs Y
H	X	Z
L	L	L
L	H	H

- H: High level  
 L: Low level  
 X: Immaterial  
 Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 6.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5\text{ V}$
Input voltage	$V_I$	-0.5 to 6.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5\text{ V}$
		50		$V_O = V_{CC} + 0.5\text{ V}$
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 6.0		Output "Z" or $V_{CC}$ :OFF
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Storage temperature	Tstg	-65 to +150	$^{\circ}\text{C}$	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

**Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	1.5 to 5.5	V	Data hold
		2.0 to 5.5		At operation
Input / output voltage	V <sub>I</sub>	0 to 5.5	V	C, A
	V <sub>O</sub>	0 to V <sub>CC</sub>	V	Output "H" or "L"
		0 to 5.5		Output "Z" or V <sub>CC</sub> :OFF
Operating temperature	T <sub>a</sub>	-40 to 85	°C	
Output current	I <sub>OH</sub>	-12	mA	V <sub>CC</sub> = 2.7 V
		-24 <sup>*2</sup>		V <sub>CC</sub> = 3.0 V to 5.5 V
	I <sub>OL</sub>	12	mA	V <sub>CC</sub> = 2.7 V
		24 <sup>*2</sup>		V <sub>CC</sub> = 3.0 V to 5.5 V
Input rise / fall time <sup>*1</sup>	t <sub>r</sub> , t <sub>f</sub>	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

2. Duty cycle ≤ 50%

**Electrical Characteristics**

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—		
	V <sub>IL</sub>	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3		
Output voltage	V <sub>OH</sub>	2.7 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.7	2.2	—		I <sub>OH</sub> = -12 mA
		3.0	2.4	—		I <sub>OH</sub> = -24 mA
		3.0	2.2	—		
		4.5	3.8	—		
	V <sub>OL</sub>	2.7 to 5.5	—	0.2	V	I <sub>OL</sub> = 100 μA
		2.7	—	0.4		I <sub>OL</sub> = 12 mA
		3.0	—	0.55		I <sub>OL</sub> = 24 mA
		3.0	—	0.55		
		4.5	—	0.55		
Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA	V <sub>IN</sub> = 5.5 V <sub>CC</sub> GND
Off state output current	I <sub>IOZ</sub>	2.7 to 5.5	—	±5.0	μA	V <sub>IN</sub> = V <sub>CC</sub> , GND, V <sub>OUT</sub> = 5.5 V or GND
Output leak current	I <sub>OFF</sub>	0	—	20	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±10	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 3.6 to 5.5 V
		2.7 to 5.5	—	10		V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND

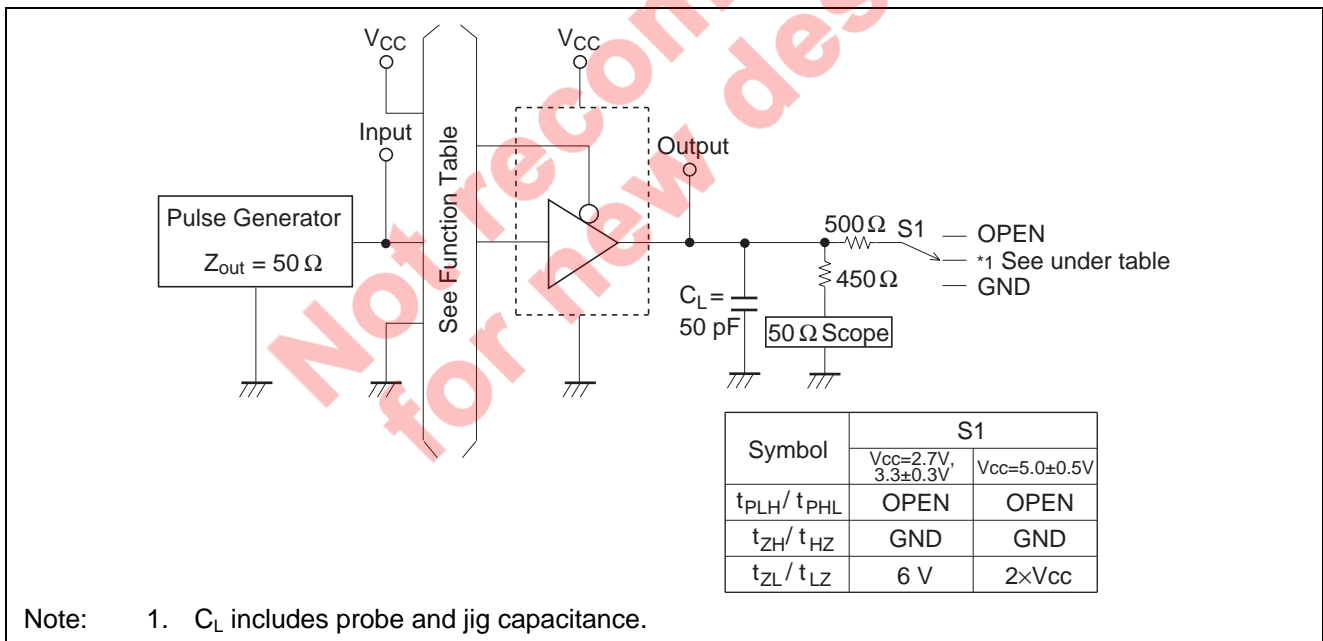
Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t <sub>PLH</sub>	2.7	—	—	6.5	ns	A	Y
	t <sub>PHL</sub>	3.3±0.3	1.5	—	6.0			
		5.0±0.5	—	—	5.0			
Output enable time	t <sub>ZH</sub>	2.7	—	—	8.0	ns	C	Y
	t <sub>ZL</sub>	3.3±0.3	1.5	—	7.0			
		5.0±0.5	—	—	6.0			
Output disable time	t <sub>HZ</sub>	2.7	—	—	6.5	ns	C	Y
	t <sub>LZ</sub>	3.3±0.3	1.5	—	5.5			
		5.0±0.5	—	—	4.5			
Between output pins skew <sup>*1</sup>	t <sub>OSLH</sub>	2.7	—	—	—	ns		
	t <sub>OSHL</sub>	3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C <sub>IN</sub>	2.7	—	3.0	—	pF		
Output capacitance	C <sub>O</sub>	2.7	—	15.0	—	pF		

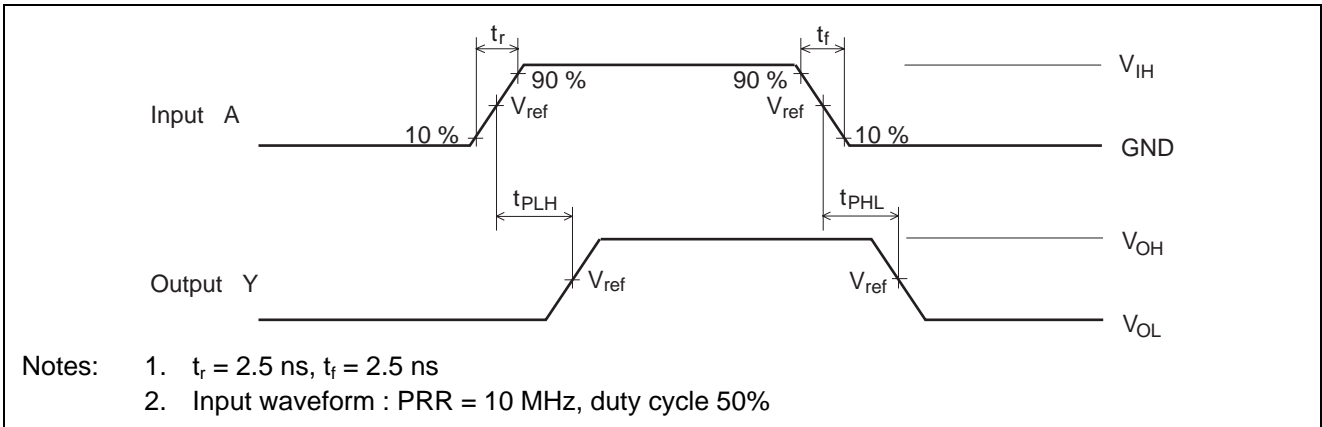
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

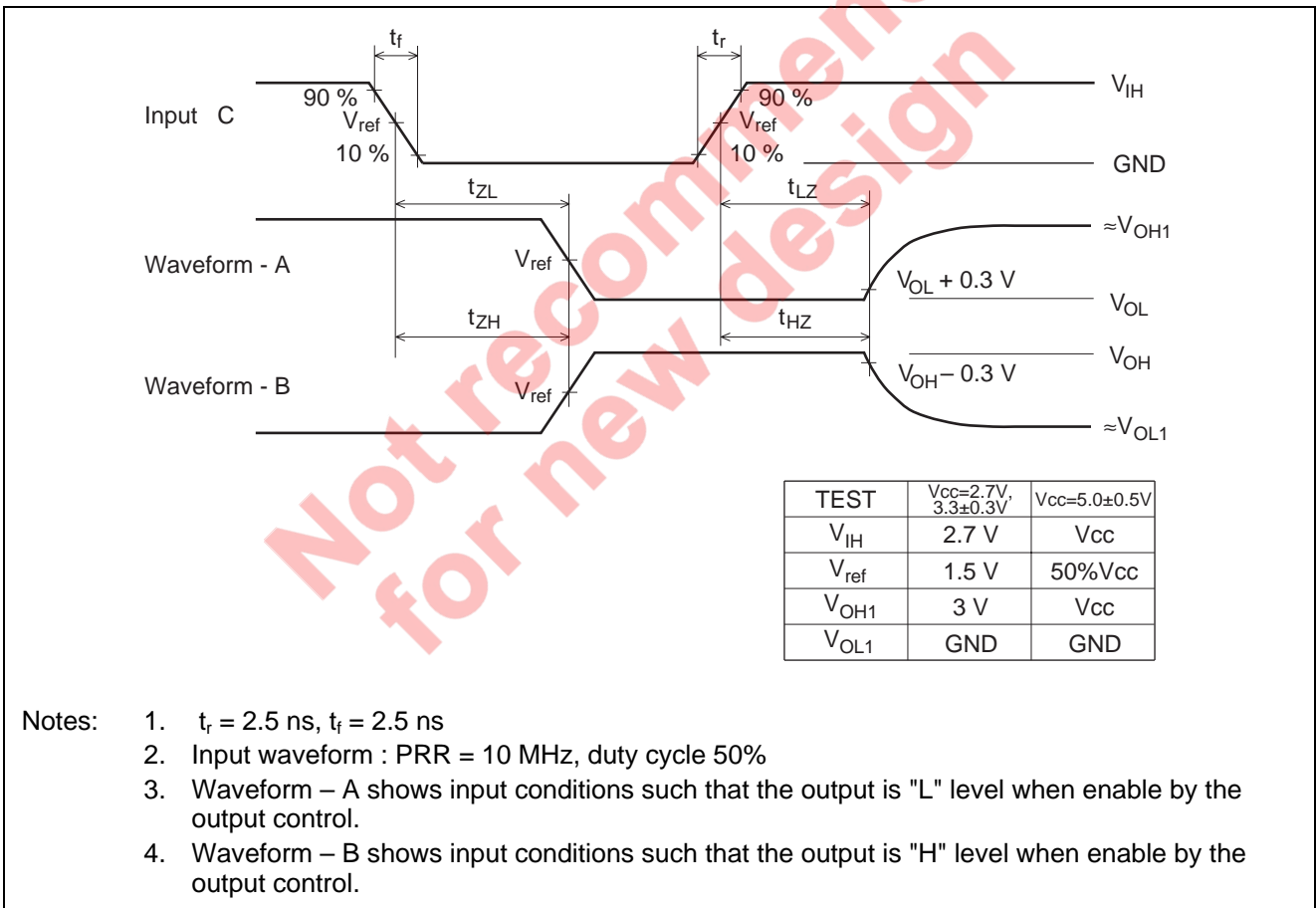
Test Circuit



Waveforms – 1

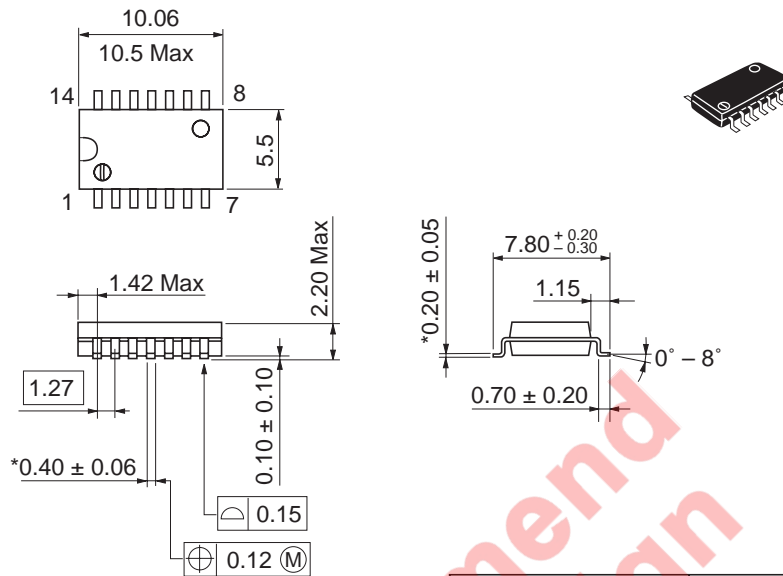


Waveforms – 2



Package Dimensions

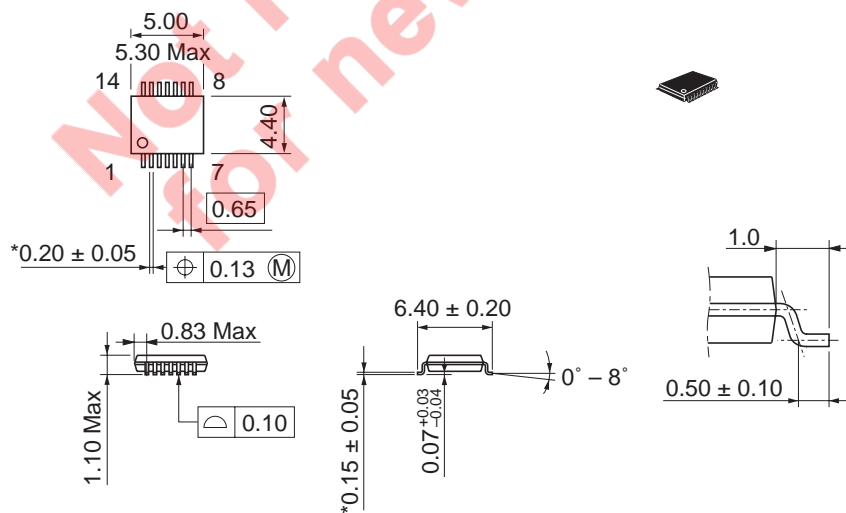
As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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