

HD74LVC16373A

16-bit D-type Transparent Latches with 3-state Outputs

HITACHI

ADE-205-121B(Z)
3rd Edition
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Description

The HD74LVC16373A has sixteen D type latches with three state outputs in a 48 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input ($\overline{1G}$, $\overline{2G}$), all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V to }5.5\text{ V}$)
- All outputs $V_{OUT}(\text{Max.}) = 5.5\text{ V}$ (@ $V_{CC} = 0\text{ V}$ or output off state)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0\text{ V}$ (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 24\text{ mA}$ (@ $V_{CC} = 3.0\text{ V to }5.5\text{ V}$)

Function Table

| Inputs | | | |
|----------------|----|---|----------|
| \overline{G} | LE | D | Output Q |
| H | X | X | Z |
| L | H | L | L |
| L | H | H | H |
| L | L | X | Q_0 |

H: High level

L: Low level

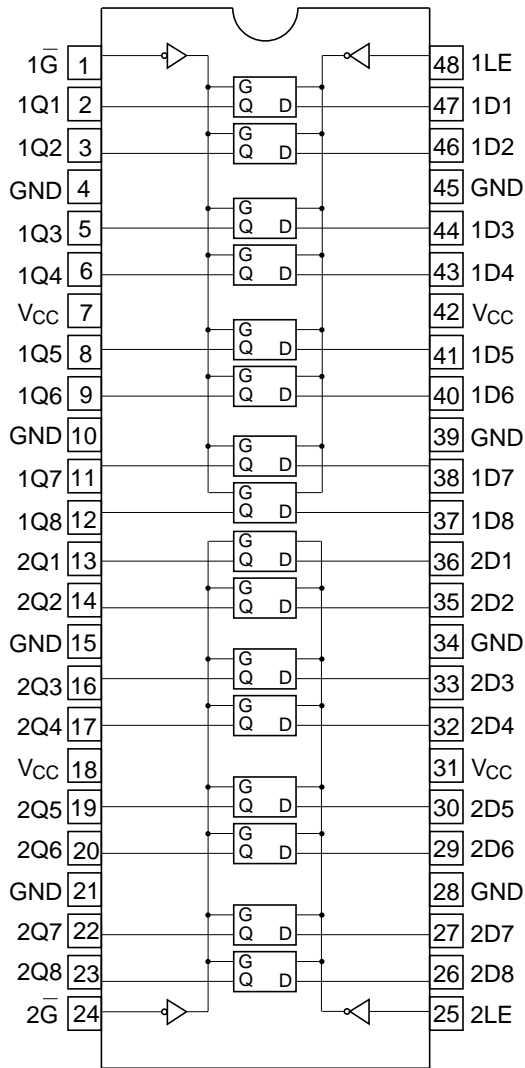
X: Immaterial

Z: High impedance

Q_0 : Level of Q before the indicated steady input conditions were established.

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Pin Arrangement



(Top view)

Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|------------------------------|-----------------------|------------------------|-------------|----------------------------|
| Supply voltage | V_{CC} | -0.5 to 6.0 | V | |
| Input diode current | I_{IK} | -50 | mA | $V_I = -0.5$ V |
| Input voltage | V_I | -0.5 to 6.0 | V | |
| Output diode current | I_{OK} | -50 | mA | $V_O = -0.5$ V |
| | | 50 | mA | $V_O = V_{CC} + 0.5$ V |
| Output voltage | V_O | -0.5 to $V_{CC} + 0.5$ | V | Output "H" or "L" |
| | | -0.5 to 6.0 | V | Output "Z" or $V_{CC}:OFF$ |
| Output current | I_O | ± 50 | mA | |
| V_{CC} , GND current / pin | I_{CC} or I_{GND} | 100 | mA | |
| Storage temperature | T_{stg} | -65 to +150 | $^{\circ}C$ | |

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

| Item | Symbol | Ratings | Unit | Conditions |
|-------------------------------------|------------|------------------|-------------|----------------------------|
| Supply voltage | V_{CC} | 1.5 to 5.5 | V | Data hold |
| | | 2.0 to 5.5 | V | At operation |
| Input / output voltage | V_I | 0 to 5.5 | V | \bar{G} , LE, D |
| | V_O | 0 to V_{CC} | V | Output "H" or "L" |
| | | 0 to 5.5 | V | Output "Z" or $V_{CC}:OFF$ |
| Operating temperature | T_a | -40 to 85 | $^{\circ}C$ | |
| Output current | I_{OH} | -12 | mA | $V_{CC} = 2.7$ V |
| | | -24 ² | mA | $V_{CC} = 3.0$ V to 5.5 V |
| | I_{OL} | 12 | mA | $V_{CC} = 2.7$ V |
| | | 24 ² | mA | $V_{CC} = 3.0$ V to 5.5 V |
| Input rise / fall time ¹ | t_r, t_f | 10 | ns/V | |

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle $\leq 50\%$

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Electrical Characteristics

| Item | Symbol | V_{CC} (V) | $T_a = -40 \text{ to } 85^\circ\text{C}$ | | Unit | Test Conditions |
|--------------------------|-----------------|--------------|--|---------------------|---------------|--|
| | | | Min | Max | | |
| Input voltage | V_{IH} | 2.7 to 3.6 | 2.0 | — | V | |
| | | 4.5 to 5.5 | $V_{CC} \times 0.7$ | — | V | |
| | V_{IL} | 2.7 to 3.6 | — | 0.8 | V | |
| | | 4.5 to 5.5 | — | $V_{CC} \times 0.3$ | V | |
| Output voltage | V_{OH} | 2.7 to 5.5 | $V_{CC} - 0.2$ | — | V | $I_{OH} = -100 \mu\text{A}$ |
| | | 2.7 | 2.2 | — | V | $I_{OH} = -12 \text{ mA}$ |
| | | 3.0 | 2.4 | — | V | |
| | | 3.0 | 2.2 | — | V | $I_{OH} = -24 \text{ mA}$ |
| | | 4.5 | 3.8 | — | V | |
| | V_{OL} | 2.7 to 5.5 | — | 0.2 | V | $I_{OL} = 100 \mu\text{A}$ |
| | | 2.7 | — | 0.4 | V | $I_{OL} = 12 \text{ mA}$ |
| | | 3.0 | — | 0.55 | V | $I_{OL} = 24 \text{ mA}$ |
| | | 4.5 | — | 0.55 | V | |
| | | | | | | |
| Input current | I_{IN} | 0 to 5.5 | — | ± 5.0 | μA | $V_{IN} = 5.5 \text{ V or GND}$ |
| Off state output current | I_{OZ} | 2.7 to 5.5 | — | ± 5.0 | μA | $V_{IN} = V_{CC}, \text{ GND}$ $V_{OUT} = 5.5 \text{ V or GND}$ |
| Output leak current | I_{OFF} | 0 | — | 20 | μA | $V_{IN} / V_{OUT} = 5.5 \text{ V}$ |
| Quiescent supply current | I_{CC} | 2.7 to 3.6 | — | ± 20 | μA | $V_{IN} / V_{OUT} = 3.6 \text{ to } 5.5 \text{ V}$ |
| | | 2.7 to 5.5 | — | 20 | μA | $V_{IN} = V_{CC} \text{ or GND}$ |
| | ΔI_{CC} | 3.0 to 3.6 | — | 500 | μA | $V_{IN} = \text{one input at } (V_{CC} - 0.6) \text{ V,}$ other inputs at $V_{CC} \text{ or GND}$ |

Switching Characteristics

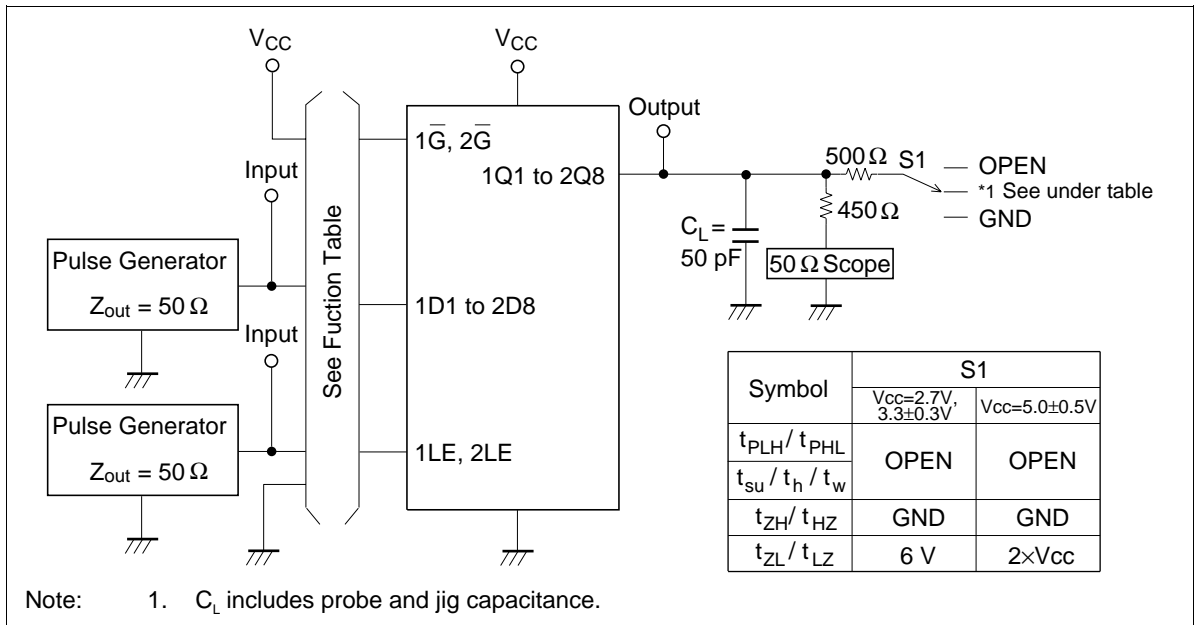
| Item | Symbol | V _{CC} (V) | Ta = -40 to 85°C | | | Unit | From (Input) | To (Output) |
|--|-------------------|---------------------|------------------|------|-----|------|--------------|-------------|
| | | | Min | Typ | Max | | | |
| Propagation delay time | t _{PLH} | 2.7 | — | — | 7.7 | ns | D | Q |
| | | 3.3±0.3 | 1.5 | — | 7.0 | ns | | |
| | | 5.0±0.5 | — | — | 5.5 | ns | | |
| | t _{PHL} | 2.7 | — | — | 8.0 | ns | LE | Q |
| | | 3.3±0.3 | 2.0 | — | 7.0 | ns | | |
| | | 5.0±0.5 | — | — | 5.5 | ns | | |
| Output enable time | t _{ZH} | 2.7 | — | — | 8.0 | ns | \bar{G} | \bar{Q} |
| | | 3.3±0.3 | 1.5 | — | 7.0 | ns | | |
| | | 5.0±0.5 | — | — | 6.0 | ns | | |
| Output disable time | t _{ZL} | 2.7 | — | — | 8.0 | ns | \bar{G} | \bar{Q} |
| | | 3.3±0.3 | 1.5 | — | 7.0 | ns | | |
| | | 5.0±0.5 | — | — | 6.0 | ns | | |
| Setup time | t _{su} | 2.7 | 2.0 | — | — | ns | | |
| | | 3.3±0.3 | 2.0 | — | — | ns | | |
| | | 5.0±0.5 | 2.0 | — | — | ns | | |
| Hold time | t _h | 2.7 | 1.5 | — | — | ns | | |
| | | 3.3±0.3 | 1.5 | — | — | ns | | |
| | | 5.0±0.5 | 1.5 | — | — | ns | | |
| Pulse width | t _w | 2.7 | 3.0 | — | — | ns | | |
| | | 3.3±0.3 | 3.0 | — | — | ns | | |
| | | 5.0±0.5 | 3.0 | — | — | ns | | |
| Between output pins skew ^{*1} | t _{OSLH} | 2.7 | — | — | — | ns | | |
| | | 3.3±0.3 | — | — | 1.0 | ns | | |
| | | 5.0±0.5 | — | — | 1.0 | ns | | |
| Input capacitance | C _{IN} | 2.7 | — | 3.0 | — | pF | | |
| Output capacitance | C _O | 2.7 | — | 15.0 | — | pF | | |

Note: 1. This parameter is characterized but not tested.

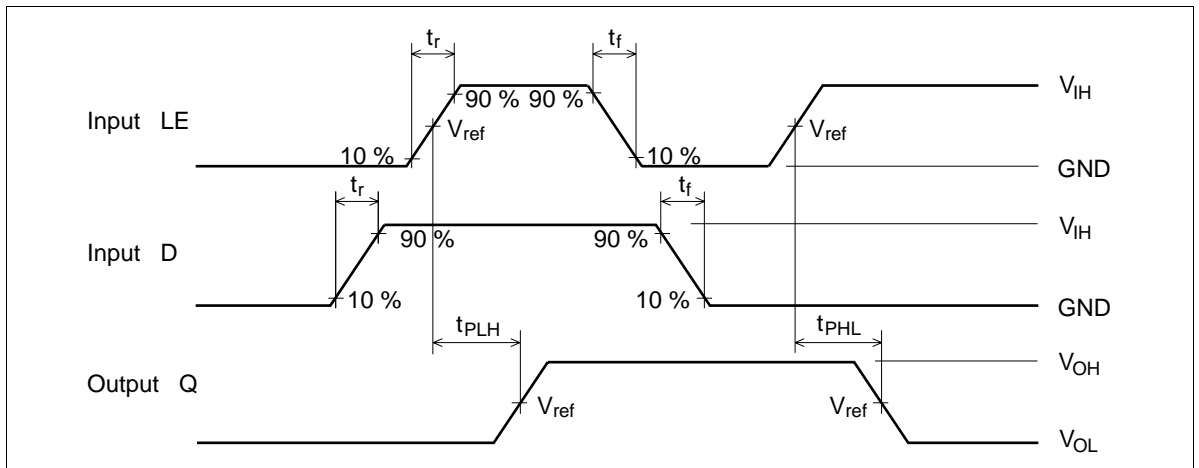
$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

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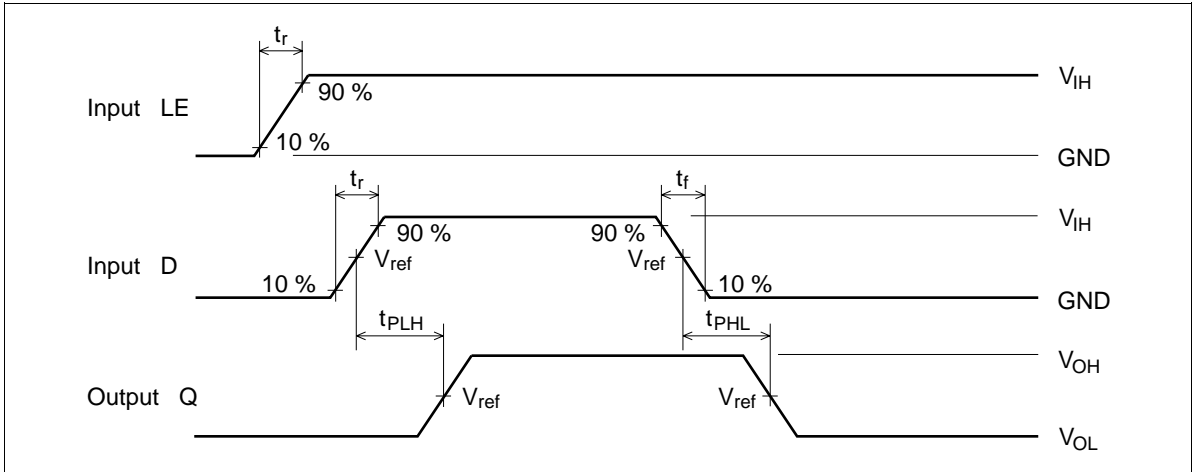
Test Circuit



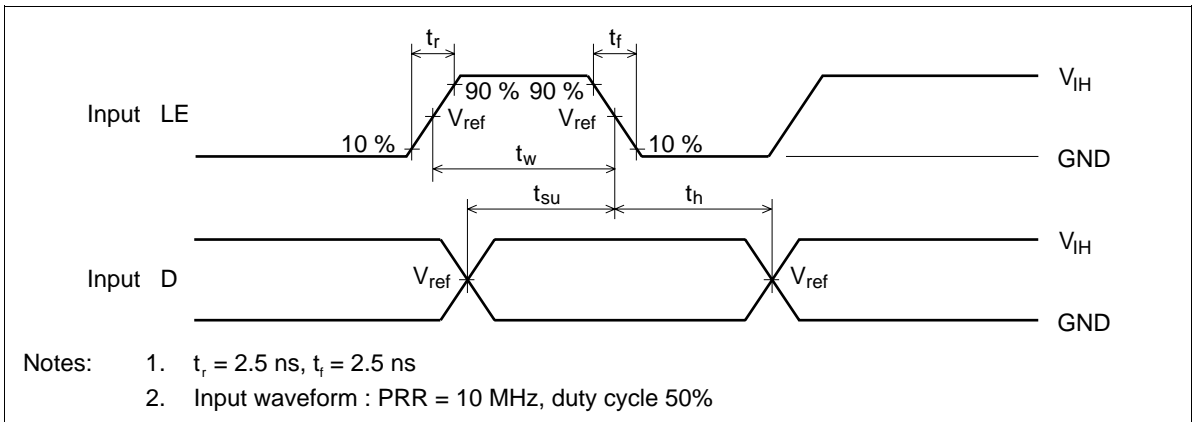
Waveforms - 1



Waveforms – 2



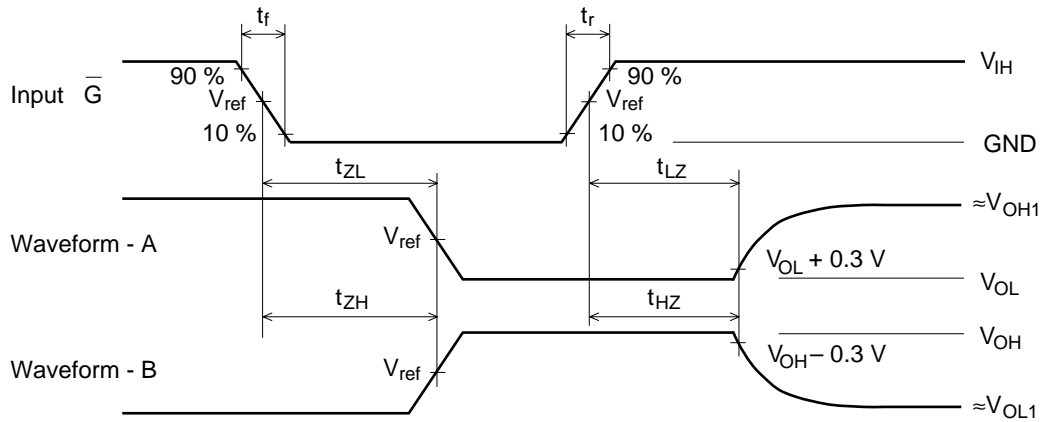
Waveforms – 3



- Notes:
1. $t_r = 2.5 \text{ ns}$, $t_f = 2.5 \text{ ns}$
 2. Input waveform : PRR = 10 MHz, duty cycle 50%

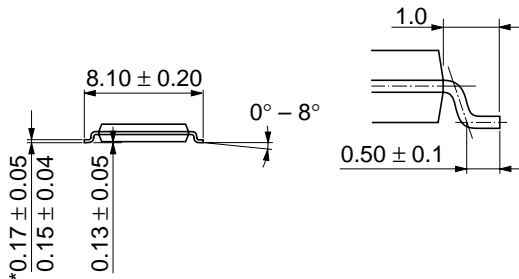
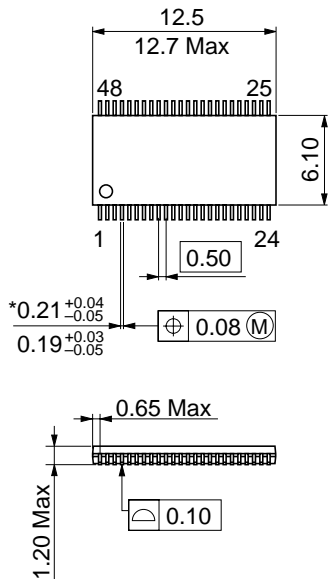
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Waveforms – 4



| TEST | $V_{CC}=2.7V, 3.3\pm 0.3V$ | $V_{CC}=5.0\pm 0.5V$ |
|-----------|----------------------------|----------------------|
| V_{IH} | 2.7 V | V_{CC} |
| V_{ref} | 1.5 V | $50\%V_{CC}$ |
| V_{OH1} | 3 V | V_{CC} |
| V_{OL1} | GND | GND |

- Notes:
- $t_r = 2.5 \text{ ns}$, $t_f = 2.5 \text{ ns}$
 - Input waveform : PRR = 10 MHz, duty cycle 50%
 - Waveform – A shows input conditions such that the output is "L" level when enable by the output control.
 - Waveform – B shows input conditions such that the output is "H" level when enable by the output control.



*Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | TTP-48DB |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.20 g |

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