HD74LVC74

Dual D-type Flip Flops with Preset and Clear

REJ03D0347–0400Z
(Previous ADE-205-066C (Z))
Rev.4.00
Jul. 22, 2004

Description

The HD74LVC74 has independent data, preset, clear, and clock inputs Q and $\overline{Q}$ outputs in a 14 pin package. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- V_{CC} = 2.0 V to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current ±24 mA (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC74FPEL	SOP–14 pin (JEITA)	FP–14DAV	FP	EL (2,000 pcs/reel)
HD74LVC74TELL	TSSOP–14 pin	TTP–14DV	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

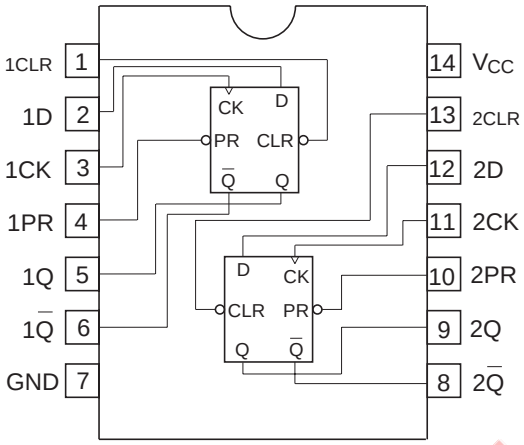
Function Table

Inputs				Outputs	
PR	**CLR**	**CK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [*1]	H [*1]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$
H	H	H	X	Q_0	$\overline{Q}_0$
H	H	↓	X	Q_0	$\overline{Q}_0$

H: High level
L: Low level
X: Immaterial
↓: High to Low transition
↑: Low to high transition
Q_0: Level to Q before the indicated steady input conditions was established.

Note: 1. Q and $\overline{Q}$ will remain high as long as preset and clear are low, but Q and $\overline{Q}$ are unpredictable, if preset and clear go high simultaneously.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 6.0	V	
Input diode current	I_{IK}	–50	mA	V_I = –0.5 V
Input voltage	V_I	–0.5 to 6.0	V	
Output diode current	I_{OK}	–50	mA	V_O = –0.5 V
		50		V_O = V_{CC} +0.5 V
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Output current	I_O	±50	mA	
V_{CC}, GND current / pin	I_{CC} or I_{GND}	100	mA	
Storage temperature	Tstg	–65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	1.5 to 5.5	V	Data retention
		2.0 to 5.5		At operation
Input / output voltage	V_I	0 to 5.5	V	PR, CLR, CK, D
	V_O	0 to V_{CC}		Q, $\overline{Q}$
Operating temperature	Ta	–40 to 85	°C	
Output current	I_{OH}	–12	mA	V_{CC} = 2.7 V
		–24 *2		V_{CC} = 3.0 V to 5.5 V
	I_{OL}	12	mA	V_{CC} = 2.7 V
		24 *2		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time *1	t_r, t_f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.
2. Duty cycle ≤ 50%

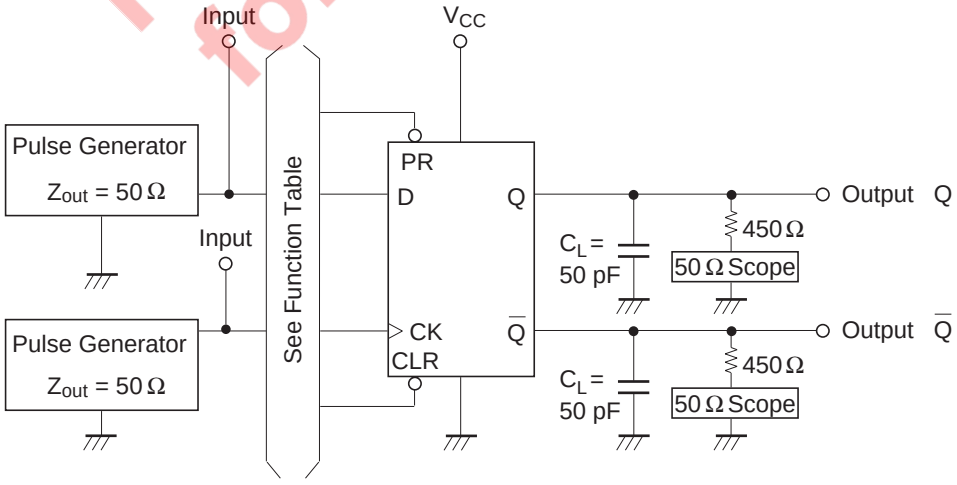
Electrical Characteristics

Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V_{CC}×0.7	—		
	V_{IL}	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V_{CC}×0.3		
Output voltage	V_{OH}	2.7 to 5.5	V_{CC} –0.2	—	V	I_{OH} = –100 µA
		2.7	2.2	—		I_{OH} = –12 mA
		3.0	2.4	—		
		3.0	2.0	—		I_{OH} = –24 mA
		4.5	3.8	—		
	V_{OL}	2.7 to 5.5	—	0.2	V	I_{OL} = 100 µA
		2.7	—	0.4		I_{OL} = 12 mA
		3.0	—	0.55		I_{OL} = 24 mA
		4.5	—	0.55		
Input current	I_{IN}	0 to 5.5	—	±5.0	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	20	µA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	500	µA	V_{IN} = one input at (V_{CC} –0.6)V, other inputs at V_{CC} or GND

Switching Characteristics

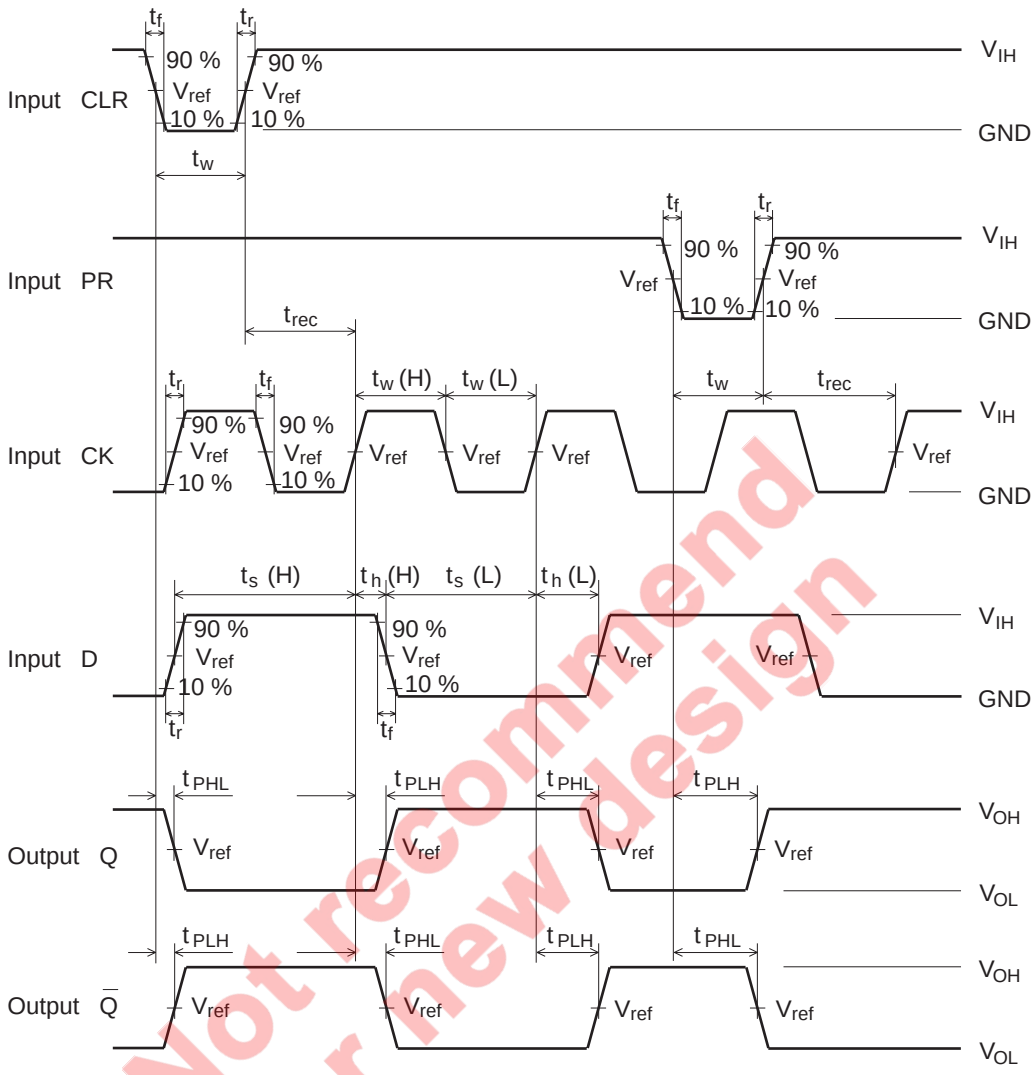
Item	Symbol	V_{CC} (V)	Ta = –40 to 85°C Min	Typ	Max	Unit	From (Input)	To (Output)
Maximum clock frequency	f_{max}	2.7	150.0	—	—	MHz		
		3.3±0.3	150.0	—	—			
		5.0±0.5	150.0	—	—			
Propagation delay time	t_{PLH}	2.7	—	6.0	9.0	ns	CLK	Q, $\overline{Q}$
	t_{PHL}	3.3±0.3	1.5	5.0	8.0			
		5.0±0.5	—	4.0	6.5			
	t_{PLH}	2.7	—	6.5	9.0	ns	PR or CLR	Q, $\overline{Q}$
	t_{PHL}	3.3±0.3	1.5	5.0	8.0			
		5.0±0.5	—	4.0	6.5			
Setup time	t_{su}	2.7	4.0	—	—	ns		
		3.3±0.3	3.0	—	—			
		5.0±0.5	3.0	—	—			
Hold time	t_h	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Pulse width	t_w	2.7	4.0	—	—	ns	CK	
		3.3±0.3	4.0	—	—			
		5.0±0.5	4.0	—	—			
		2.7	6.0	—	—		PR or CLR	
		3.3±0.3	5.0	—	—			
		5.0±0.5	4.0	—	—			
Recovery time	t_{rec}	2.7	3.0	—	—	ns		
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Input capacitance	C_{IN}	2.7	—	3.0	—	pF		
Output capacitance	C_O	2.7	—	15.0	—	pF		

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. Test is put into the each flip flops.

Waveforms

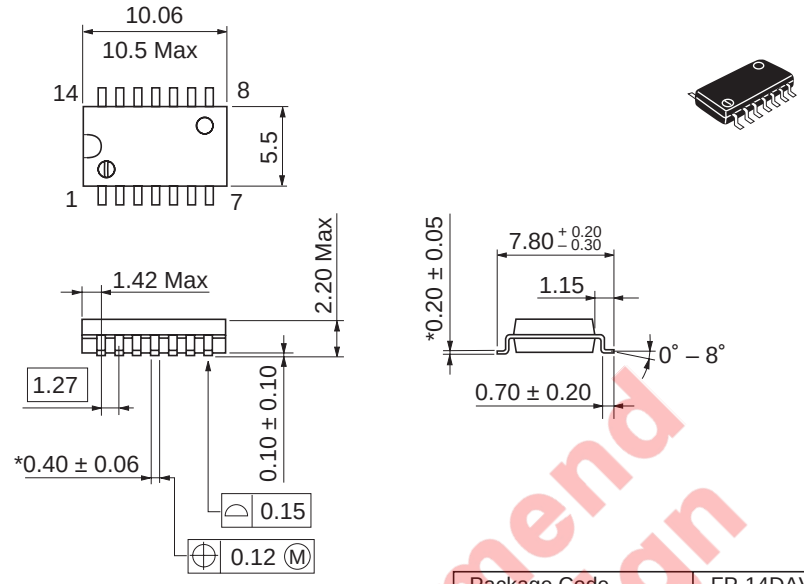


Symbol	V_{CC} = 2.7 V, 3.3±0.3 V	V_{CC} = 5.0±0.5 V
V_{IH}	2.7 V	V_{CC}
V_{ref}	1.5 V	50%V_{CC}

Notes:
1. tr = 2.5 ns, tf = 2.5 ns
2. Clock pulse input waveform : PRR = 10 MHz, duty cycle 50%
3. Data input waveform : PRR = 5 MHz, duty cycle 50%

Package Dimensions

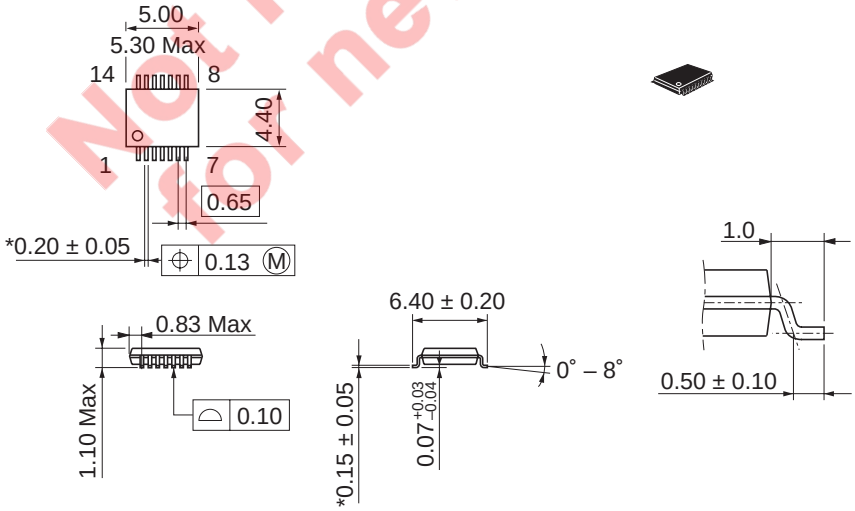
As of January, 2003
Unit: mm



Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

*Ni/Pd/Au plating

As of January, 2003
Unit: mm



Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

*Ni/Pd/Au plating

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