**DDR SDRAM Module 1024Mbyte (128Mx72bit), based on 64Mx8, 4Banks, 8K Ref., 184Pin-DIMM with PLL & Register Part No. HDD128M72D18RPW**

## GENERAL DESCRIPTION

The HDD128M72D18RPW is a 128M x 72 bit Double Data Rate(DDR) Synchronous Dynamic RAM high-density memory module. The module consists of eighteen CMOS 64M x 8 bit with 4banks DDR SDRAMs in 66pin TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 184-pin glass-epoxy. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD128M72D18RPW is a DIMM( Dual in line Memory Module) .Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications. All module components may be powered from a single 2.5V DC power supply and all inputs and outputs are SSTL_2 compatible.

## FEATURES

• Part Identification

HDD128M72D18RPW – 13A : 133MHz (CL=2)

HDD128M72D18RPW – 13B : 133MHz (CL=2.5)

HDD128M72D18RPW – 16B : 166MHz (CL=2.5)

• 1024MB(64Mx72) Registered DDR DIMM based on 64Mx8 DDR SDRAM

• 2.5V ± 0.2V VDD and VDDQ power supply

• Auto & self refresh capability (8K Cycles / 64ms)

• All input and output are compatible with SSTL_2 interface

• Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock

• All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock

• MRS cycle with address key programs

- Latency (Access from column address) : 2, 2.5
- Burst length : 2, 4, 8
- Data scramble : Sequential & Interleave

• Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock

• All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock

• The used device is 16M x 8bit x 4Banks DDR SDRAM

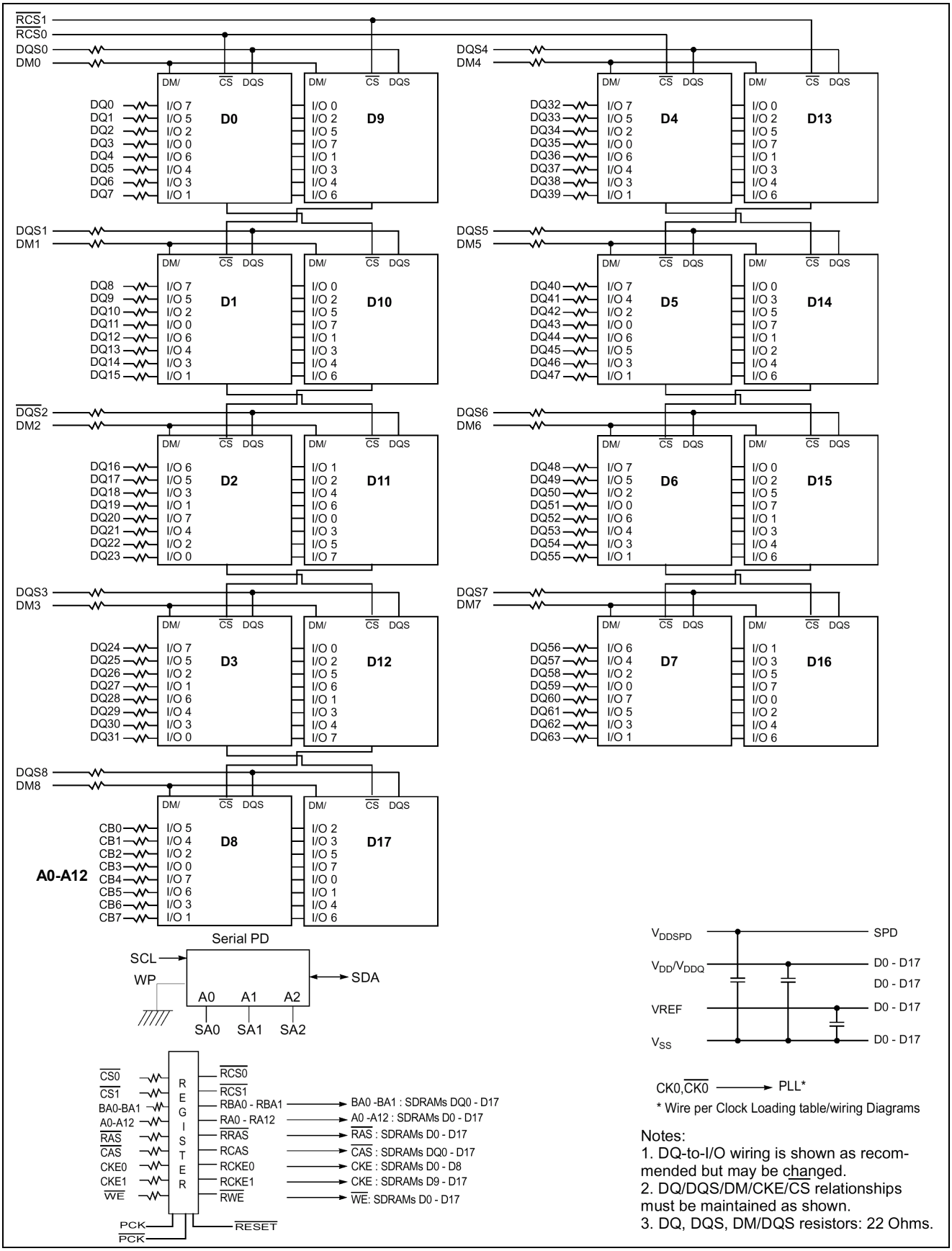
## PIN ASSIGNMENT

| PIN | Front | PIN | Back | PIN | Frontl | PIN | Back | PIN | Front | PIN | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF | 32 | A5 | 62 | $V_{DDQ}$ | 93 | $V_{SS}$ | 124 | $V_{SS}$ | 154 | /RAS |
| 2 | DQ0 | 33 | DQ24 | 63 | /WE | 94 | DQ4 | 125 | A6 | 155 | DQ45 |
| 3 | $V_{SS}$ | 34 | $V_{SS}$ | 64 | DQ41 | 95 | DQ5 | 126 | DQ28 | 156 | $V_{DDQ}$ |
| 4 | DQ1 | 35 | DQ25 | 65 | /CAS | 96 | $V_{DDQ}$ | 127 | DQ29 | 157 | /CS0 |
| 5 | DQS0 | 36 | DQS3 | 66 | $V_{SS}$ | 97 | DM0 | 128 | $V_{DDQ}$ | 158 | /CS1 |
| 6 | DQ2 | 37 | A4 | 67 | DQS5 | 98 | DQ6 | 129 | DM3 | 159 | DM5 |
| 7 | $V_{DD}$ | 38 | $V_{DD}$ | 68 | DQ42 | 99 | DQ7 | 130 | A3 | 160 | $V_{SS}$ |
| 8 | DQ3 | 39 | DQ26 | 69 | DQ43 | 100 | $V_{SS}$ | 131 | DQ30 | 161 | DQ46 |
| 9 | NC | 40 | DQ27 | 70 | $V_{DD}$ | 101 | NC | 132 | $V_{SS}$ | 162 | DQ47 |
| 10 | /RESET | 41 | A2 | 71 | * /CS2 | 102 | NC | 133 | DQ31 | 163 | * /CS3 |
| 11 | $V_{SS}$ | 42 | $V_{SS}$ | 72 | DQ48 | 103 | *A13 | 134 | CB4 | 164 | $V_{DDQ}$ |
| 12 | DQ8 | 43 | A1 | 73 | DQ49 | 104 | $V_{DDQ}$ | 135 | CB5 | 165 | DQ52 |
| 13 | DQ9 | 44 | CB0 | 74 | $V_{SS}$ | 105 | DQ12 | 136 | $V_{DDQ}$ | 166 | DQ53 |
| 14 | DQS1 | 45 | CB1 | 75 | * CK2 | 106 | DQ13 | 137 | CK0 | 167 | NC |
| 15 | $V_{DDQ}$ | 46 | $V_{DD}$ | 76 | * /CK2 | 107 | DM1 | 138 | /CK0 | 168 | $V_{DD}$ |
| 16 | * CK1 | 47 | DQS8 | 77 | $V_{DDQ}$ | 108 | $V_{DD}$ | 139 | $V_{SS}$ | 169 | DM6 |
| 17 | * /CK1 | 48 | A0 | 78 | DQS6 | 109 | DQ14 | 140 | DM8 | 170 | DQ54 |
| 18 | $V_{SS}$ | 49 | CB2 | 79 | DQ50 | 110 | DQ15 | 141 | A10 | 171 | DQ55 |
| 19 | DQ10 | 50 | $V_{SS}$ | 80 | DQ51 | 111 | CKE1 | 142 | CB6 | 172 | $V_{DDQ}$ |
| 20 | DQ11 | 51 | CB3 | 81 | $V_{SS}$ | 112 | $V_{DDQ}$ | 143 | $V_{DDQ}$ | 173 | NC |
| 21 | CKE0 | 52 | BA1 | 82 | VDDID | 113 | * BA2 | 144 | CB7 | 174 | DQ60 |
| 22 | $V_{DDQ}$ | KEY | | 83 | DQ56 | 114 | DQ20 | KEY | | 175 | DQ61 |
| 23 | DQ16 | 53 | DQ32 | 84 | DQ57 | 115 | A12 | 145 | $V_{SS}$ | 176 | $V_{SS}$ |
| 24 | DQ17 | 54 | $V_{DDQ}$ | 85 | $V_{DD}$ | 116 | $V_{SS}$ | 146 | DQ36 | 177 | DM7 |
| 25 | DQS2 | 55 | DQ33 | 86 | DQS7 | 117 | DQ21 | 147 | DQ37 | 178 | DQ62 |
| 26 | $V_{SS}$ | 56 | DQS4 | 87 | DQ58 | 118 | A11 | 148 | $V_{DD}$ | 179 | DQ63 |
| 27 | A9 | 57 | DQ34 | 88 | DQ59 | 119 | DM2 | 149 | DM4 | 180 | $V_{DDQ}$ |
| 28 | DQ18 | 58 | $V_{SS}$ | 89 | $V_{SS}$ | 120 | $V_{DD}$ | 150 | DQ38 | 181 | SA0 |
| 29 | A7 | 59 | BA0 | 90 | NC | 121 | DQ22 | 151 | DQ39 | 182 | SA1 |
| 30 | $V_{DDQ}$ | 60 | DQ35 | 91 | SDA | 122 | A8 | 152 | $V_{SS}$ | 183 | SA2 |
| 31 | DQ19 | 61 | DQ40 | 92 | SCL | 123 | DQ23 | 153 | DQ44 | 184 | VDDSPD |

* : These pins are not used in this module.

| PIN | PIN DESCRIPTION | PIN | PIN DESCRIPTION |
|---|---|---|---|
| A0~A12 | Address input | VDD | Power supply(2.5V) |
| BA0~BA1 | Bank Select Address | VDDQ | Power supply for DQs(2.5V) |
| DQ0~DQ63 | Data input/output | VREF | Power supply for reference |
| CB0~CB7 | Check Bit | VDDSPD | Serial EEPROM Power supply(3.3) |
| DQS0~DQS8 | Data Strobe input/output | VSS | Ground |
| DM0~DM8 | Data-in Mask | SA0~SA2 | Address in EEPROM |
| CK0~/CK0 | Clock input | SDA | Serial data I/O |
| CKE0~CKE1 | Clock enable input | SCL | Serial clock |
| /CS0~/CS1 | Chip Select input | VDDID | VDD identification flag |
| /RAS | Row Address strobe | NC | No connection |
| /CAS | Column Address strobe | | |

# Functional Block Diagram




Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

## PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|---|---|---|
| CK, /CK | Clock | CK and /CK are differential clock inputs. All address and control input signals are sampled on the positive edge of CK and negative edge of /CK. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/ /CK. |
| CKE | Clock Enable | CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognizean LVCMOS LOW level prior to VREF being stable on power-up. |
| /CS0, /CS1 | Chip Select | CS enables(registered LOW) and disables(registered HIGH) the command decoder.<br>All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code. |
| A0 ~ A12 | Address | Row/column addresses are multiplexed on the same pins.<br>Row address : RA0 ~ RA12, Column address : CA0 ~ CA9, CA11 |
| BA0 ~ BA1 | Bank select address | BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied. |
| /RAS | Row address strobe | Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge. |
| /CAS | Column address strobe | Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access. |
| /WE | Write enable | Enables write operation and row precharge.<br>Latches data in starting from /CAS, /WE active. |
| DQS0 ~ 7 | Data Strobe | Output with read data, input with write data. Edge-aligned with read data, cen-tered in write data. Used to capture write data. |
| DM0~7 | Input Data Mask | DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS load-ing. |
| DQ0 ~ 63 | Data input/output | Data inputs/outputs are multiplexed on the same pins. |
| VDDQ | Supply | DQ Power Supply : +2.5V ± 0.2V. |
| VDD | Supply | Power Supply : +2.5V ± 0.2V (device specific). |
| VSS | Supply | DQ Ground. |
| VREF | Supply | SSTL_2 reference voltage. |
| VSPD | Supply | Serial EEPROM Power Supply : 3.3v |
| VDDID | | VDD identification Flag |

## Absolute Maximum Ratings

| PARAMETER | SYMBOL | RATING | UNTE |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.5 ~ 3.6 | V |
| Voltage on $V_{DD}$ supply relative to Vss | $V_{DD}$ | -1.0 ~ 3.6 | V |
| Voltage on $V_{DDQ}$ supply relative to Vss | $V_{DDQ}$ | -0.5 ~ 3.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power dissipation | $P_D$ | 1.5 * # of component | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

**Notes:** Operation at above absolute maximum rating can adversely affect device reliability

## DC operating conditions

(Recommended operating conditions (Voltage referenced to Vss = 0V, $T_A$ = 0 to 70°C) )

| PARAMETER | SYMBOL | MIN | MAX | UNIT | NOTE |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.3 | 2.7 | V | |
| I/O Supply Voltage | $V_{DDQ}$ | 2.3 | 2.7 | V | |
| I/O Reference Voltage | $V_{REF}$ | 0.49*VDDQ | 0.51*VDDQ | V | 1 |
| I/O Termination Voltage(system) | $V_{TT}$ | $V_{REF}$ – 0.04 | $V_{REF}$ + 0.04 | V | 2 |
| Input High Voltage | $V_{IH}$ (DC) | $V_{REF}$ + 0.15 | $V_{REF}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ (DC) | -0.3 | $V_{REF}$ - 0.15 | V | |
| Input Voltage Level, CK and /CK inputs | $V_{IN}$ (DC) | -0.3 | $V_{DDQ}$ + 0.3 | V | |
| Input Differential Voltage, CK and /CK inputs | $V_{ID}$ (DC) | 0.3 | $V_{DDQ}$ + 0.6 | V | |
| Input leakage current | $I_{LI}$ | -2 | 2 | uA | 3 |
| Output leakage current | $I_{OZ}$ | -5 | 5 | uA | |
| Output High current (Normal strength driver) ; $V_{OUT}$=$V_{TT}$ + 0.84V | $I_{OH}$ | -16.8 | | mA | |
| Output Low current (Normal strength driver) ; $V_{OUT}$=$V_{TT}$ - 0.84V | $I_{OL}$ | 16.8 | | mA | |
| Output High current (Half strength driver) ; $V_{OUT}$=$V_{TT}$ + 0.45V | $I_{OH}$ | -9 | | mA | |

**Notes :**

1. Includes ±25mV margin for DC offset on $V_{REF}$, and a combined total of ±50mV margin for all AC noise and DC offset on $V_{REF}$, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on $V_{REF}$ and internal DRAM noise coupled to $V_{REF}$, both of which may result in $V_{REF}$ noise. $V_{REF}$ should be de-coupled with an inductance of $\leq$ 3nH.

2.$V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$, and must track variations in the DC level of $V_{REF}$

3. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on /CK.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a $V_{REF}$ envelop that has been bandwidth limited to 200MHZ.

## Input / Output Capacitance

($V_{DD}$ = min to max, $V_{DDQ}$ = 2.5V to 2.7V, $T_A$ = 25°C, f = 100MHz)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|
| Input capacitance(A0~A12, BA0~BA1, /RAS, /CAS,/WE) | $C_{IN1}$ | 9 | 11 | pF |
| Input capacitance(CKE0,CKE1) | $C_{IN2}$ | 9 | 11 | pF |
| Input capacitance(/CS0) | $C_{IN3}$ | 9 | 11 | pF |
| Input capacitance(CK0~CK2, /CK0~/CK2) | $C_{IN4}$ | 11 | 12 | pF |
| Input capacitance(DM0~DM7) | $C_{IN5}$ | 14 | 16 | pF |
| Data input/output capacitance (DQ0 ~ DQ63, DQS0~DQS7) | $C_{OUT1}$ | 14 | 16 | pF |
| Data input/output capacitance (CB0~CB7) | $C_{OUT2}$ | 14 | 16 | pF |

## DC Characteristics

($V_{DD}$ = 2.7V, T =10°C)

| Symbol | | -16B (DDR333@CL=2.5) | -13A (DDR266@CL=2.0) | -13B (DDR266@CL=2.5) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | 2230 | 2010 | 2010 | mA | |
| IDD1 | | 2500 | 2280 | 2280 | mA | |
| IDD2P | | 590 | 540 | 540 | mA | |
| IDD2F | | 1420 | 1290 | 1290 | mA | |
| IDD2Q | | 950 | 900 | 900 | mA | |
| IDD3P | | 1040 | 990 | 990 | mA | |
| IDD3N | | 1690 | 1560 | 1560 | mA | |
| IDD4R | | 2540 | 2280 | 2280 | mA | |
| IDD4W | | 2630 | 2330 | 2330 | mA | |
| IDD5 | | 3130 | 2910 | 2910 | mA | |
| IDD6 | Normal | 590 | 540 | 540 | mA | |
| | Low Power | 560 | 510 | 510 | mA | Optional |
| IDD7A | | 4520 | 4080 | 4080 | mA | |

**Notes:** Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**AC Operating Conditions**

| PARAMETER | STMBOL | MIN | MAX | UNIT | NOTE |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | $V_{IH}$ (AC) | VREF + 0.35 | | | |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals. | $V_{IL}$ (AC) | | VREF - 0.31 | V | |
| Input Differential Voltage, CK and CK inputs | $V_{ID}$ (AC) | 0.7 | VDDQ+0.6 | V | 1 |
| Input Crossing Point Voltage, CK and CK inputs | $V_{IX}$ (AC) | 0.5*VDDQ-0.2 | 0.5*VDDQ+0.2 | V | 2 |

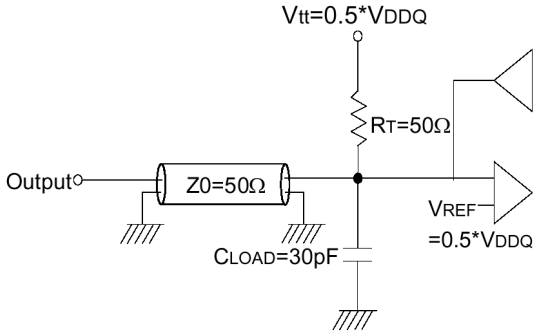
**Notes:**

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.

The value of $V_{IX}$ is expected to equal 0.5* $V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same

3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simula-tion.

the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.




Output Load Circuit (SSTL_2)

## AC characteristics

(THESE AC CHARACTERISTICS WERE TESTED ON THE COMPONENT)

| PARAMETER | | SYMBOL | DDR333@CL=2.5 -16B | | DDR266A@CL=2.0 -13A | | DDR266B@CL=2.5 -13B | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Row cycle time | | $t_{RC}$ | 60 | | 65 | | 65 | | ns | |
| Refresh row cycle time | | $t_{RFC}$ | 72 | | 75 | | 75 | | ns | |
| Row active time | | $t_{RAS}$ | 42 | 70K | 45 | 120K | 45 | 120K | ns | |
| /RAS to /CAS delay | | $t_{RCD}$ | 18 | | 20 | | 20 | | ns | |
| Row precharge time | | $t_{RP}$ | 18 | | 20 | | 20 | | ns | |
| Row active to Row active delay | | $t_{RRD}$ | 12 | | 15 | | 15 | | ns | |
| Write recovery time | | $t_{WR}$ | 15 | | 15 | | 15 | | $t_{CK}$ | |
| Last data in to Read command | | $t_{WTR}$ | 1 | | 1 | | 1 | | $t_{CK}$ | |
| Col. address to Col. address delay | | $t_{CCD}$ | 1 | | 1 | | 1 | | $t_{CK}$ | |
| Clock cycle time | CL=2.0 | $t_{CK}$ | 7.5 | 12 | 7.5 | 12 | 10 | 12 | ns | |
| | CL=2.5 | | 6 | 12 | 7.5 | 12 | 7.5 | 12 | ns | |
| Clock high level width | | $t_{CH}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | |
| Clock low level width | | $t_{CL}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | |
| DQS-out access time from CK/CK | | $t_{DQSCK}$ | -0.6 | +0.6 | -0.75 | +0.75 | -0.75 | +0.75 | ns | |
| Output data access time from CK/CK | | $t_{AC}$ | -0.7 | +0.7 | -0.75 | +0.75 | -0.75 | +0.75 | ns | |
| Data strobe edge to ouput data edge | | $t_{DQSQ}$ | - | 0.45 | - | +0.5 | - | +0.5 | ns | 12 |
| Read Preamble | | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | |
| Read Postamble | | $t_{RPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ | |
| CK to valid DQS-in | | $t_{DQSS}$ | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | $t_{CK}$ | |
| DQS-in setup time | | $t_{WPRES}$ | 0 | | 0 | | 0 | | ns | 3 |
| DQS-in hold time | | $t_{WPREH}$ | 0.25 | | 0.25 | | 0.25 | | $t_{CK}$ | |
| DQS-in falling edge to CK rising-setup time | | $t_{DSS}$ | 0.2 | | 0.2 | | 0.2 | | $t_{CK}$ | |
| DQS-in falling edge to CK rising hold time | | $t_{DSH}$ | 0.2 | | 0.2 | | 0.2 | | $t_{CK}$ | |
| DQS-in high level width | | $t_{DQSH}$ | 0.35 | | 0.35 | | 0.35 | | $t_{CK}$ | |
| DQS-in low level width | | $t_{DQSL}$ | 0.35 | | 0.35 | | 0.35 | | $t_{CK}$ | |
| DQS-in cycle time | | $t_{DSC}$ | 0.9 | | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | |
| Address and Control Input setup time(Fast) | | $t_{IS}$ | 0.75 | | 0.9 | | 0.9 | | ns | i,5.7~9 |
| Address and Control Input hold time(Fast) | | $t_{IH}$ | 0.75 | | 0.9 | | 0.9 | | ns | i,5.7~9 |
| Address and Control Input setup time(Slow) | | $t_{IS}$ | 0.8 | | 1.0 | | 1.0 | | ns | i, 6~9 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Address and Control Input hold time(Slow) | $t_{IH}$ | 0.8 | | 1.0 | | 1.0 | | ns | i, 6~9 |
| Data-out high impedence time from CK/CK | $t_{HZ}$ | -0.7 | +0.7 | -0.75 | +0.75 | -0.75 | +0.75 | ns | 1 |
| Data-out low impedence time from CK/CK | $t_{LZ}$ | -0.7 | +0.7 | -0.75 | +0.75 | -0.75 | +0.75 | ns | 1 |
| Input Slew Rate(for input only pins) | $t_{SL(IO)}$ | 0.5 | | 0.5 | | 0.5 | | ns | |
| Input Slew Rate(for I/O pins) | $t_{SL(O)}$ | 0.5 | | 0.5 | | 0.5 | | $t_{CK}$ | |
| Output Slew Rate(x4,x8) | $t_{SL(O)}$ | 1.0 | 4.5 | 1.0 | 4.5 | 1.0 | 4.5 | $t_{CK}$ | |
| Output Slew Rate(x16) | $t_{SL(O)}$ | 0.7 | 5 | 0.7 | 5 | 0.7 | 5 | | |
| Output Slew Rate Matching Ratio(rise to fall) | $t_{SLMR}$ | 0.67 | 1.5 | 0.67 | 1.5 | 0.67 | 1.5 | | |
| Mode register set cycle time | $t_{MRD}$ | 12 | | 15 | | 15 | | ns | |
| DQ & DM setup time to DQS | $t_{DS}$ | 0.45 | | 0.5 | | 0.5 | | ns | j, k |
| DQ & DM hold time to DQS | $t_{DH}$ | 0.45 | | 0.5 | | 0.5 | | ns | j, k |
| Control & Address input pulse width | $t_{IPW}$ | 2.2 | | 2.2 | | 2.2 | | ns | 8 |
| DQ & DM input pulse width | $t_{DIPW}$ | 1.75 | | 1.75 | | 1.75 | | ns | 8 |
| Power down exit time | $t_{PDEX}$ | 6 | | 7.5 | | 7.5 | | ns | |
| Exit self refresh to non-Read command | $t_{XSNR}$ | 75 | | 75 | | 75 | | ns | |
| Exit self refresh to read command | $t_{XSRD}$ | 200 | | 200 | | 200 | | $t_{CK}$ | |
| Refresh interval time | $t_{REFI}$ | 7.8 | | 7.8 | | 7.8 | | ns | 4 |
| Output DQS valid window | $t_{QH}$ | $t_{HP}$ -$t_{QHS}$ | - | $t_{HP}$ -$t_{QHS}$ | - | $t_{HP}$ -$t_{QHS}$ | - | ns | 11 |
| Clock half period | $t_{HP}$ | $t_{CLmin}$ or $t_{CHmin}$ | - | $t_{CLmin}$ or $t_{CHmin}$ | - | $t_{CLmin}$ or $t_{CHmin}$ | - | ns | 10,11 |
| Data hold skew factor | $t_{QHS}$ | | 0.55 | | 0.75 | | 0.75 | ns | 11 |
| DQS write postamble time | $t_{WPST}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{CK}$ | 2 |
| Active to Read with Auto precharge command | $t_{RAP}$ | | 18 | | 20 | | 20 | | |
| Autoprecharge write recovery + Precharge time | $t_{DAL}$ | ($t_{WR}$/$t_{CK}$)+ ($t_{RP}$/$t_{CK}$) | | ($t_{WR}$/$t_{CK}$)+ ($t_{RP}$/$t_{CK}$) | | ($t_{WR}$/$t_{CK}$)+ ($t_{RP}$/$t_{CK}$) | | $t_{CK}$ | 13 |

**Notes :**

Maximum burst refresh of 8.

$t_{HZQ}$ transitions occurs in the same assess time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving.

The specific requirement is that DQS be valid(High-Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on $t_{DQSS}$.

The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

## System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333, DDR266 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

**Table 1 : Input Slew Rate for DQ, DQS, and DM**

| AC CHARACTERISTICS | | DDR333 | | DDR266 | | | |
|---|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | MIN | MAX | Units | Notes |
| DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC) | DCSLEW | TBD | TBD | TBD | TBD | V/ns | a, m |

**Table 2 : Input Setup & Hold Time Derating for Slew Rate**

| INPUT SLEW RATE | TIS | TIH | UNITS | NOTES |
|---|---|---|---|---|
| 0.5 V/ns | 0 | 0 | ps | i |
| 0.4 V/ns | +50 | 0 | ps | i |
| 0.3 V/ns | +100 | 0 | ps | i |

**Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate**

| INPUT SLEW RATE | TDS | TDH | UNITS | NOTES |
|---|---|---|---|---|
| 0.5 V/ns | 0 | 0 | ps | k |
| 0.4 V/ns | +75 | +75 | ps | k |
| 0.3 V/ns | +150 | +150 | ps | k |

**Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate**

| DELTA SLEW RATE | TDS | TDH | UNITS | NOTES |
|---|---|---|---|---|
| +/- 0.0 V/ns | 0 | 0 | ps | j |
| +/- 0.25 V/ns | +50 | +50 | ps | j |
| +/- 0.5 V/ns | +100 | +100 | ps | j |

**Table 5 : Output Slew Rate Characteristice (X4, X8 Devices only)**

| SLEW RATE CHARACTERISTIC | TYPICAL RANGE (V/NS) | MINIMUM (V/NS) | MAXIMUM (V/NS) | NOTES |
|---|---|---|---|---|
| Pullup Slew Rate | 1.2 ~ 2.5 | 1.0 | 4.5 | a,c,d,f,g,h |
| Pulldown slew | 1.2 ~ 2.5 | 1.0 | 4.5 | b,c,d,f,g,h |

**Table 6 : Output Slew Rate Characteristice (X16 Devices only)**

| SLEW RATE CHARACTERISTIC | TYPICAL RANGE (V/NS) | MINIMUM (V/NS) | MAXIMUM (V/NS) | NOTES |
|---|---|---|---|---|
| Pullup Slew Rate | 1.2 ~ 2.5 | 0.7 | 5.0 | a,c,d,f,g,h |
| Pulldown slew | 1.2 ~ 2.5 | 0.7 | 5.0 | b,c,d,f,g,h |

**Table 7 : Output Slew Rate Matching Ratio Characteristics**

| AC CHARACTERISTICS | DDR333 | | DDR266 | | |
|---|---|---|---|---|---|
| PARAMETER | MIN | MAX | MIN | MAX | Notes |
| Output Slew Rate Matching Ratio (Pullup to Pulldown) | TBD | TBD | TBD | TBD | e,m |

## Component Notes

1. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).

2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

5. For command/address input slew rate $\geq$ 1.0 V/ns

6. For command/address input slew rate $\geq$ 0.5 V/ns and < 1.0 V/ns

7. For CK & CK slew rate $\geq$ 1.0 V/ns

8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

9. Slew Rate is measured between VOH(ac) and VOL(ac).

10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

11. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and pchannel to n-channel variation of the output drivers.

12. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

13. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3)
tDAL = 5 clocks

**System Notes :**

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 1.

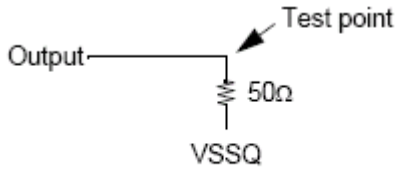



Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

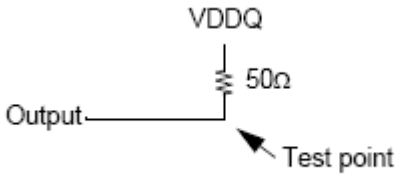



Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
Example : For typical slew rate, DQ0 is switching
For minmum slew rate, all DQ bits are switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical : 25 °C (T Ambient), VDDQ = 2.5V, typical process
Minimum : 70 °C (T Ambient), VDDQ = 2.3V, slow - slow process
Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package divices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates detemined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as: {1/(Slew Rate1)} - {1/(Slew Rate2)}
For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC - AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotony.

## SIMPLIFIED TRUTH TABLE

| COMMAND | | | CKE n-1 | CKE n | /CS | /RAS | /CAS | /WE | DM | BA 0,1 | A10/ AP | A11,A12 A9~A0 | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Extended MRS | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Register | Mode register set | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank active & row addr. | | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column Address | 4 |
| | Auto precharge eable | | | | | | | | | | H | | 4 |
| Write & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column Address | 4 |
| | Auto precharge enable | | | | | | | L | | | H | | 4,6 |
| Burst Stop | | | H | X | L | H | H | L | X | X | | | 7 |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | | X | H | | 5 |
| Clock suspend or active power down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge power down mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| DM | | | H | X | | | | | V | X | | | 8 |
| No operation command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :**

1. OP Code : Operand code

A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at $t_{RP}$ after the end of burst.

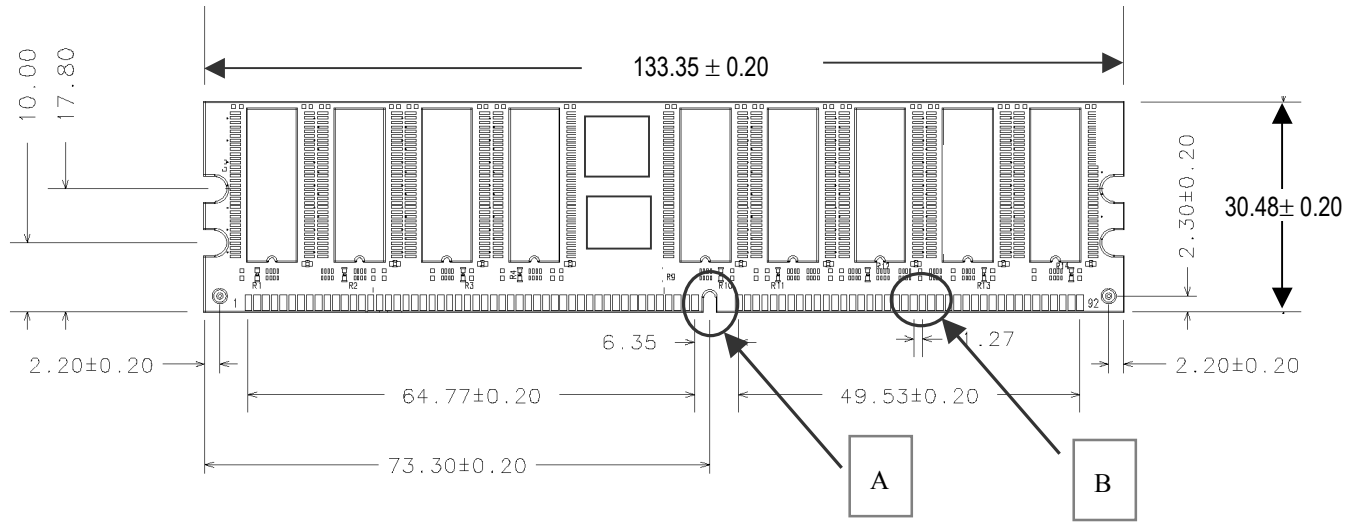
6. Burst stop command is valid at every burst length.

DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0)

## PACKAGING INFORMATION

**Unit : mm**

### <Front–Side >

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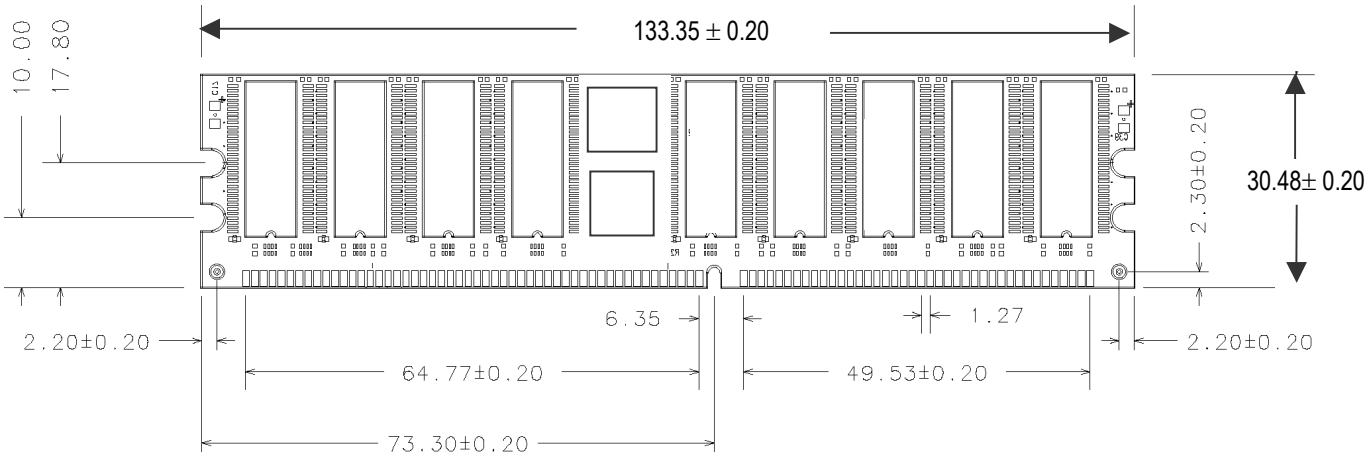
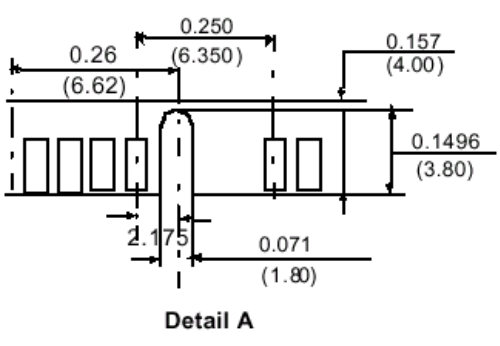
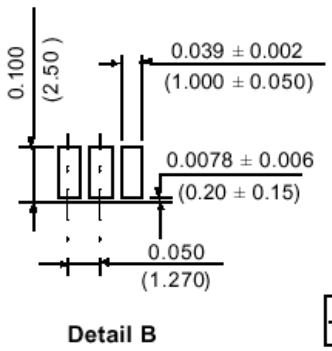
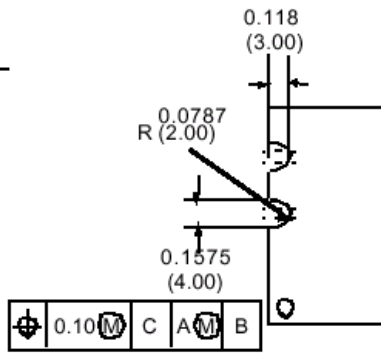



Detail A




Detail B




*** **PCB Thickness : 1.27 ± 0.08 mm**

## ORDERING INFORMATION

| Part Number | Density | Org. | Package | Ref. | Vcc | MODE | MAX.frq |
|---|---|---|---|---|---|---|---|
| HDD128M72D18RPW-16B | 1024MByte | 128M x 72 | 184PIN DIMM | 8K | 2.5V | DDR Registered | 166MHz/CL2 DDR333 |
| HDD128M72D18RPW-13A | 1024MByte | 128M x 72 | 184PIN DIMM | 8K | 2.5V | DDR Registered | 133MHz/CL2 DDR266 |
| HDD128M72D18RPW-13B | 1024MByte | 128M x 72 | 184PIN DIMM | 8K | 2.5V | DDR Registered | 133MHz/CL2.5 DDR266 |