

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF40174B** **MSI** Hex D-type flip-flop

Product specification  
File under Integrated Circuits, IC04

January 1995

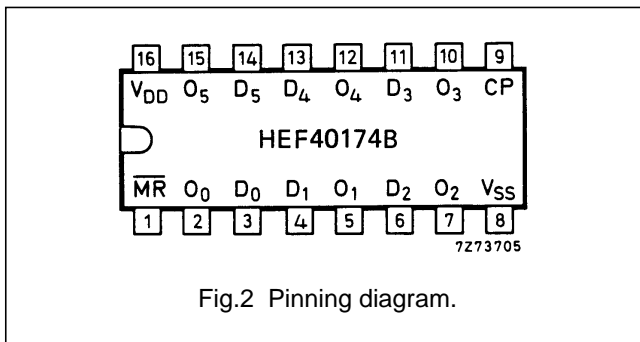
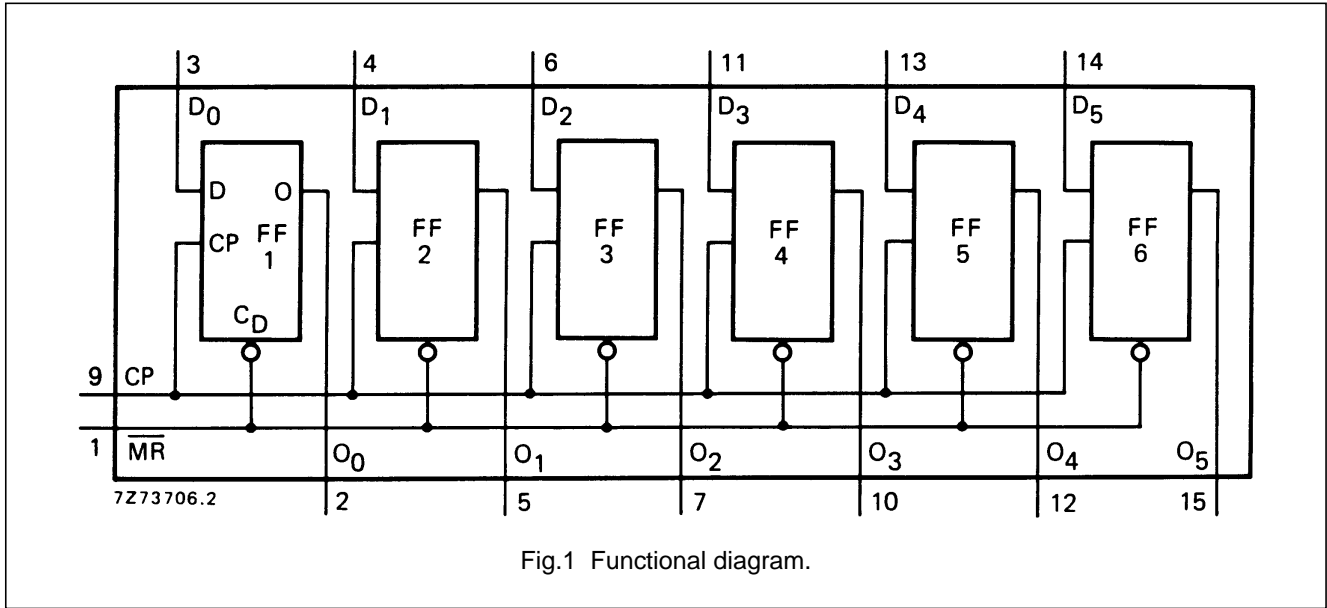
# Hex D-type flip-flop

# HEF40174B MSI

**DESCRIPTION**

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D<sub>0</sub> to D<sub>5</sub>), a clock input (CP), an overriding asynchronous master reset input (MR), and six

buffered outputs (O<sub>0</sub> to O<sub>5</sub>). Information on D<sub>0</sub> to D<sub>5</sub> is transferred to O<sub>0</sub> to O<sub>5</sub> on the LOW to HIGH transition of CP if MR is HIGH. When LOW, MR resets all flip-flops (O<sub>0</sub> to O<sub>5</sub> = LOW) independent of CP and D<sub>0</sub> to D<sub>5</sub>.



**PINNING**

- D<sub>0</sub> to D<sub>5</sub> data inputs
- CP clock input (LOW to HIGH; edge-triggered)
- MR master reset input (active LOW)
- O<sub>0</sub> to O<sub>5</sub> buffered outputs

**FUNCTION TABLE**

INPUTS			OUTPUT
CP	D	MR	O
	H	H	H
	L	H	L
	X	H	no change
X	X	L	L

**Notes**

1. H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial
- = positive-going transition
- = negative-going transition

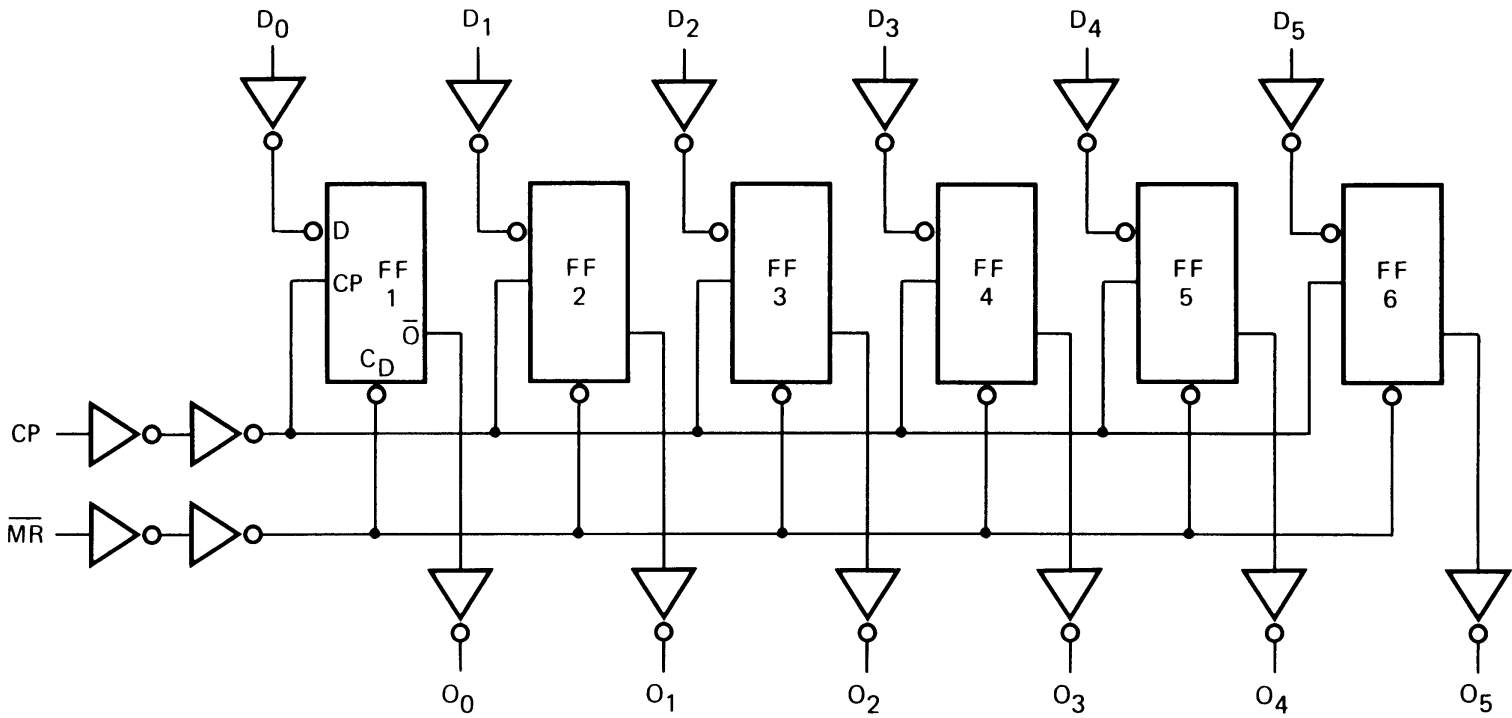
- HEF40174BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40174BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40174BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

**FAMILY DATA, I<sub>DD</sub> LIMITS category MSI**

See Family Specifications

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Fig.3 Logic diagram.

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## AC CHARACTERISTICS

 $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		75	155	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			30	65	ns	
	15			20	45	ns	
LOW to HIGH	5	$t_{PLH}$		75	155	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			30	65	ns	
	15			20	45	ns	
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		85	175	ns	$58 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10			35	70	ns	
	15			25	50	ns	
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10			30	60	ns	
	15			20	40	ns	
LOW to HIGH	5	$t_{TLH}$		60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10			30	60	ns	
	15			20	40	ns	
Set-up time $D_n \rightarrow CP$	5	$t_{su}$	20	10		ns	see also waveforms Fig.4
	10		10	5		ns	
	15		10	5		ns	
Hold time $D_n \rightarrow CP$	5	$t_{hold}$	10	0		ns	
	10		5	0		ns	
	15		5	0		ns	
Minimum clock pulse width; LOW	5	$t_{WCPL}$	70	35		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum $\overline{MR}$ pulse width; LOW	5	$t_{WMRL}$	70	35		ns	
	10		35	15		ns	
	15		25	10		ns	
Recovery time for $\overline{MR}$	5	$t_{RMR}$	45	25		ns	
	10		20	10		ns	
	15		15	5		ns	
Maximum clock pulse frequency	5	$f_{max}$	5	11		MHz	
	10		15	30		MHz	
	15		20	45		MHz	

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	$V_{DD}$ V	TYPICAL FORMULA FOR P( $\mu$ W)	
Dynamic power dissipation per package (P)	5 10 15	$3500 f_i + \sum (f_o C_L) \times V_{DD}^2$ $16\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $42\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)

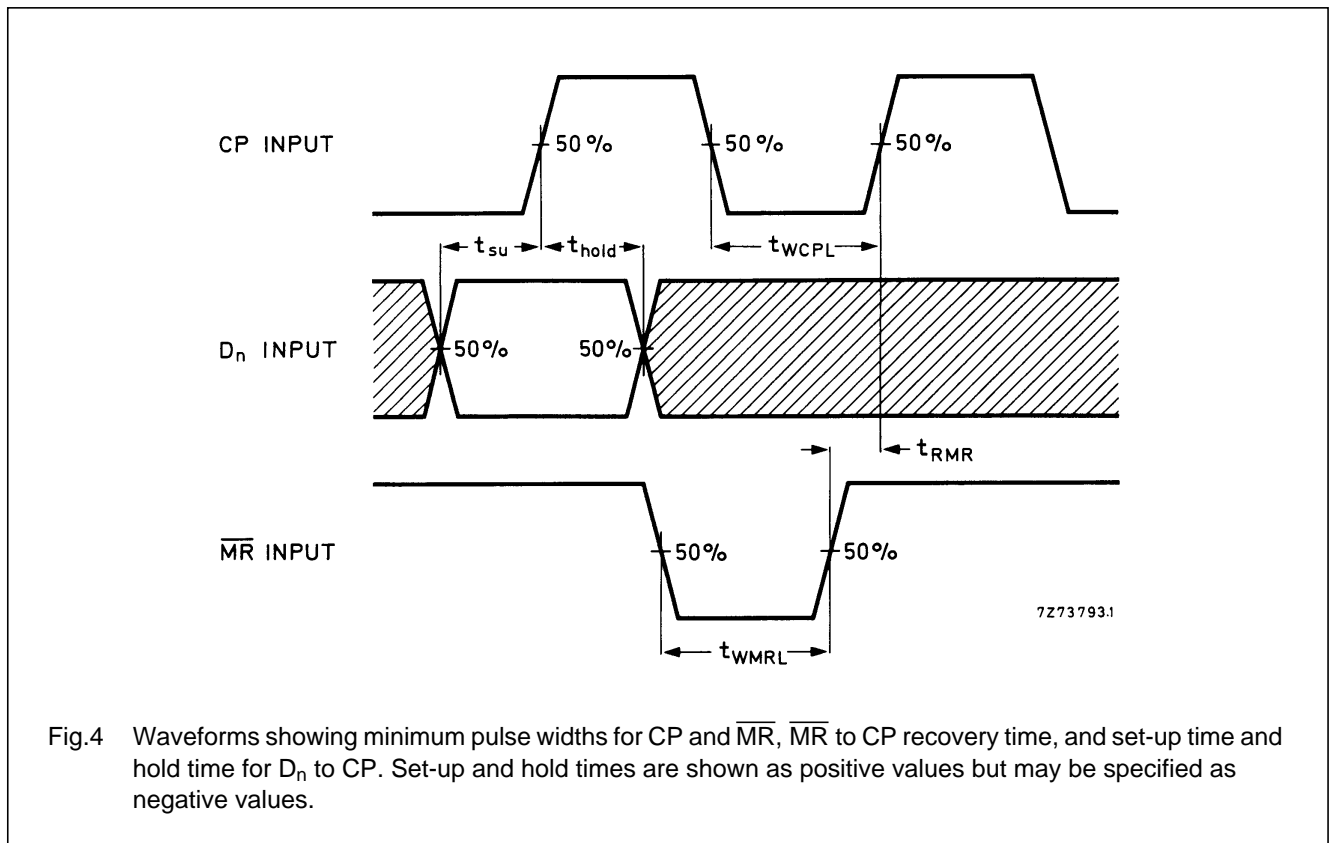


Fig.4 Waveforms showing minimum pulse widths for CP and MR, MR to CP recovery time, and set-up time and hold time for D<sub>n</sub> to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator